UFCF6Y-30-3 Embedded Systems Development

Practical 1 – Literature Review

Martin Serpell

Why do you need to know how to do a proper literature review?

Why do you need to know how to do a proper literature review?

I have only used it once in 30 years as a developer

Why do you need to know how to do a proper literature review?

As a researcher I need to do literature reviews regularly. They let me know what work other people have already been done so that I do not waste my time re-inventing something

But, why do you need to know how to do a proper literature review?

But, why do you need to know how to do a proper literature review?

20% of your **final year project** marks are for your **literature review**

How should you do a literature review?

How should you do a literature review?

You should **NOT** go onto **Wikipedia**!

How should you do a literature review?

You should **NOT** go onto **Wikipedia**!

Anyone can write **anything** at **anytime** on Wikipedia and so it is **not a reliable source of information**

How should you do a literature review?

At a bare minimum you should use Google Scholar to search for peer reviewed conference and journal papers

Lets look and see what recent research has been done on multi-processor embedded systems

Lets see what we can find using Google Scholar

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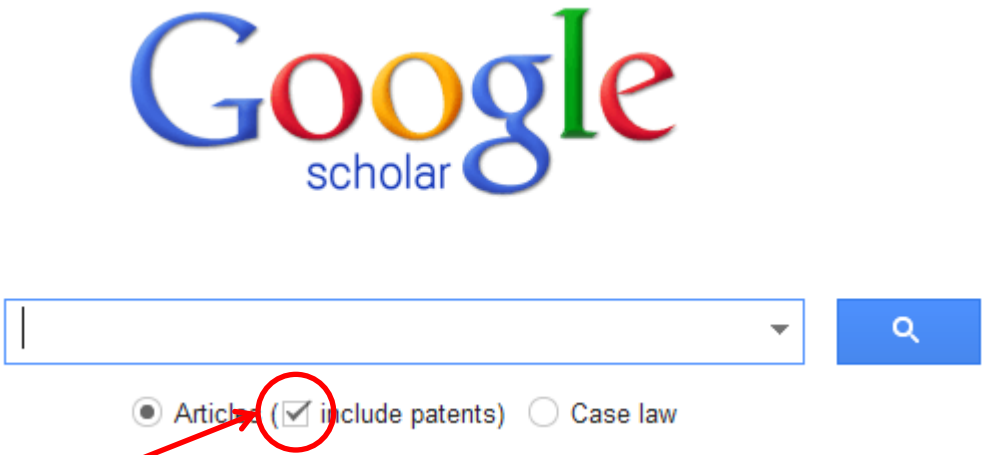

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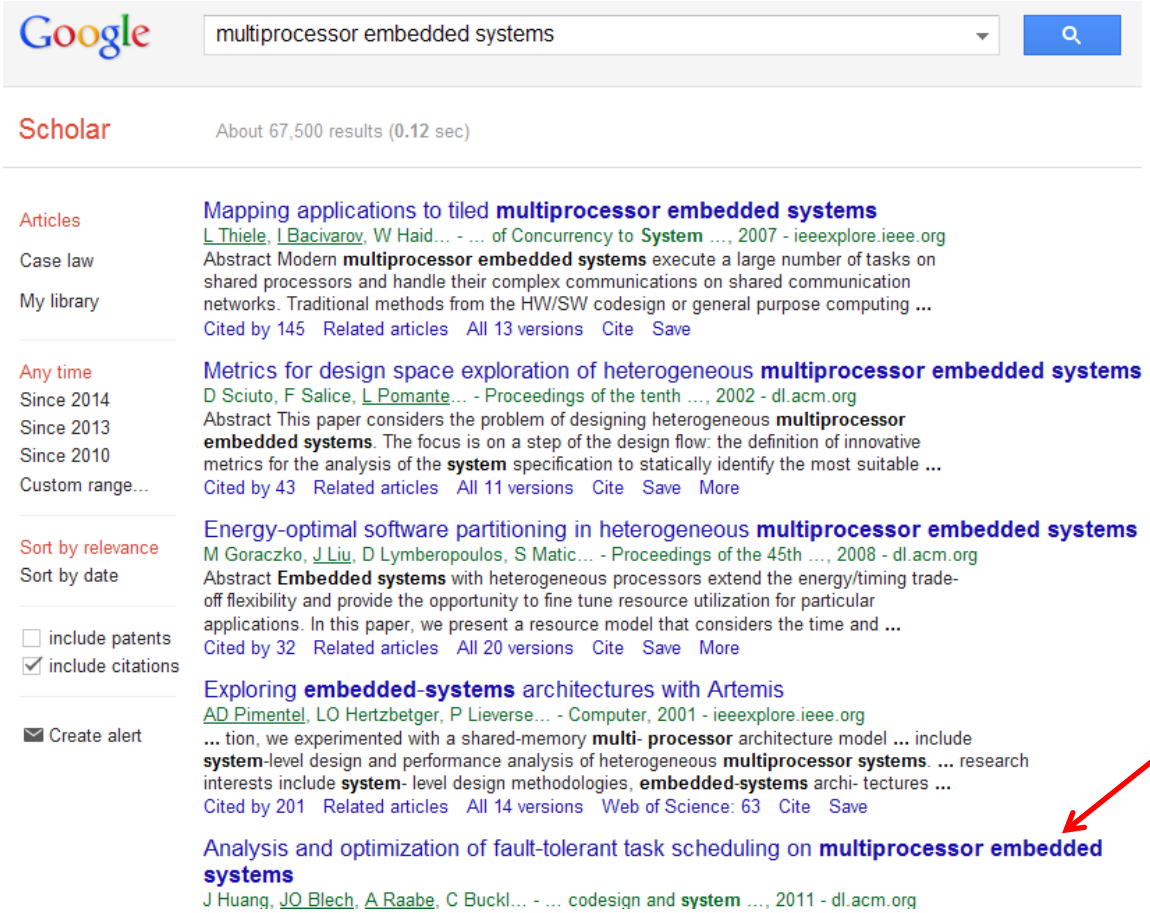
Search for multiprocessor embedded systems



This one looks like it might be interesting

Analysis and optimization of fault-tolerant task scheduling on multiprocessor embedded systems

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Alois Knoll Technische Universität München, Munich, Germany

2011 Article

Published in:

· Proceeding
CODES+ISSS '11 Proceedings of the seventh IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis
Pages 247-256
ACM New York, NY, USA ©2011
table of contents ISBN: 978-1-4503-0715-4 doi>10.1145/2039370.2039409

Reliability is a major requirement for most safety-related systems. To meet this requirement, fault-tolerant techniques such as hardware replication and software re-execution are often utilized. In this paper, we tackle the problem of analysis and optimization of fault-tolerant task scheduling for multiprocessor embedded systems. A set of existing fault- and process-models are adopted and a Binary Tree Analysis (BTA) is proposed to compute the system-level reliability in the presence of software/hardware redundancy. The BTA is integrated into a multi-objective evolutionary algorithm via a two-step encoding to perform reliability-aware design optimization. The optimization results contain the mapping of tasks to processing elements, the exact task and message schedule and the fault-tolerance policy assignment. Based on the observation that permanent faults need to be considered together with transient faults to achieve optimal system design, we propose a virtual mapping technique to take both types of faults into account. To the best of our knowledge, this is the first

Analysis and optimization of fault-tolerant task scheduling on multiprocessor embedded systems

Full Text: PDF

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Abstract

Reliability is a major requirement for most safety-related systems. To meet this requirement, fault-tolerant techniques such as hardware replication and software re-execution are often utilized. In this paper, we tackle the problem of analysis and optimization of fault-tolerant task scheduling for multiprocessor embedded systems. A set of existing fault- and process-models are adopted and a Binary Tree Analysis (BTA) is proposed to compute the system-level reliability in the presence of software/hardware redundancy. The BTA is integrated into a multi-objective evolutionary algorithm via a two-step encoding to perform reliability-aware design optimization. The optimization results contain the mapping of tasks to processing elements, the exact task and message schedule and the fault-tolerance policy assignment. Based on the observation that permanent faults need to be considered together with transient faults to achieve optimal system design, we propose a virtual mapping technique to take both types of faults into account. To the best of our knowledge, this is the first

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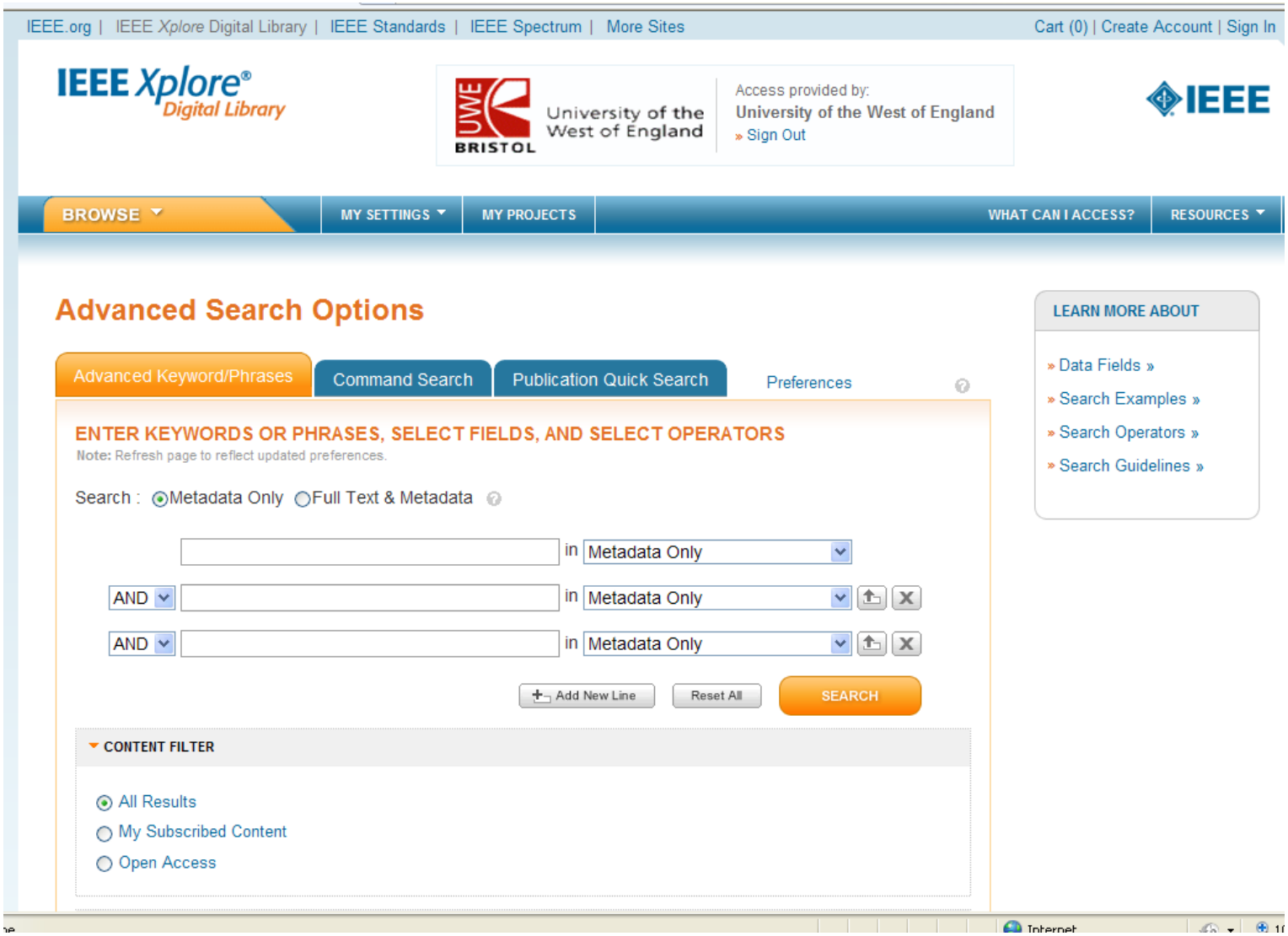

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Yuan Cai ; Reddy, S.M. ; Pomeranz, I. ; Al-Hashimi, B.M.

Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on

DOI: 10.1109/ISCAS.2005.1464663

Publication Year: 2005 , Page(s): 616 - 619 Vol. 1

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- The abstract
- The whole document

Use the **Advanced Search** to narrow in on the papers of interest

Keep a table of statistics showing in what database you searched, what search terms you used and how many papers you found.

This will make a nice **Appendix** in your **Final Year Project**

Search Engine/Database: ERIC and ProQuest search facility (tick peer reviewed).

Phrase	Hits	Title interesting	Abstract interesting	Full Paper available	Paper interesting
ti("on-line learning") AND ti((Study OR Comparison))	53	23	13	8	8
ti("on-line teaching") AND ti((Study OR Comparison))	9	5	4	4	4
ti("on-line education") AND ti((Study OR Comparison))	4	1	1	0	
ti("on-line courses") AND ti((Study OR Comparison))	7	4	4	4	4
ti(“remote learning” ") AND ti((Study OR Comparison))	0				
ti(“remote teaching” ") AND ti((Study OR Comparison))	0				
ti(“remote education” ") AND ti((Study OR Comparison))	0				
ti(“remote courses ") AND ti((Study OR Comparison))	0				
ti("distance learning") AND ti((Study OR Comparison))	53	6	2	0	
ti("distance teaching") AND ti((Study OR Comparison	5	0			
ti("distance education") AND ti((Study OR	79	9	3	1	1

Filter out the papers that are not relevant by...

1. Title
2. Abstract
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When you have a list of interesting papers download them and save them into a subdirectory

Cut and Paste the interesting bits from the .pdf into a Word document

Get rid of

Experimental results show the better effectiveness of the proposed procedure compared with a DVS procedure for distributed embedded systems [4] that assigned slack iteratively to the latest executed tasks (Cai et al, 2005).

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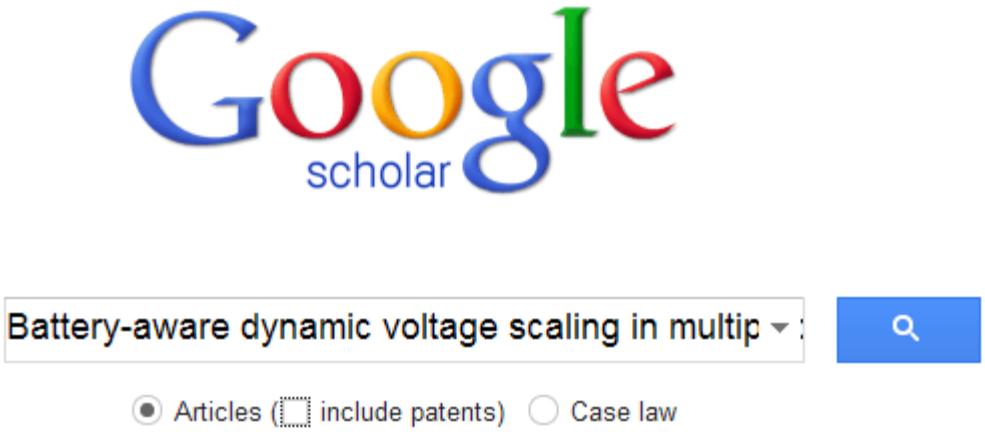

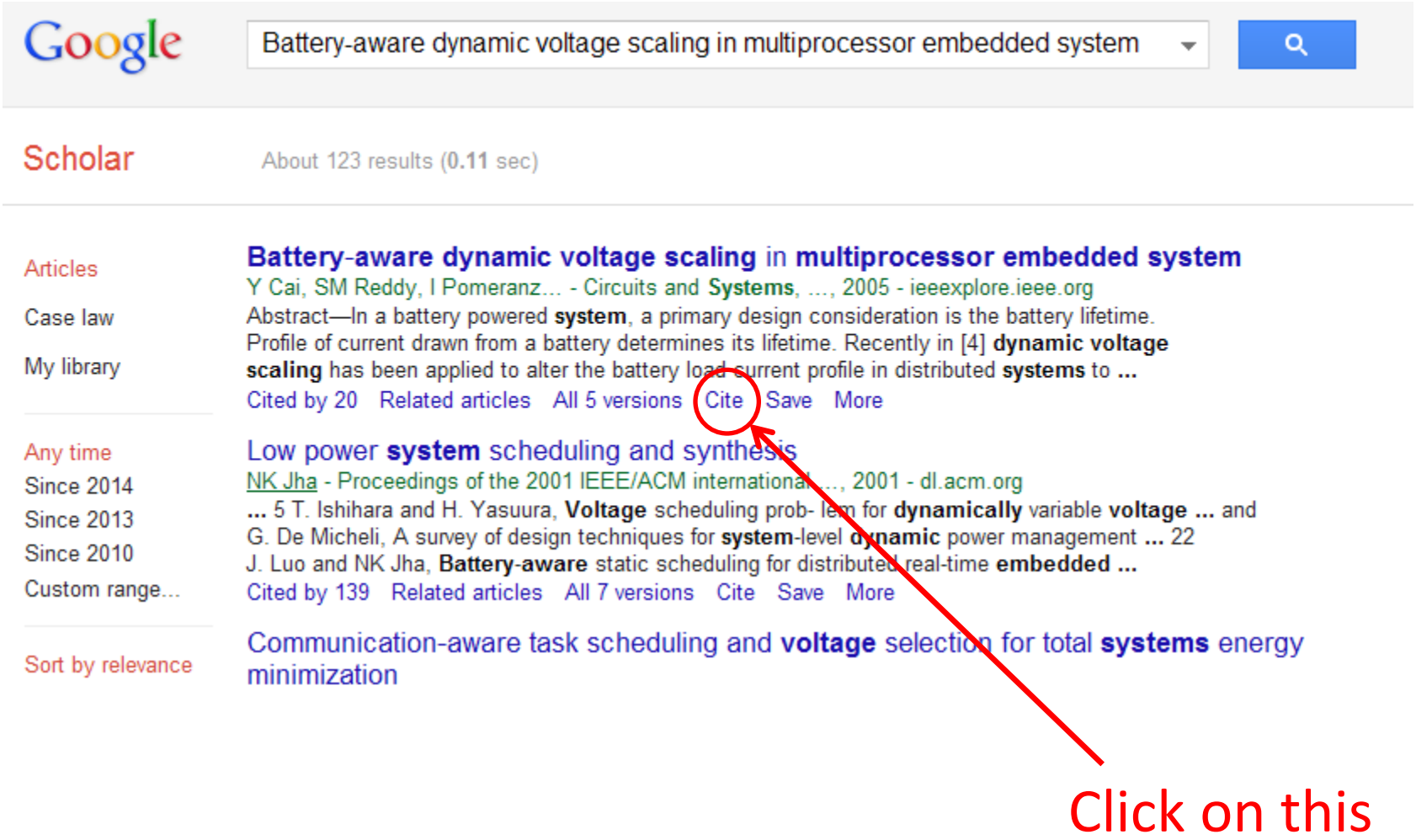
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Y Cai, SM Reddy, I Pomeranz... - Circuits and Systems, ..., 2005 - ieeexplore.ieee.org
Abstract—In a battery powered system, a primary design consideration is the battery lifetime. Profile of current drawn from a battery determines its lifetime. Recently in [4] dynamic voltage scaling has been applied to alter the battery load current profile in distributed systems to ...
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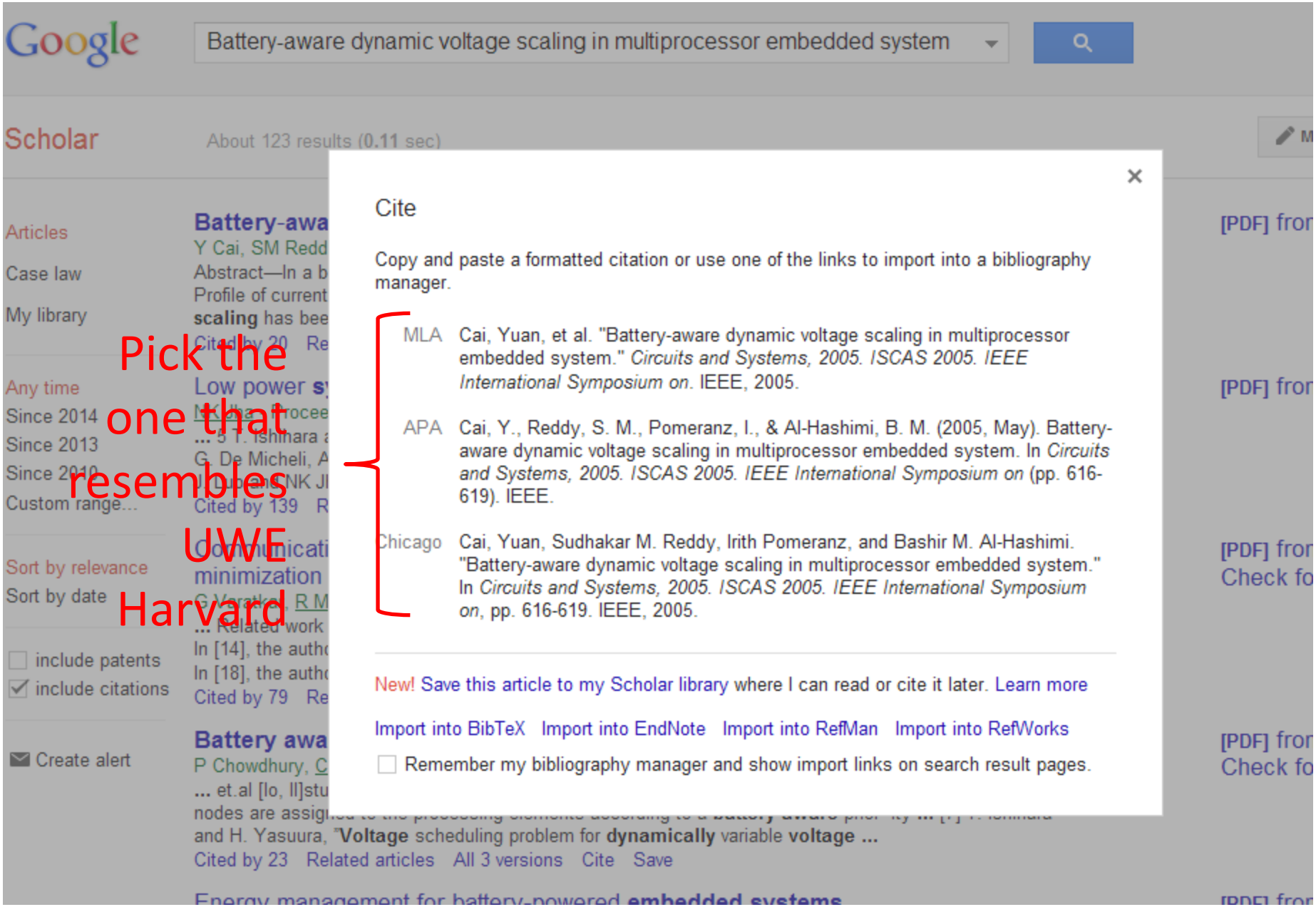
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MLA Cai, Yuan, et al. "Battery-aware dynamic voltage scaling in multiprocessor embedded system." Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on. IEEE, 2005.
APA Cai, Y., Reddy, S. M., Pomeranz, I., & Al-Hashimi, B. M. (2005, May). Battery-aware dynamic voltage scaling in multiprocessor embedded system. In Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on (pp. 616-619). IEEE.
Chicago Cai, Yuan, Sudhakar M. Reddy, Irith Pomeranz, and Bashir M. Al-Hashimi. "Battery-aware dynamic voltage scaling in multiprocessor embedded system." In Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on, pp. 616-619. IEEE, 2005.
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Remember

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