CTA01 – Huiswerk week 7

Vandaag hebben we paragraaf 5.1 t/m 5.4 van het boek behandeld. De slides staan op de de wiki in pptx en pdf formaat. We hebben van H5 slide 1 t/m 47 behandeld.

Huiswerk

Lees paragraaf 5.1 t/m 5.4 door. Vragen over de tekst graag uiterlijk volgende lesweek dinsdag 23:59 uur mailen zodat ik ze op woensdag in de les kan behandelen. Vergeet niet om de 'check yourself' oefeningen te maken. De antwoorden staan op p .513.

Maak de volgende opgaven uit paragraaf 5.19: 5.1 t/m 5.3, 5.5 en 5.10 t/m 5.12

Vragen over de opgaven graag uiterlijk volgende lesweek dinsdag 23:59 uur mailen zodat ik ze op woensdag in de les kan behandelen. Maak een issue aan op de wiki als je een fout in dit document hebt gevonden.

Mijn antwoorden

5.1.1 2

5.1.2 `I`, `J`, and `B[I][0]`

5.1.3 `A[I][J]`

5.1.4 `I`, `J`, and `B[I][0]`

5.1.5 `A(J, I)` and `B[I][0]`

5.1.6 32 004 with Matlab
32 008 with C

5.2.1 See Table 1.

5.2.2 See Table 2.

5.2.3 For cache 1: see Table 3. Miss rate cache 1 = 100 %.
For cache 2: see Table 4. Miss rate cache 2 = 83 %.
For cache 3: see Table 5. Miss rate cache 3 = 92 %.

Table 1: Cache behavior for Excercise 5.2.1.

Word adress	Binary address	Tag	Index	Miss/Hit
0x03	0b00000011	0000	0011	Miss
0xB4	0b10110100	1011	0100	Miss
0x2B	0b00111011	0011	1011	Miss
0x02	0b00000010	0000	0010	Miss
0xBF	0b10111111	1011	1111	Miss
0x58	0b01011000	0101	1000	Miss
0xBE	0b10111110	1011	1110	Miss
0x0E	0b00001110	0000	1110	Miss
0xB5	0b10110101	1011	0101	Miss
0x2C	0b00101100	0010	1100	Miss
0xBA	0b10111010	1011	1010	Miss
0xFD	0b11111101	1111	1101	Miss

Conclusion cache 2 has the lowest miss rate

5.3.1 364 544 bit

5.3.2 549 376 bit This is a 51 % increase when compared to 5.3.1.

5.3.3 The larger block size may require an increased hit time and an increased miss penalty than the original cache. The fewer number of blocks may cause a higher conflict miss rate than the original cache.

5.3.4 Associative caches are designed to reduce the rate of conflict misses. As such, a sequence of read requests with the same 12-bit index field but a different tag field will generate many misses. For the cache described above, the sequence 0, 32768, 0, 32768, 0, 32768, . . . , would miss on every access, while a two-way set associate cache with LRU replacement,

Table 2: Cache behavior for Excercise 5.2.2.

Word adress	Binary address	Tag	Index	Offset	Miss/Hit
0x03	0b00000011	0000	001	1	Miss
0xB4	0b10110100	1011	010	0	Miss
0x2B	0b00111011	0011	101	1	Miss
0x02	0b00000010	0000	001	0	Hit
0xBF	0b10111111	1011	111	1	Miss
0x58	0b01011000	0101	100	0	Miss
0xBE	0b10111110	1011	111	0	Hit
0x0E	0b00001110	0000	111	0	Miss
0xB5	0b10110101	1011	010	1	Hit
0x2C	0b00101100	0010	110	0	Miss
0xBA	0b10111010	1011	101	0	Miss
0xFD	0b11111101	1111	110	1	Miss

even one with a significantly smaller overall capacity, would hit on every access after the first two.

5.5.1 8 words van 32-bits

5.5.2 32 blocks

5.5.3 The ratio is 1.21

5.5.4 See Table 6.

5.5.5 33 %

5.5.6
```
<0, 3, Mem[0x0..0C00]-Mem[0x0..0C1F]>
<4, 2, Mem[0x0..0880]-Mem[0x0..089F]>
<5, 0, Mem[0x0..00A0]-Mem[0x0..00BF]>
<7, 0, Mem[0x0..00E0]-Mem[0x0..00FF]>
```

Table 3: Cache behavior for Excercise 5.2.3 (cache 1)

Word adress	Binary address	Tag	Index	Miss/Hit
0x03	0b00000011	00000	011	Miss
0xB4	0b10110100	10110	100	Miss
0x2B	0b00111011	00111	011	Miss
0x02	0b00000010	00000	010	Miss
0xBF	0b10111111	10111	111	Miss
0x58	0b01011000	01011	000	Miss
0xBE	0b10111110	10111	110	Miss
0x0E	0b00001110	00001	110	Miss
0xB5	0b10110101	10110	101	Miss
0x2C	0b00101100	00101	100	Miss
0xBA	0b10111010	10111	010	Miss
0xFD	0b11111101	11111	101	Miss

5.10.1 P1 1.515 GHz
P2 1.110 GHz

5.10.2 P1 9.56 cycles
P2 5.68 cycles

5.10.3 P1 12.64 CPI
P2 7.36 CPI P2 is faster (calculate time per instruction for P1 and P2 to determine which is faster)

5.10.4 AMAT = 9.85 cycles. The AMAT is worse with the L2 cache.

5.10.5 13.04 CPI

5.10.6 miss rate < 0.916

5.10.7 miss rate < 0.693

Table 4: Cache behavior for Excercise 5.2.3 (cache 2)

Word adress	Binary address	Tag	Index	Offset	Miss/Hit
0x03	0b00000011	00000	01	1	Miss
0xB4	0b10110100	10110	10	0	Miss
0x2B	0b00111011	00111	01	1	Miss
0x02	0b00000010	00000	01	0	Miss
0xBF	0b10111111	10111	11	1	Miss
0x58	0b01011000	01011	00	0	Miss
0xBE	0b10111110	10111	11	0	Hit
0x0E	0b00001110	00001	11	0	Miss
0xB5	0b10110101	10110	10	1	Hit
0x2C	0b00101100	00101	10	0	Miss
0xBA	0b10111010	10111	01	0	Miss
0xFD	0b11111101	11111	10	1	Miss

5.11.1 Each line in the cache will have a total of six blocks (two in each of three ways). There will be a total of $48/6 = 8$ lines.

5.11.2 See Table 7.

5.11.3 The cache has 8 words and every address can be mapped to one of the 8 words. There are 8 comperators and there is no index.

5.11.4 See Table 8.

5.11.5 The cache has 4 blocks (lines). Every block contains two adjacent words. Every address can be mapped to one of the 4 blocks. There are 4 comperators and there is no index. There is an offset of one bit.

5.11.6 See Table 9.

5.11.7 See Table 10.

5.11.8 There are more correct answers. For example: see Table 11.

Table 5: Cache behavior for Excercise 5.2.3 (cache 3)

Word adress	Binary address	Tag	Index	Offset	Miss/Hit
0x03	0b00000011	00000	0	11	Miss
0xB4	0b10110100	10110	1	00	Miss
0x2B	0b00111011	00111	0	11	Miss
0x02	0b00000010	00000	0	10	Miss
0xBF	0b10111111	10111	1	11	Miss
0x58	0b01011000	01011	0	00	Miss
0xBE	0b10111110	10111	1	10	Hit
0x0E	0b00001110	00001	1	10	Miss
0xB5	0b10110101	10110	1	01	Miss
0x2C	0b00101100	00101	1	00	Miss
0xBA	0b10111010	10111	0	10	Miss
0xFD	0b11111101	11111	1	01	Miss

5.12.1 L1 only: CPI = 15.5 Direct mapped L2: CPI = 2.83 8-way set associated L2: CPI = 3.67 Doubled memory access time L1 only: CPI = 29.5 (90 % increase) Direct mapped L2: CPI = 3.32 (17 % increase) 8-way set associated L2: CPI = 3.88 (5 % increase)

5.12.2 CPI = 2.47 Adding the L3 cache does reduce the overall memory access time, which is the main advantage of having an L3 cache. The disadvantage is that the L3 cache takes real estate away from having other types of resources, such as functional units.

5.12.3 No size will achieve the performance goal.

Table 6: Cache behavior for Excercise 5.5.4.

Byte adress	Binary address	Tag	Index	Offset	Miss/Hit	Bytes replaced
0x0..0000	0b0..0000000000000	0..00	00000	00000	Miss	
0x0..0004	0b0..0000000000100	0..00	00000	00100	Hit	
0x0..0010	0b0..0000000010000	0..00	00000	10000	Hit	
0x0..0084	0b0..0000010000100	0..00	00100	00100	Miss	
0x0..00E8	0b0..0000011101000	0..00	00111	01000	Miss	
0x0..00A0	0b0..0000010100000	0..00	00101	00000	Miss	
0x0..0400	0b0..0010000000000	0..01	00000	00000	Miss	0x0..000 - 0x0..01F
0x0..001E	0b0..0000000011110	0..00	00000	11110	Miss	0x0..400 - 0x0..41F
0x0..008C	0b0..0000000011100	0..00	00000	11100	Hit	
0x0..0C1C	0b0..0110000011100	0..11	00000	11100	Miss	0x0..000 - 0x0..01F
0x0..00B4	0b0..0000010110100	0..00	00101	10100	Hit	
0x0..0884	0b0..0100010000100	0..10	00100	00100	Miss	0x0..080 - 0x0..09F

Table 7: Cache behavior for Excercise 5.11.2.

Word adress	Binary address	Tag	Index	Offset	Way	Miss/Hit
0x03	0b00000011	0000	001	1	0	Miss
0xB4	0b10110100	1011	010	0	0	Miss
0x2B	0b00101011	0010	101	1	0	Miss
0x02	0b00000010	0000	001	0	0	Hit
0xBE	0b10111110	1011	111	0	0	Miss
0x58	0b01011000	0101	100	0	0	Miss
0xBF	0b10111111	1011	111	1	0	Hit
0x0E	0b00001110	0000	111	0	1	Miss
0x1F	0b00011111	0001	111	1	2	Miss
0xB5	0b10110101	1011	010	1	0	Hit
0xBF	0b10111111	1011	111	1	0	Hit
0xBA	0b10111010	1011	101	0	1	Miss
0x2E	0b00101110	0010	111	1	1	Miss
0xCE	0b11001110	1100	111	1	2	Miss

Table 8: Cache behavior for Excercise 5.11.4.

Word adress	Binary address	Tag	Way	Miss/Hit
0x03	0b00000011	00000011	0	Miss
0xB4	0b10110100	10110100	1	Miss
0x2B	0b00101011	00101011	2	Miss
0x02	0b00000010	00000010	3	Miss
0xBE	0b10111110	10111110	4	Miss
0x58	0b01011000	01011000	5	Miss
0xBF	0b10111111	10111111	6	Miss
0x0E	0b00001110	00001110	7	Miss
0x1F	0b00011111	00011111	0	Miss
0xB5	0b10110101	10110101	1	Miss
0xBF	0b10111111	10111111	6	Hit
0xBA	0b10111010	10111010	2	Miss
0x2E	0b00101110	00101111	3	Miss
0xCE	0b11001110	11001111	4	Miss

Table 9: Cache behavior for Excercise 5.11.6.

Word adress	Binary address	Tag	Offset	Way	Miss/Hit
0x03	0b00000011	0000001	1	0	Miss
0xB4	0b10110100	1011010	0	1	Miss
0x2B	0b00101011	0010101	1	2	Miss
0x02	0b00000010	0000001	0	0	Hit
0xBE	0b10111110	1011111	0	3	Miss
0x58	0b01011000	0101100	0	1	Miss
0xBF	0b10111111	1011111	1	3	Hit
0x0E	0b00001110	0000111	0	2	Miss
0x1F	0b00011111	0001111	1	0	Miss
0xB5	0b10110101	1011010	1	1	Miss
0xBF	0b10111111	1011111	1	3	Hit
0xBA	0b10111010	1011101	0	2	Miss
0x2E	0b00101110	0010111	1	0	Miss
0xCE	0b11001110	1100111	1	1	Miss

Table 10: Cache behavior for Excercise 5.11.7.

Word adress	Binary address	Tag	Offset	Way	Miss/Hit
0x03	0b00000011	0000001	1	0	Miss
0xB4	0b10110100	1011010	0	1	Miss
0x2B	0b00101011	0010101	1	2	Miss
0x02	0b00000010	0000001	0	0	Hit
0xBE	0b10111110	1011111	0	3	Miss
0x58	0b01011000	0101100	0	3	Miss
0xBF	0b10111111	1011111	1	3	Miss
0x0E	0b00001110	0000111	0	3	Miss
0x1F	0b00011111	0001111	1	3	Miss
0xB5	0b10110101	1011010	1	1	Hit
0xBF	0b10111111	1011111	1	1	Miss
0xBA	0b10111010	1011101	0	1	Miss
0x2E	0b00101110	0010111	1	1	Miss
0xCE	0b11001110	1100111	1	1	Miss

Table 11: Cache behavior for Excercise 5.11.8.

Word adress	Binary address	Tag	Offset	Way	Miss/Hit
0x03	0b00000011	0000001	1	0	Miss
0xB4	0b10110100	1011010	0	1	Miss
0x2B	0b00101011	0010101	1	2	Miss
0x02	0b00000010	0000001	0	0	Hit
0xBE	0b10111110	1011111	0	3	Miss
0x58	0b01011000	0101100	0	0	Miss
0xBF	0b10111111	1011111	1	3	Hit
0x0E	0b00001110	0000111	0	0	Miss
0x1F	0b00011111	0001111	1	0	Miss
0xB5	0b10110101	1011010	1	1	Hit
0xBF	0b10111111	1011111	1	3	Hit
0xBA	0b10111010	1011101	0	0	Miss
0x2E	0b00101110	0010111	1	0	Miss
0xCE	0b11001110	1100111	1	0	Miss