BỘ GIAO THÔNG VẬN TẢI

TRƯỜNG ĐẠI HỌC GIAO THÔNG VẬN TẢI TP.HỒ CHÍ MINH

KIẾN TRÚC MÁY TÍNH

ĐỀ TÀI:

TỔNG QUAN VỀ IBM POWER E1050

Nhóm phụ trách: **Nhóm**

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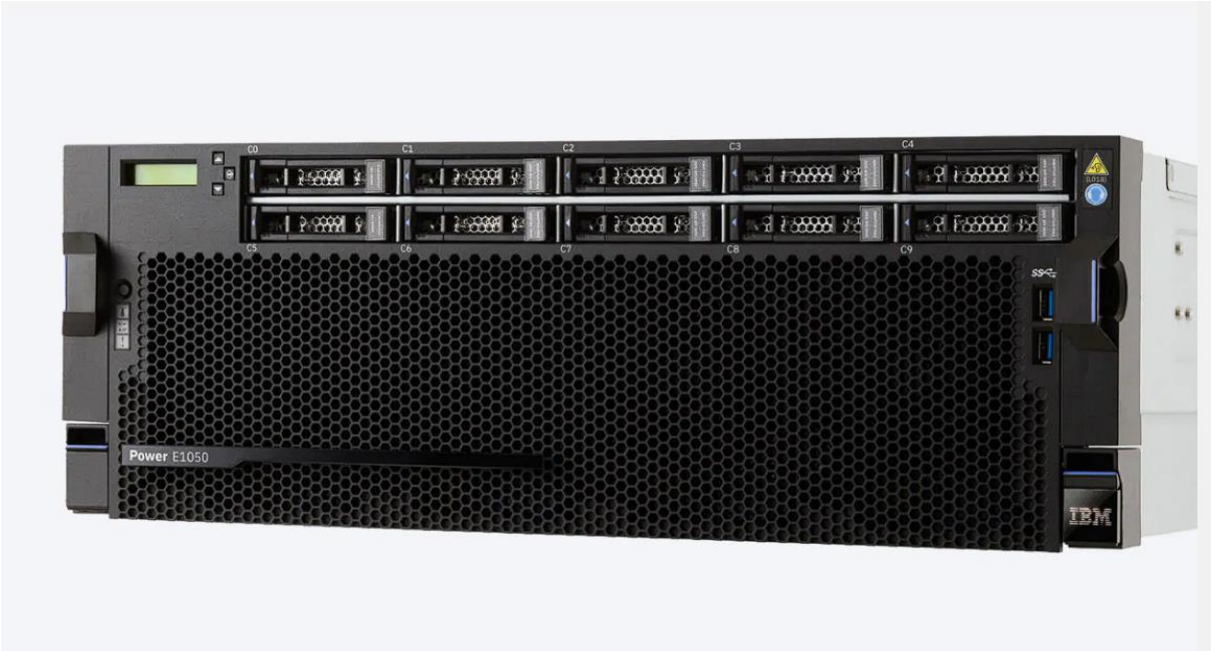
Đỗ Đăng Tú

Khóa học : **2022-2023**

Mục lục

I. Overview: IBM Power E1050

- High performance, secure 4-socket server with industry leading reliability designed for dynamic demands of enterprise computing.



- The core applications, data stores and processes that run your business simply cannot go down, no matter what. With accelerated digital adoption, the demands on these applications are increasing, along with security risks. To meet the challenges of today's market, your IT infrastructure needs to be modernized. This requires an infrastructure platform that efficiently scales to meet your business demands, protects your applications and data with pervasive and layered security, and enables you to transform data into insights quickly.

- IBM Power E1050 offers a unique blend of enterprise-class capabilities in a space-efficient 4-socket 4U form factor. The Power E1050 server allows you to:
    - Respond faster to business demands with world record performance scalability for core enterprise workloads and flexible consumption options to enhance your hybrid cloud experience.
    - Protect data from core to cloud with accelerated encryption and new in-core defense against return- oriented programming attacks.
    - Streamline insights and automation with in-core AI inferencing and machine learning.
    - Maximize reliability and availability with Open Memory Interface (OMI) attached memory DIMMs.

Source

II. Power E1050 hardware components:

1.Processor

The Power10 processor is a superscalar symmetric multiprocessor that is manufactured in complimentary metal-oxide-semiconductor (CMOS) 7-nm lithography with 18 layers of metal. The processor contains up to 15 cores that support eight simultaneous multithreading (SMT8) independent execution contexts.

Each core has private access to 2 MB L2 cache and local access to 8 MB of L3 cache capacity. The local L3 cache region of a specific core also is accessible from all other cores on the processor chip. The cores of one Power10 processor share up to 120 MB of latency optimized non-uniform cache access (NUCA) L3 cache.

The processor supports the following three distinct functional interfaces, which can run with a signaling rate of up to 32 GTps2 (Giga-transfers per second):

+ Open Memory Interface (OMI)

The Power10 processor has eight memory controller unit (MCU) channels that support one OMI port with two OMI links each.3 One OMI link aggregates eight lanes running at 32 GTps speed and connects to one memory buffer-based Differential Dual Inline Memory Module (DDIMM) slot to access main memory. Physically, the OMI interface is implemented in two separate die areas of eight

OMI links each. The maximum theoretical full-duplex bandwidth aggregated over all 128 OMI lanes is 1 TBps.

+ SMP fabric interconnect (Power A-bus/X-bus/OpenCAPI/Networking (PowerAXON))

A total of 144 lanes are available in the Power10 processor to facilitate the connectivity to other processors in an SMP architecture configuration. Each SMP connection requires 18 lanes, that is, eight data lanes plus one spare lane per direction (2 x(8+1)). Thus, the processor can support a maximum of eight SMP connections with at total of 128 data lanes per processor. This configuration yields a maximum theoretical full-duplex bandwidth aggregated over all SMP connections of 1 TBps .

The generic nature of the interface implementation also allows you to use 128 data lanes to potentially connect accelerator or memory devices through the OpenCAPI protocols. Also, this implementation can support memory cluster and memory interception architectures.

Because of the versatile characteristic of this technology, it is also referred to as

PowerAXON interface.4 The OpenCAPI and the memory clustering and memory

interception use cases can be pursued in the future, and they are currently not used by the available technology products.

+ Peripheral Component Interconnect Express (PCIe) Version 5.0 interface

To support external I/O connectivity and access to internal storage devices, the Power10 processor provides differential PCIe 5.0 interface busses (PCIe Gen 5) with a total of 32 lanes. The lanes are grouped in two sets of 16 lanes that can be used in one of the following configurations:

– One x16 PCIe Gen 4

– Two x8 PCIe Gen 4

– One x8, and two x4 PCIe Gen 4

– One x8 PCIe Gen 5, and one x8 PCIe Gen 4

– One x8 PCIe Gen 5, and two x4 PCIe Gen 4

Figure 2-2 shows the Power10 processor die with several functional units that are labeled. Sixteen SMT8 processor cores are shown, but the dual-chip module (DCM) with two Power10 processors provides 12-, 18-, or 24-core for Power E1050 server configurations

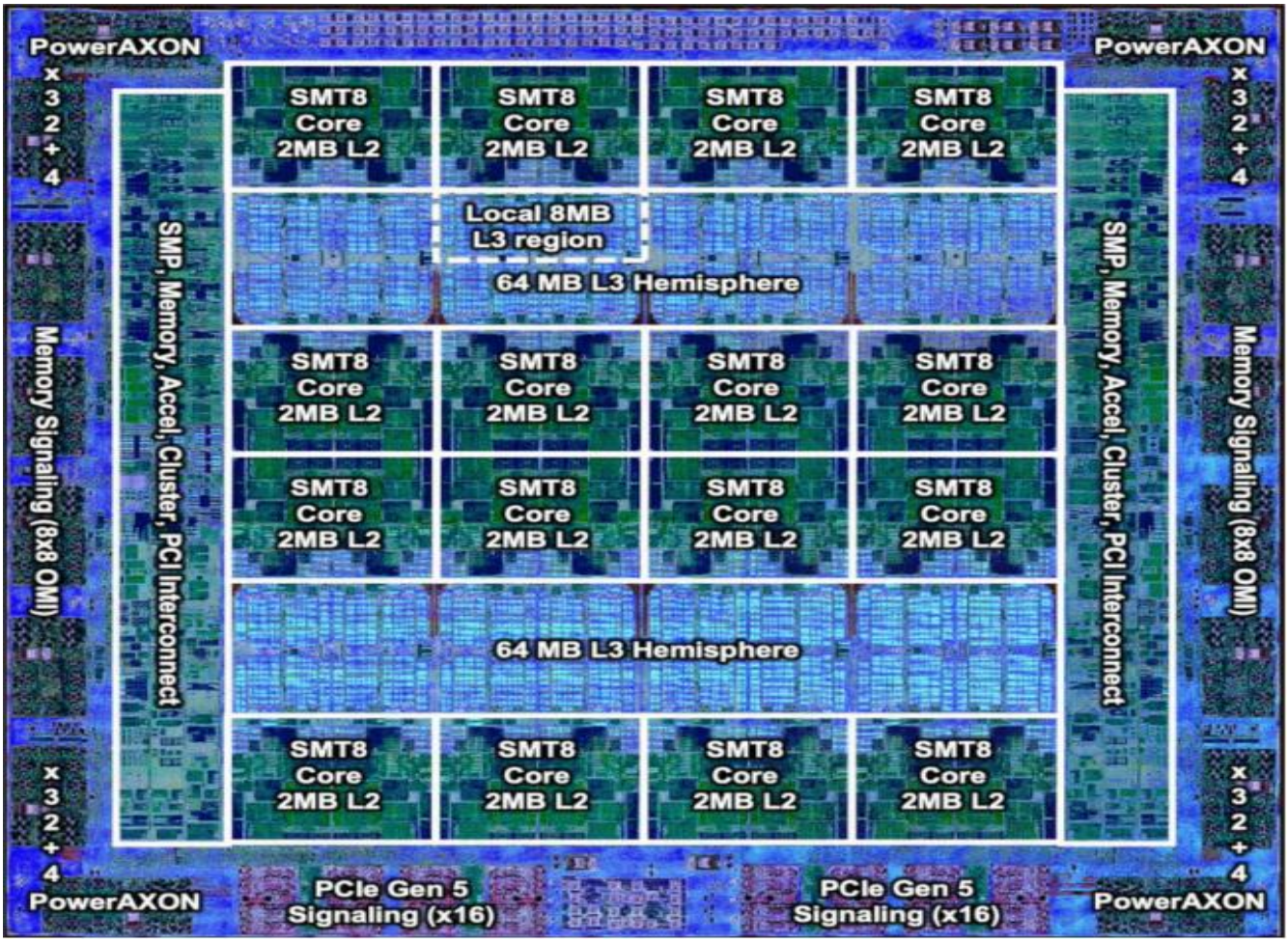


Figure 2-2 The Power10 processor chip (die photo courtesy of Samsung Foundry)
(https://www.anandtech.com/show/16936/ibm-power10-coming-to-market-e1080-for-frictionless-hybrid-cloud-experiences)

Important Power10 processor characteristics are listed in Table 2-1.

Table 2-1 Summary of the Power10 processor chip and processor core technology

Technology	Power10 processor chip
Processor die size	602 mm^2
Fabrication technology	► CMOS[a] 7-nm lithography ► 18 layers of metal
Maximum processor cores per chip	15
Maximum execution threads per core / chip	8 / 120
Maximum L2 cache core	2 MB
Maximum On-chip L3 cache per core / chip	8 MB / 120 MB

Technology	Power10 processor chip
Number of transistors	18 billion
Processor compatibility modes	Support for Power ISA[b] of Power8 and Power9

A. CMOS
B. Power ISA

The Power10 processor can be packaged as single-chip module (SCM) or DCM. The Power E1050 server implements the DCM version. The DCM contains two Power10 processors plus more logic that is needed to facilitate power supply and external connectivity to the module.

Figure 2-3 shows the logical diagram of the Power10 DCM.

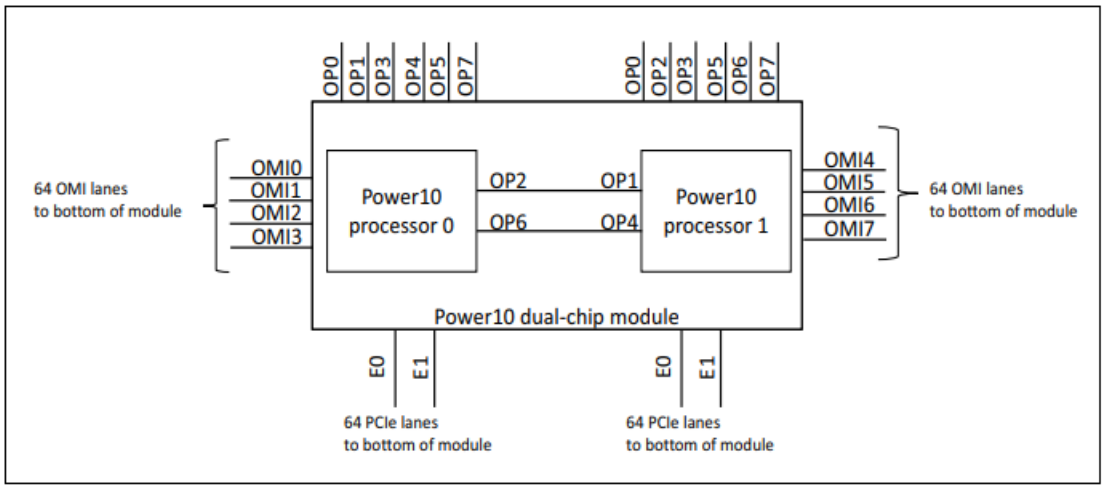


Figure 2-3 Power10 dual-chip module

Source: IBM Power E1050: Technical Overview and Introduction

2. Memory

2.1 Open Memory Interface (OMI)

The Power E1050 server uses the new and innovative OMI. OMI is a technology-neutral memory interface. The Power E1050 server supports DDIMMs that are based on DDR4 technology, which are plugged into the OMI slots. A maximum of 64 OMI slots are available in a server with all four processor sockets populated, with which a maximum of 16 TB of memory can be installed in to the server. In the following sections, the details about OMI and DDIMMs are described in more detail.

The OMI is driven by eight on-chip MCUs, and it is implemented in two separate physical building blocks that lie in opposite areas at the outer edge of the Power10 die. Each area supports 64 OMI lanes that are grouped in four OMI ports. One port in turn consists of two OMI links with eight lanes each, which operate in a latency-optimized manner with unprecedented bandwidth and scale at 32-Gbps speed. One Power10 processor chip supports the following functional elements to access main memory:

- Eight MCUs

- Eight OMI ports that are controlled one-to-one through a dedicated MCU
- Two OMI links per OMI port, for a total of 16 OMI links
- Eight lanes per OMI link for a total of 128 lanes, all running at 32-Gbps speed

The Power10 processor provides natively an aggregated maximum theoretical full-duplex memory interface bandwidth of 1 TBps per chip.

Memory interface architecture for dual-chip modules

The DCM that is used in the Power E1050 server combines two Power10 processor chips inone processor package. A total of 2 x 8 = 16 OMI ports and 2 x 16 = 32 OMI links are physically present on a Power10 DCM. But because the chips on the DCM are tightly integrated and the aggregated memory bandwidth of 8 OMI ports already culminates at a maximum theoretical full-duplex bandwidth of 1 TBps, only half of the OMI ports are active. Each chip of the DCM contributes four OMI ports and eight OMI links to facilitate main memory access. Figure 2-1 on page 35 and Figure 2-11 on page 61 show details about the OMI port designation and the physical location of the active OMI units of a DCM. In summary, one DCM supports the following functional elements to access main memory:

- Four active MCUs per chip, for a total of eight MCUs per module.
- Each MCU maps one-to-one to an OMI port.
- Four OMI ports per chip, for at total of eight OMI ports per module.
- Two OMI links per OMI port for a total of eight OMI links per chip and 16 OMI links per module.
- Eight lanes per OMI link for a total of 128 lanes per module, all running at 32-Gbps speed.

The Power10 DCM provides an aggregated maximum theoretical full-duplex memory interface bandwidth of 512 GBps per chip and 1 TBps per module

2.2 Maximum memory and maximum theoretical memory bandwidth

Maximum memory and maximum theoretical memory bandwidth The OMI physical interface enables low latency, high-bandwidth, and technology-neutral host memory semantics to the processor and allows attaching established and emerging memory elements. With the Power10 processor-based E1050 server, OMI initially supports one main tier, low-latency, and enterprise-grade DDR4 DDIMM per OMI link. This architecture yields a total memory module capacity of 16 DDIMMs per populated processor module (64 with all four modules populated).

The memory bandwidth and the total memory capacity depend on the DDIMM density and the associated DDIMM frequency that are configured for the Power E1050 server. Table 2-7 list the maximum memory and memory bandwidth per populated socket and the maximum values for a fully populated server.

Feature Code	DIMM size	DRAM speed	Max memory per socket	Max memory per server	Max memory bandwidth per socket	Max memory bandwidth per server
#EM75	64 GB (2 x32 GB)	3200 MHz	512 GB	2 TB	409 GBps	1.636 GBps
#EM76	128 GB (2 x64 GB)	3200 MHz	1 TB	4 TB	409 GBps	1.636 GBps
#EM77	256 GB (2 x128 GB)	2933 MHz	2 TB	8 TB	375 GBps	1.500 GBps
#EM7J	512 GB (2 x256 GB)	2933 MHz	4 TB	16 TB	375 GBps	1.500 GBps

Note: The 128 GB and 256 GB DDIMMs are planned to be available from 9 December 2022

2.3 Pervasive memory encryption

The Power10 MCU provides the system memory interface between the on-chip SMP interconnect fabric and the OMI links. This design qualifies the MCU as an ideal functional unit to implement memory encryption logic. The Power10 on-chip MCU encrypts and decrypts all traffic to and from system memory that is based on the AES technology.

The MCU crypto engine is transparently integrated into the data path, which ensures that the data fetch and store bandwidth are not compromised by the AES CTR encryption mode. Because the encryption has no noticeable performance effect and because of the obvious security benefit, the pervasive memory encryption is enabled by default, and it cannot be turned off through any administrative interface.

- ⇨ Enhanced security with transparent memory encryption which is designed to simplify encryption and support end-to-end security without affecting performance by using hardware features for a seamless user experience

Source: https://m.kaon.com/c/ib/qm5vPQ

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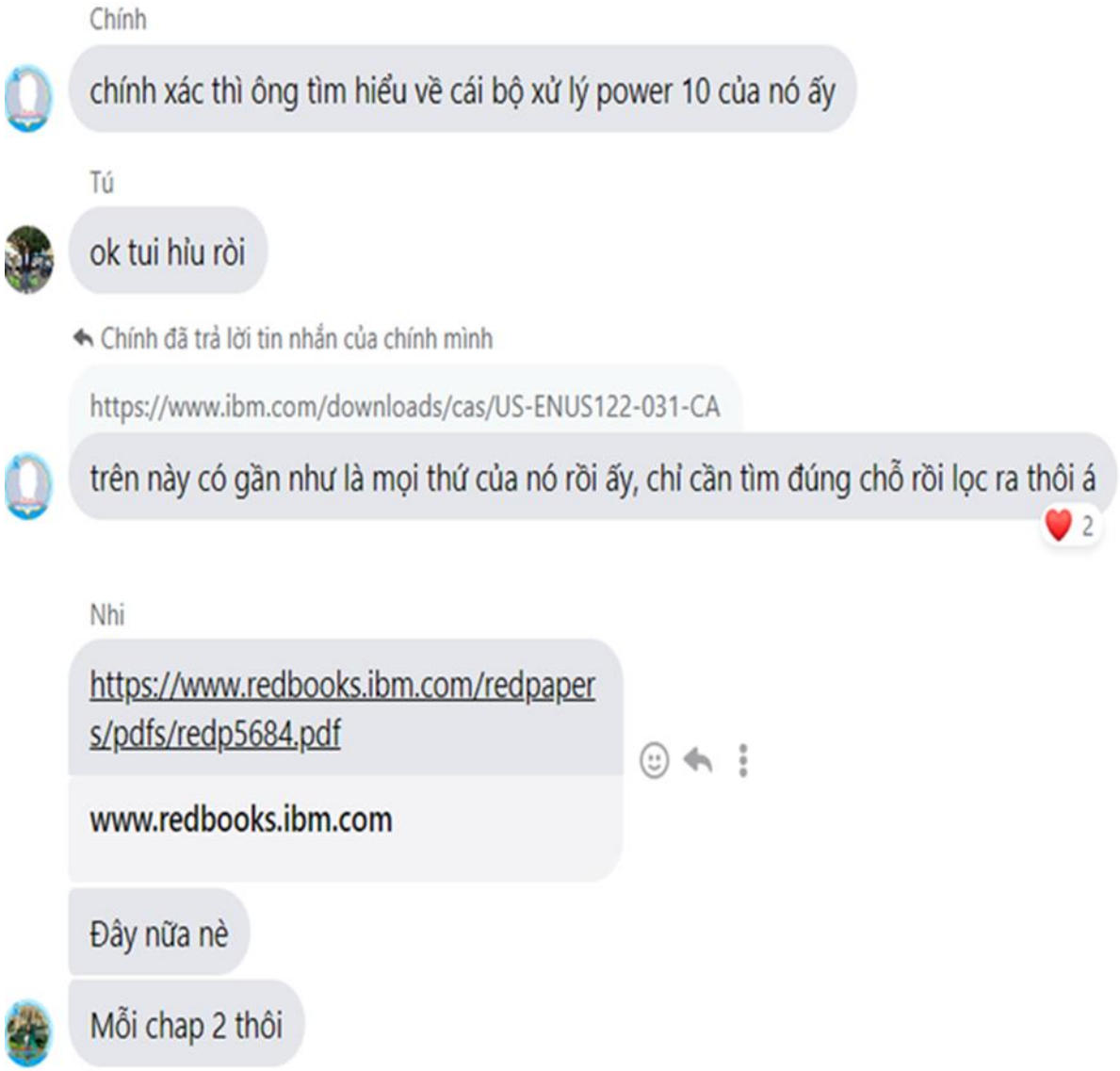


3.Input/Output

Eleven I/O PCIe adapter slots

PCIe Gen 5 provides 2X the bandwidth, gigatransfer and frequency of the prior generation (PCIe Gen4)

- Up to 8 of the 11 slots are PCIe Gen 5 capable, all slots are concurrently maintainable.
- Data can be transferred at substantially faster speeds.
- Ideal for large data, compute-intensive enterprise environment like Machine Learning (ML) and/or Artificial Intelligence (AI).

3.1 Virtual I/O Server

VIOS is part of the PowerVM Enterprise edition feature. VIOS is software that is installed in a special LPAR, which facilitates the sharing of physical I/O resources between client LPARs within the server. VIOS provides virtual Small Computer Serial Interface (SCSI) target, virtual FC, SEA, and PowerVM Active Memory Sharing capabilities to client LPARs within the system.

3.2. Internal I/O subsystem

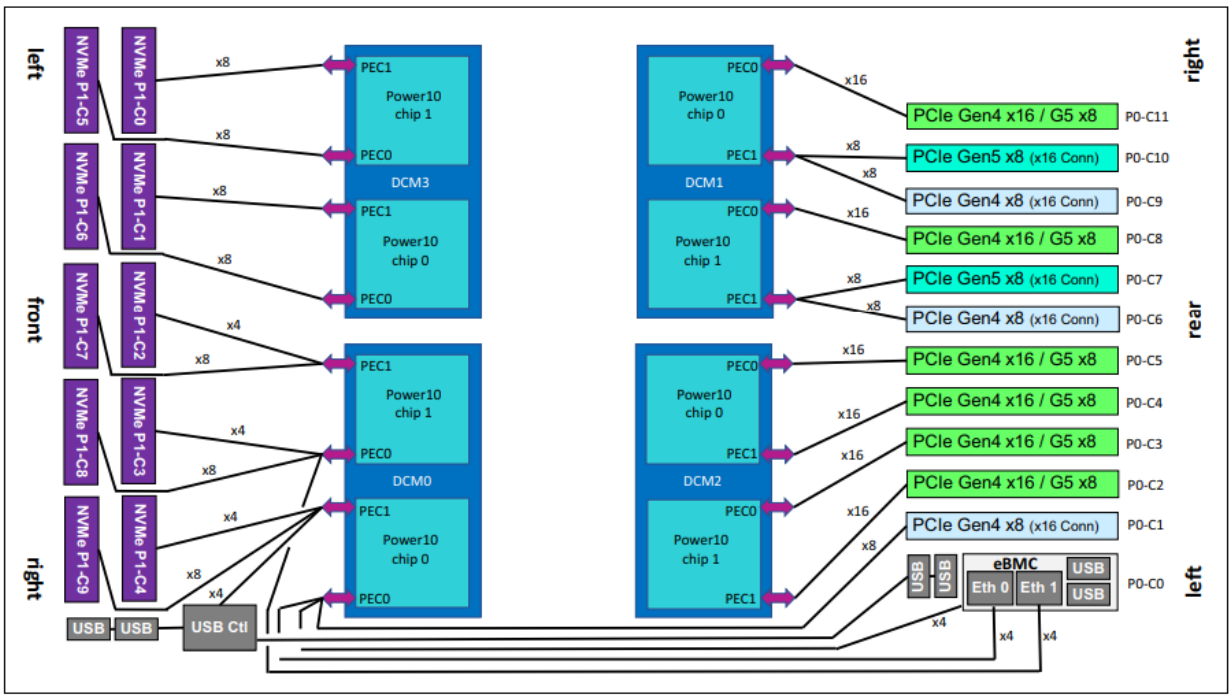
The internal I/O subsystem of the Power E1050 server is connected to the PCIe Express controllers on a Power10 chip in the system. A Power10 chip has two PCI

Express controllers (PECs) of 16 lanes each for a total of 32 Gen5/Gen4 lanes per chip and 64 Gen5/Gen4 lanes per DCM. Each PEC supports up to three PCI host bridges (PHBs) that directly connect to PCIe slots or devices. Both PEC0 and PEC1 can be configured as follows:

- One x16 Gen4 PHB or one x8 Gen5 PHB
- One x8 Gen5 and one x8 Gen4 PHB
- One x8 Gen5 PHB and two x4 Gen4 PHBs

PEC configuration	E-Bus ports	PHB
One x16 at DCM0	E0	PHB0
Two x8 at DCM0	E0A and E0B	PHB0 and PHB1
One x8 and two x4 at DCM0	E0A, E0B, and E0C	PHB0, PHB1, and PHB2
One x16 at DCM1	E1	PHB3
Two x8 at DCM1	E1A and E1B	PHB3 and PHB4
One x8 and two x4 at DCM1	E1A, E1B, and E1C	PHB3, PHB4, and PHB5

A DIAGRAM OF THE I/O SUBSYSTEM OF THE POWER E1050 SERVER



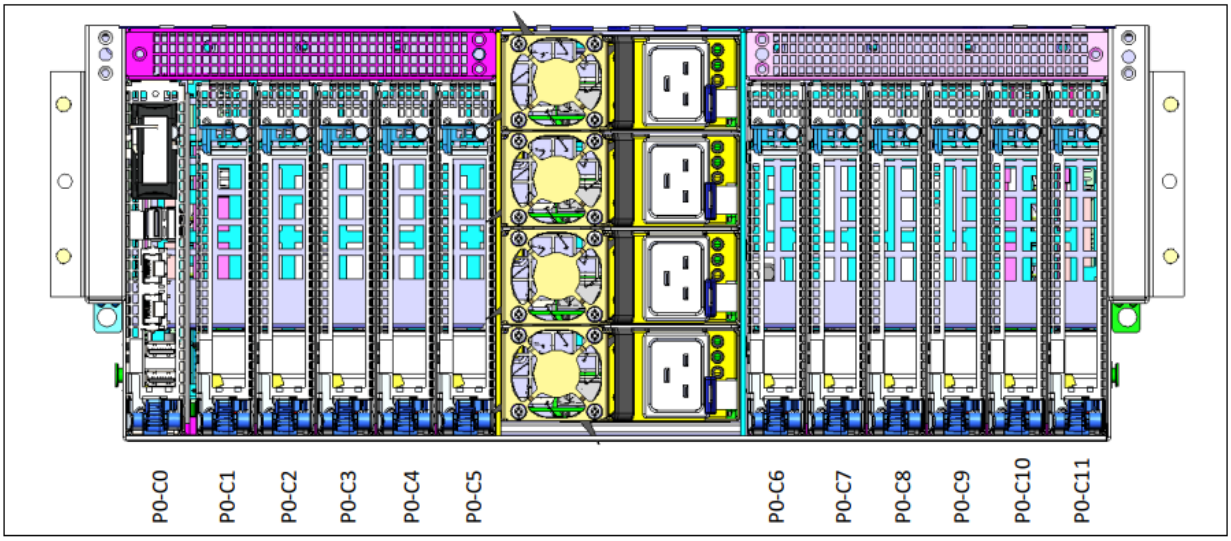
3.3. USB ports

The first DCM (DCM0) also hosts the USB controller that is connected by using four PHBs, although the USB controller uses only one lane. DCM0 provides four USB 3.0 ports, with two in the front and two in the back. The two front ports provide up to 1.5 A USB current, mainly to support the external USB DVD (Feature Code EUA5)

The two rear USB ports current capacity is 0.9 A.

3.4. PCIe adapter slot details

THE REAR VIEW OF THE POWER E1050 SERVER WITH THE LOCATION CODES FOR THE PCIE ADAPTER SLOTS

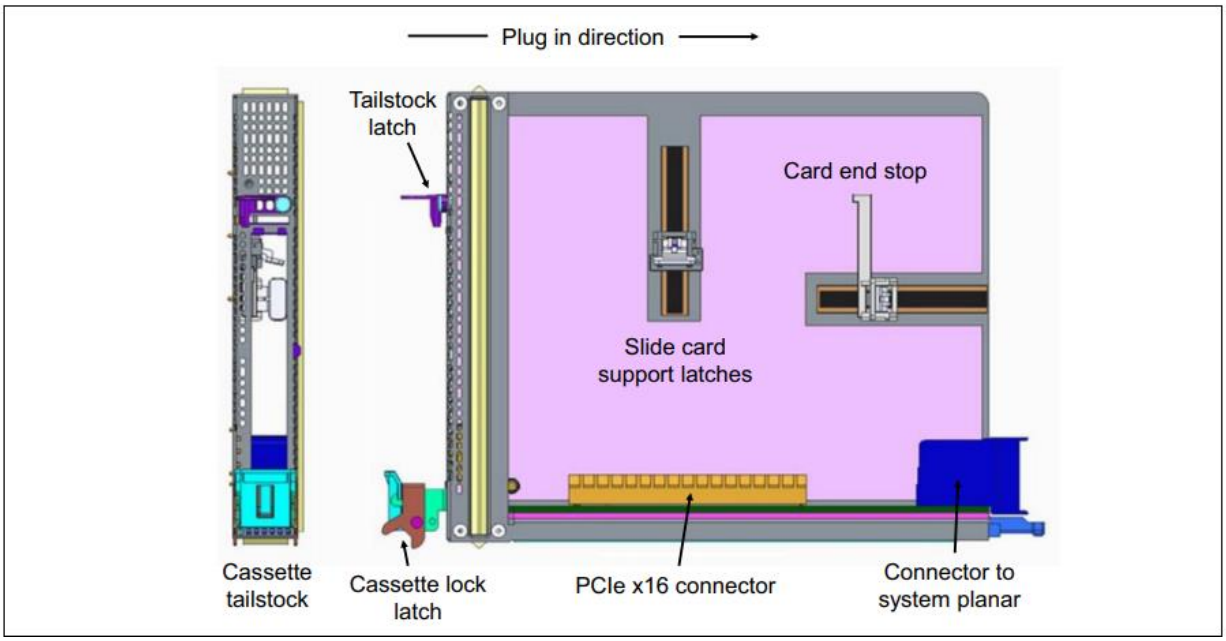


(Slot P0-C0 is not a PCIe slot; instead, it holds a special I/O Cassette for the eBMC Service Processor Card)

3.5. I/O Blind-Swap Cassettes

The Power E1050 server supports I/O BSCs for easy hot-plugging of PCIe adapters. PCIe adapters are installed inside a BSC before inserting it into the system from the rear. Each BSC has one x16 PCIe connector. There is always a BCS in each slot (C1 - C11), either with an adapter or a blank. All PCIe slots C1 - C11 are concurrently maintainable by using a BCS.

Power E1050 Blind-Swap Cassette



Non-volatile Memory Express bays

Sources: + [3D (ibm.com)]

+ [IBM Power E1050: Technical Overview and Introduction]

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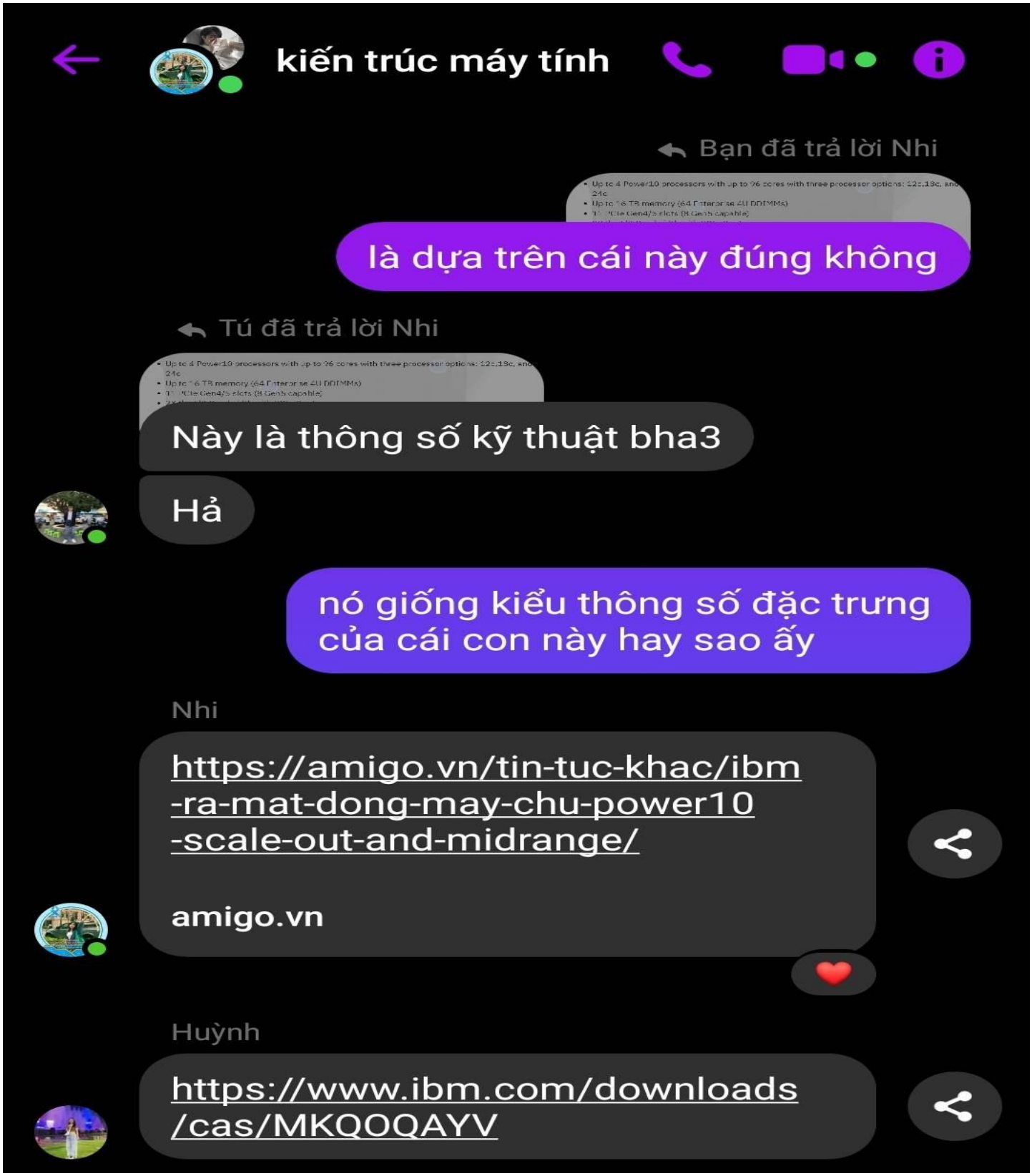
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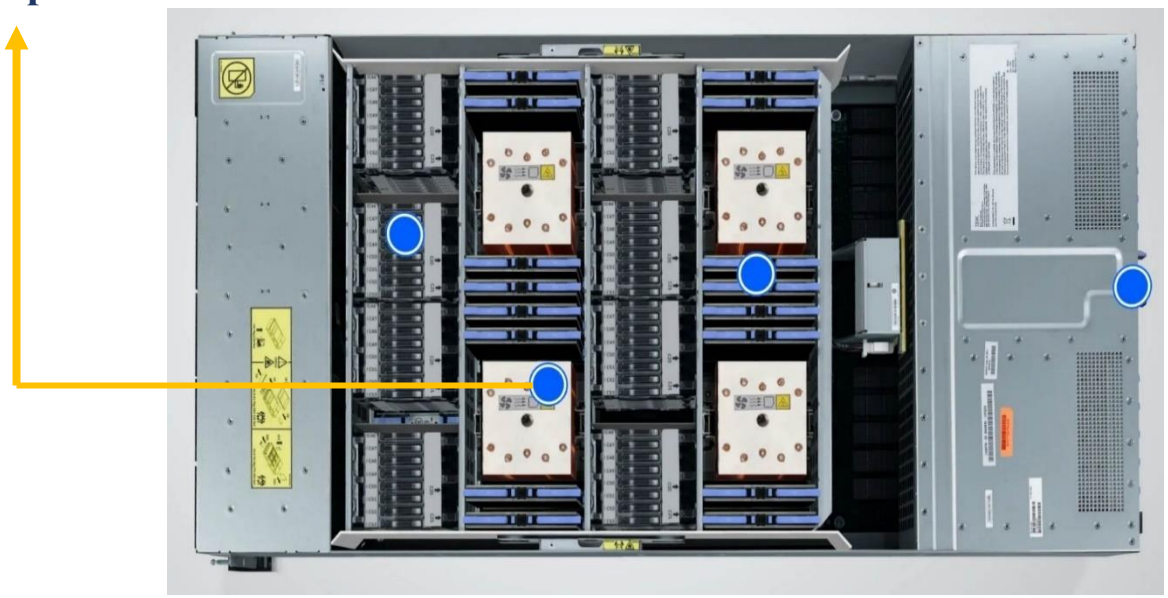
4.Reliability, fault tolerance, and data correction

The reliability of systems starts with components, devices, and subsystems that are designed to be highly reliable. During the design and development process, subsystems go through rigorous verification and integration testing processes. During system manufacturing, systems go through a thorough testing process to help ensure the highest level of product quality.

The Power10 processor-based E1050 system comes with the following RAS characteristics:

4.1 Power10 processor RAS :



Although there are many differences internally in the Power10 processor compared to the Power9 processor that relate to performance, number of cores, and other features, the general RAS philosophy for how errors are handled has remains the same. Therefore, information about Power9 processor-based subsystem RAS can still be referenced to understand the design

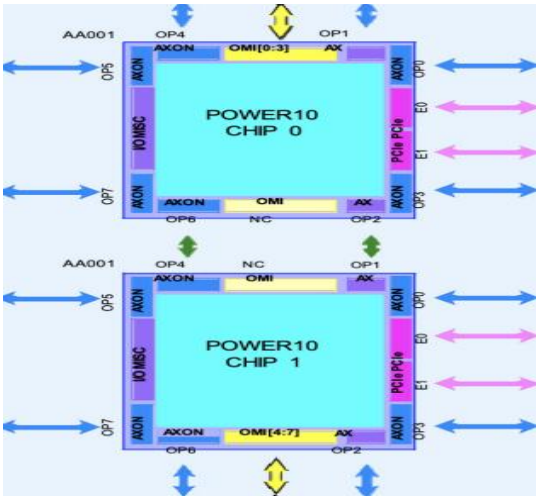
Power10 Dual Chip Module (DCM)

Available in the following options, the Power10 DCM delivers more than 2X performance per core of competitive x86 systems

- 12 cores (48 cores max) 3.36 to 4.00GHz
- 18 cores (72 cores max) 3.20 to 4.00 GHz
- 24 cores (96 cores max) 2.95 to 3.90 GHz

The Power E1050 supports 24 to 96 processor cores with two to four Power10 DCM processor modules

AI inferencing at the point of data with built in MMA, to efficiently accelerate MMA operations, the Power10 processor core implements a dense math engine (DME) microarchitecture that effectively provides an accelerator for cognitive computing, machine learning, and AI inferencing workloads



Source: https://m.kaon.com/c/ib/qm5vPQ

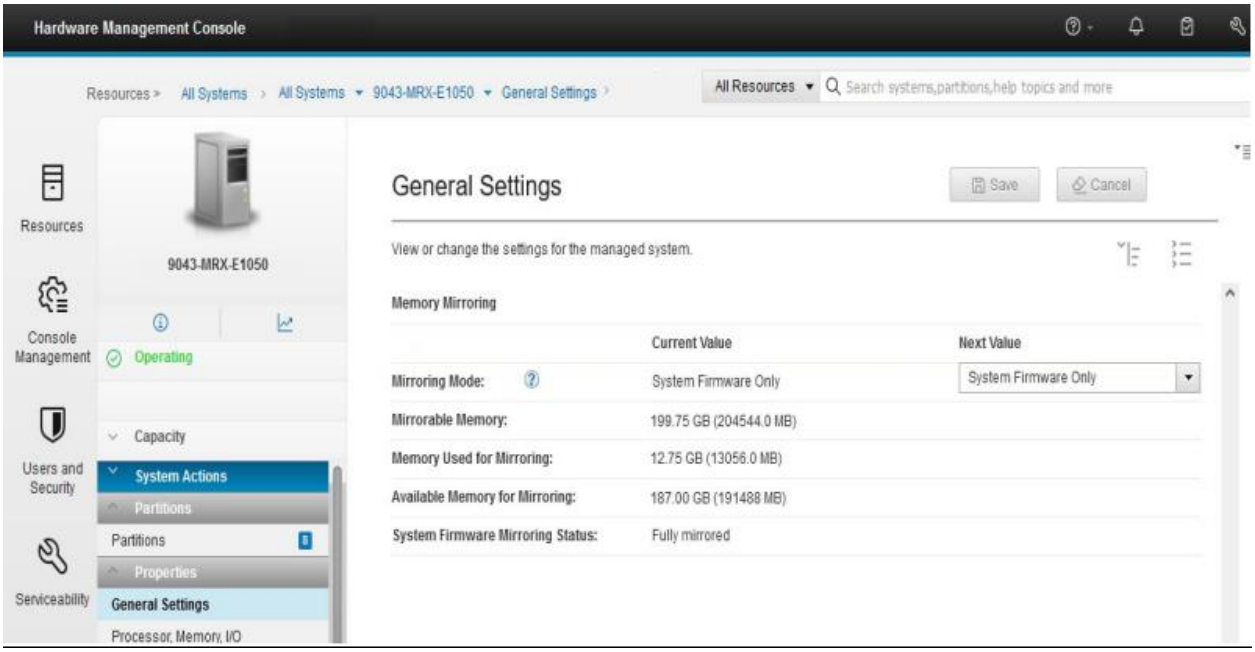
4.2 Enterprise BMC service processor for system management and service:

Processor: The IBM Power E1050 server is expected to be powered by IBM's Power10 processor. The Power10 processor is built on advanced architecture and is designed to deliver high-performance computing with improved energy efficiency.

The Power E1050 server can mirror the Power Hypervisor code across multiple memory DDIMMs. If a DDIMM that contains the hypervisor code develops an uncorrectable error, its mirrored partner enables the system to continue to operate uninterrupted. Active Memory Mirroring (AMM) is an optional feature (#EM81). The hypervisor code logical memory blocks are mirrored on distinct DDIMMs to enable more usable

memory. There is no specific DDIMM that hosts the hypervisor memory blocks, so the mirroring is done at the logical memory block level, not at the DDIMM level. To enable the AMM feature, the server must have enough free memory to accommodate the mirrored memory blocks.

Besides the hypervisor code itself, other components that are vital to the server operation are also mirrored: Hardware page tables (HPTs), which are responsible for tracking the state of the memory pages that are assigned to partitions Translation control entities (TCEs), which are responsible for providing I/O buffers for the partition's communications Memory that is used by the hypervisor to maintain partition configuration, I/O states, virtual I/O information, and partition state It is possible to check whether the AMM option is enabled and changes its status by using the HMC. The relevant information and controls are in the Memory Mirroring section of the General Settings window of the selected Power E1050 server.



After a failure occurs on one of the DDIMMs that contains hypervisor data, all the server operations remain active and the enterprise Baseboard Management Controller (eBMC) service processor isolates the failing DDIMMs. The system stays in the partially mirrored state until the failing DDIMM is replaced. Memory that is used to hold the contents of platform dumps is not mirrored, and AMM does not mirror partition data. AMM mirrors only the hypervisor code and its components to protect this data against a DDIMM failure. With AMM, uncorrectable errors in data that are owned by a partition or application are handled by the existing Sp.

4.3 Peripheral Component Interconnect adapters

This section covers the various types and functions of the PCIe adapters that are supported by the Power E1050 (9043-MRX). This list is based on the PCIe adapters that are available on the GA date of these systems, but it is subject to change as more PCIe adapters are tested and certified, or listed adapters are no longer available. The latest list of supported adapters is available at the Announcement Letter or Sales Manual page, which can be found at the IBM Offering Information website. The following sections describe the supported adapters and provide tables of orderable and supported feature numbers. The tables indicate OS support (AIX and Linux) for each of the adapters.

The Order type table column in the following subsections is defined as follows:

Initial	Denotes the orderability of a feature *only* with the purchase of a new system.
MES	Denotes the orderability of a feature *only* as part of an MES upgrade purchase for an existing system.
Both	Denotes the orderability of a feature as part of *both* new and MES upgrade purchases.
Supported	Denotes that feature is *not* orderable with a system, but is *supported*; that is, the feature can be migrated from existing systems, but cannot be ordered new.

- Redundant and hot-plug cooling
- Redundant and hot-plug power
- Redundant voltage regulators
- Lightpath enclosure and FRU LEDs
- Service and FRU labels
- Client or IBM install
- Proactive support and service -- call home
- Client or IBM service

4.4 Benefits:

- Increased uptime Electronic Service Agent is designed to enhance the warranty and maintenance service by potentially providing faster hardware error reporting and uploading system information to IBM Support. This can optimize the time monitoring the symptoms, diagnosing the error, and manually calling IBM Support to open a problem record. And 24x7 monitoring and reporting means no more dependency on human intervention or off-hours client personnel when errors are encountered in the middle of the night.