Kiến trúc máy tính – Các câu hỏi trắc nghiệm – HK1 2023-2024

1. Choose the **suitable function(s) for each component of a simple single – processor computer**:

Central processing unit (CPU): Controls the operation of the computer and performs its data processing functions.

Main memory: Stores data

I/O: Moves data between the computer and its external environment.

System interconnection: Provides for communication among CPU, main memory and I/O.

2. Which year was 80286 processor first introduced? 1982

3. Choose the siutable definintions for terms below:

Structure: the way in which the components are interrelated.

Function: the operatuion of each individual component as part of the structure.

Computer organization: refers to the optional units and their interconnections that realize the architectual specifications.

Computer architecture: refers to those attributes of a system visible to a programmer.

Instruction Set Architecture (ISA): instruction formats, intructions opcodes, registers, instruction and data memory; the effect of executes instructions on the registers and memory; and an algorithm for controlling instruction execution.

4. Which is (are) component(s) of the CPU?

A. Control unit. B. I/O **C. Arithmetic and logic unit (ALU)** D. Power supply

E. Main memory. F. Mainboard **G. Registers.** **H. CPU interconnections (internal bus)**

I. System interconnection.

5. Which year was 8086 processor first introduced? 1978

6. Which processor has the highest clock speed?

a. 8086 b. 8080 c. 8008

7. Choose the correct statement(s)

a. Computer architecture must be designed to implement a particular organizational specification. (sai vì, 1 architechture áp dụng cho nhiều thiết kế máy tính dù khác nhau nhưng vẫn theo 1 chuẩn kiến trúc)

b. In multicore computer structure, a core may be equivalent in functionality to a main memory on a single-CPU system.

c. ALU appears both in multicore computers and in simple single-processor computers

d. Computer organization must be designed to implement a particular architectural specification.

8. Choose the correct statement(s)

✓a. The first generation of computers used vacuum tubes for digital logic elements and memory.

b. The IAS computer consists of two main memories, two arithmetic and logic units and one control unit.. (sai vì IAS chỉ ó 1 ain memory

✓c. The IAS computer is one kinds of first-generation computer.

✓d. An IAS computer can perform some operations of arithmetic such as addition, subtraction, multiplication, and division.

9. Place the right orders of techniques based on the increasing components per chip

a. ULSI-> LSI-> VLSI

b. LSI -> VLSI ULSI (large < very large < ultra large scale integration)
c. VLSI -> LSI-> ULSI
d. ULSI -> VLSI -> LSI

10. Choose the suitable functions) for each component of a simple single-processor computer
Main memory: Stores data
System interconnection: Provides for communication among CPU, main memory, and I/O
Central processing unit (CPU): Controls the operation of the computer and performs its data processing functions
I/O: Moves data between the computer and its external environment.

11. Choose the suitable definitions for terms below
Computer architecture: refers to those attributes of a system visible to a programmer
Instruction Set Architecture (ISA): instruction formats, instruction opcodes, registers, instruction and data **memory:** the effect of executed instruction on the registers and memory; and an algorithm for controlling instruction execution
Function: the operation of each individual component as part of the structure.
Computer organization: refers to the operational units and their interconnections that realize the architectural specifications.
Structure: the way in which the components are interrelated.

12. Choose the right statement about **Memory Buffer Register** in US computer
a. Contains a word to be stored in memory or sent to the UD unit, or is used to receive a word from memory or from the I/O unit
b. Specifies the address in memory of the word to be written from or read into the MBR
c. Contains the address of the next instruction pair to be fetched from memory
d. Contains the bit opcode instruction being executed.

13. Choose the correct statement(s) about consequences of Moore's law
a. Because logic and memory elements are placed closer together on more densely packed chips, the electrical path length is increased, reducing operating speed. (sai vì densely packed -> các path chip sẽ ngắn là -> tăng tốc độ của chip)
b. The cost of a chip has remained virtually unchanged during this period of rapid growth in density. This means that the cost of computer logic and memory circuitry has fallen at a dramatic rate
c. There is a growth in power requirements. (chip càng phát triển -> điện năng càng giảm)
d. The computer becomes smaller, making it more convenient to place in a variety of environments.

14. Choose the wrong statement(s)
a. The control unit operates the IAS by fetching instructions from memory and executing them one at a time.
b. A word of the US computer at each storage location consists of 20 binary digits (bit). (consist 40 bits)
c. The memory of the IAS computer consists of 6904 storage locations (4096 mới đúng)
d. A word in IAS computer **may** alternatively contain two 20-bit instructions
e. The address bus connected between the main memory and CPU in the IAS computer has 12 lines.

15. Year by year the cost of computer systems continues to rise. **Sai (càng lúc càng giảm)**

16. Branch prediction potentially increases the amount of work wallable for the processor to execute. **True**

17. Choose the suitable characteristics of each techniques which are used to speed up microprocessor
Dataflow analysis: create an optimized schedule of instructions. This prevents unnecessary delay.

Branch prediction: potentially increases the amount of work available for the processor to execute

Pipelining: enables a processor to work simultaneously on multiple instructions by performing a different phase for each of the multiple instructions at the same time.

Superscalar execution: issue more than one instruction in every processor clock cycle.

18. The desktop application(s) that require the great power of today's microprocessor-based systems include …
a. all are correct
b. speech recognition
c. video conferencing
d. image processing

19. The interface between processor and … … … is the most crucial pathway in the entire computer because it is responsible for **carrying a constant flow of program instructions and data between memory chips and the processor.**
Select one:
a. clock speed
b. control unit
c. pipeline
d. main memory

20. Workstation systems **cannot** support highly sophisticated engineering and scientific applications. (false)

Workstation systems now support highly sophisticated engineering and scientific applications and have the capacity to support image and video applications. In addition, businesses are relying on increasingly powerful servers to handle transaction and database processing and to support massive client/server networks that have replaced the huge mainframe computer centers of yesteryear. As well, cloud service

21. Choose the suitable answer for each intel product li
80486: It was introduced the use of powerful cache technology and instruction pipelining.
80386: Intel's first 32-bit machine. It was the first intel processor to support multitasking.
8080: It was used in the first personal computer, the Altair.

22. A common measure of performance for a processor is the rate at which instructions are executed, expressed as millions of instructions per second (MIPS)? **True**

23. The raw speed of the microprocessor will not achieve its potential unless it is fed a constant stream of work to do in the form of computer instructions? **True**

But the raw speed of the microprocessor will not achieve its potential unless it is fed a constant stream of work to do in the form of computer instructions. Any-

24. Solution (s) for **improving the interface** between processor and main memory to **solve the performance balance problem**

a. Change the DRAM interface to make it more efficient (include cache and some buffering)

b. Reduce the frequency of memory access

c. Increase the number of bits that are retrieved at one time (make wider path to retrieve many bit at one time)

d. All are correct

e. Increase the interconnect bandwidth between processors and memory

- Increase the interconnect bandwidth between processors and memory by using higher-speed buses and a hierarchy of buses to buffer and structure data flow.
- Increase the number of bits that are retrieved at one time by making DRAMs "wider" rather than "deeper" and by using wide bus data paths.
- Change the DRAM interface to make it more efficient by including a cache[1] or other buffering scheme on the DRAM chip.
- Reduce the frequency of memory access by incorporating increasingly complex and efficient cache structures between the processor and main memory. This includes the incorporation of one or more caches on the processor chip as well as on an off-chip cache close to the processor chip.

25. The …… holds the **address of the next instruction** to be fetched.

a. Instruction Counter (IC)

b. Program Counter (PC) - hold address of next instruction

c. Accumulator (AC) - temp storage

d. Instruction Register (IR) - intruction being executed

26. Choose suitable statement for each kind of means:

HM (Harmonic Mean): is inversely proportional to the total execution time, which is the desired property. compare by rate (rate càng cao máy càng khỏe)

GM (Geometric Mean): gives equal weight to all of the values in the data set.

AM (Arithmetic Mean): is a good candidate for comparing the execution time performance of several svstems. - compare time (thời gian càng ngắn chạy càng tốt)

27. Choose the suitable statement for each line of x86 Evolution:

8086 - first 16 bit data path. instruction cache. prefetch few instructions

Pentium - Superscalar and multiple instructions executed in parallel

8080 - First general purpose microprocessor and 8 bit data path

Core 2 Quad - Four processors on chip

Core - First x86 with dual core

28. The… … … contains the data to be written into memory and receives the data read from memory.

a. memory address register

b. memory buffer register

c. I/O buffer register

d. I/O address register

(MAR), which specifies the address in memory for the next read or write, and a **memory buffer register (MBR)**, which contains the data to be written into memory or receives the data read from memory. Similarly, an I/O address register (I/OAR)

29. Choose the correct statement(s)

a. Average cycles per instruction are determined by ISA, CPU hardware

b. Average cycles per instruction are determined by CPU hardware (CPI)

c. Instruction count for a program is determined by CPU hardware, ISA and compiler

d. Instruction count for a program is determined by program, ISA and compiler

* Average cycles per instruction (CPI)

stant cycle time τ, where $\tau = 1/f$. Define the instruction count, I_c, for a program as the number of machine instructions executed for that program until it runs to completion or for some defined time interval. Note that this is the number of instruction

30. Small, fast memory located between the processor and main memory is called:

a. Direct memory

b. WORM memory

c. Cache memory

d. Block memory

Another prominent feature of contemporary computers is the use of multiple layers of memory, called *cache memory*, between the processor and main memory. Chapter 4 is devoted to the topic of cache memory. For our purposes in this section, we simply note that a cache memory is smaller and faster than main memory and is used to speed up memory access, by placing in the cache data from main memory, that is likely to be used in the near future. A greater performance improvement may

31. The unit of data exchanged between cache and main memory is

a. block size

b. cache size

c. memory size

d. map size

e. slot size

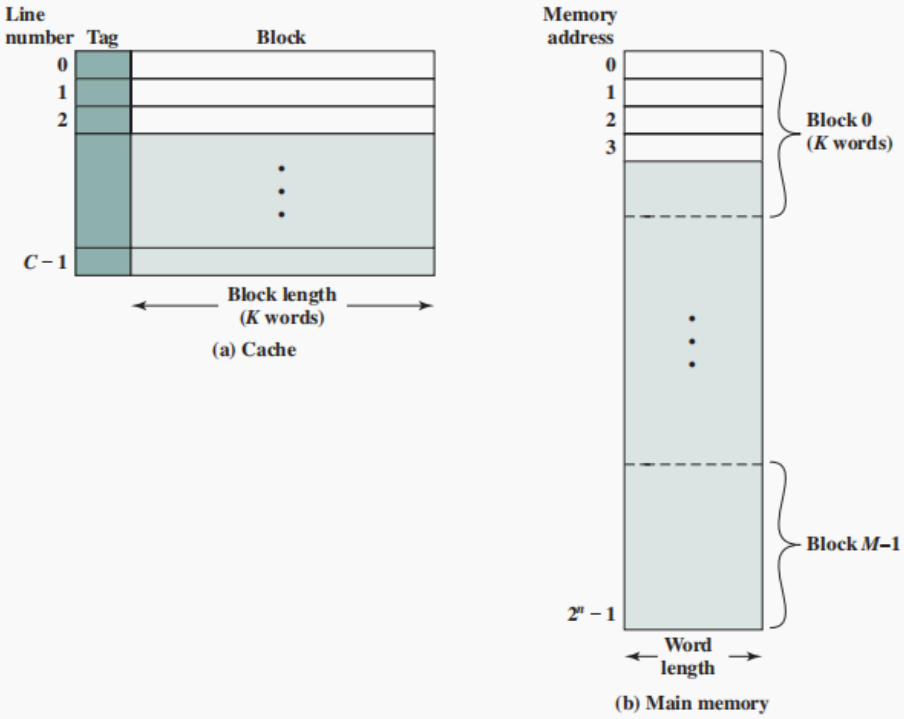


Figure 4.4 Cache/Main Memory Structure

https://sanjayjain.weebly.com/uploads/4/7/3/4/47349035/unit_1_notes.pdf

Cache Design Issues:
We will see that similar design issues must be addressed in dealing with virtual memory and disk cache design.
They fall into the following categories:
• Cache size
• Block size
• Mapping function
• Replacement algorithm
• Write policy

Size issues:
We have already dealt with the issue of cache size.
- It turns out that reasonably small caches can have a significant impact on performance.

Another size issue is that of block size:
- the unit of data exchanged between cache and main memory.

As the block size increases from very small to larger sizes, the hit ratio will at first increase because of the principle of locality:
- the high probability that data in the vicinity of a referenced word are likely to be referenced in the near future.

As the block size increases, more useful data are brought into the cache.
- The hit ratio will begin to decrease.
- However, as the block becomes even bigger and the probability of using the newly fetched data becomes less than the probability of reusing the data that have to be moved out of the cache to make room for the new block.

32. Instruction processing consists of two steps:
a. fetch and execute
b. fetch and instruction
c. instruction and halt
d. instruction and execute

the key elements of program execution. In its simplest form, instruction processing consists of two steps: The processor reads (*fetches*) instructions from memory one at a time and executes each instruction. Program execution consists of repeating the process of instruction fetch and instruction execution. The instruction execution may involve several operations and depends on the nature of the instruction (see, for example, the lower portion of Figure 2.4).

The processing required for a single instruction is called an **instruction cycle**. Using the simplified two-step description given previously, the instruction cycle is depicted in Figure 3.3. The two steps are referred to as the **fetch cycle** and the **execute cycle**. Program execution halts only if the machine is turned off, some sort of unrecoverable error occurs, or a program instruction that halts the computer is encountered.

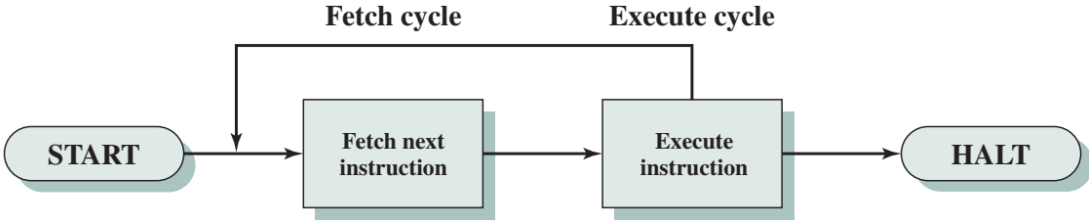


Figure 3.3 Basic Instruction Cycle

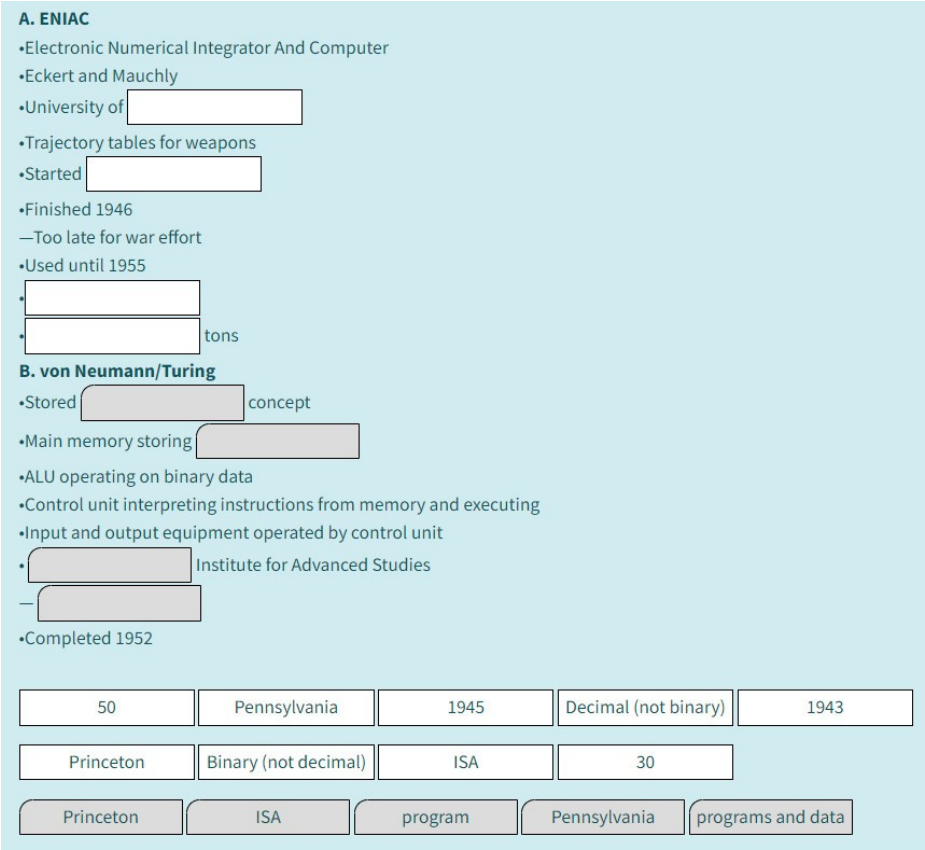
33. We can improve computer's performance by
a. All are correct
(để tăng performance thì: tăng tần số (c); giảm số chu kỳ (b); phần cứng khi thiết kế cần phải tương thích với hiệu suất, nếu không phải đánh đổi giữa clock rate và cycle)
b. Reducing number of clock cycles *(Viết lệnh tốt hơn → ít xử lý → giảm chu kỳ)*
c. Increasing clock rate *(Tăng xung nhịp → tăng số lệnh được thực thi trên 1 đơn vị thời gian)*
d. Hardware designer must often trade off clock rate against cycle count *(tăng xung nhịp → giảm chu kỳ).*

However, simply relying on increasing clock rate for increased performance runs into the power dissipation problem already referred to. The faster the clock rate, the greater the amount of power to be dissipated, and some fundamental physical limits are being reached.

Clock cycle time or clock period, is already time required per clock cycle. Question is, does the word Clock Rate makes sense? It also says, **Hardware designer must often trade off clock rate against cycle count**. But, they are inversely related. If one increases Clock speed, the clock period (time for per clock cycle) will reduce automatically.

Relation between CPU's clock speed and clock period
stackoverflow.com/questions/6570752/relation-between-cpus-clock-speed-an...

34.

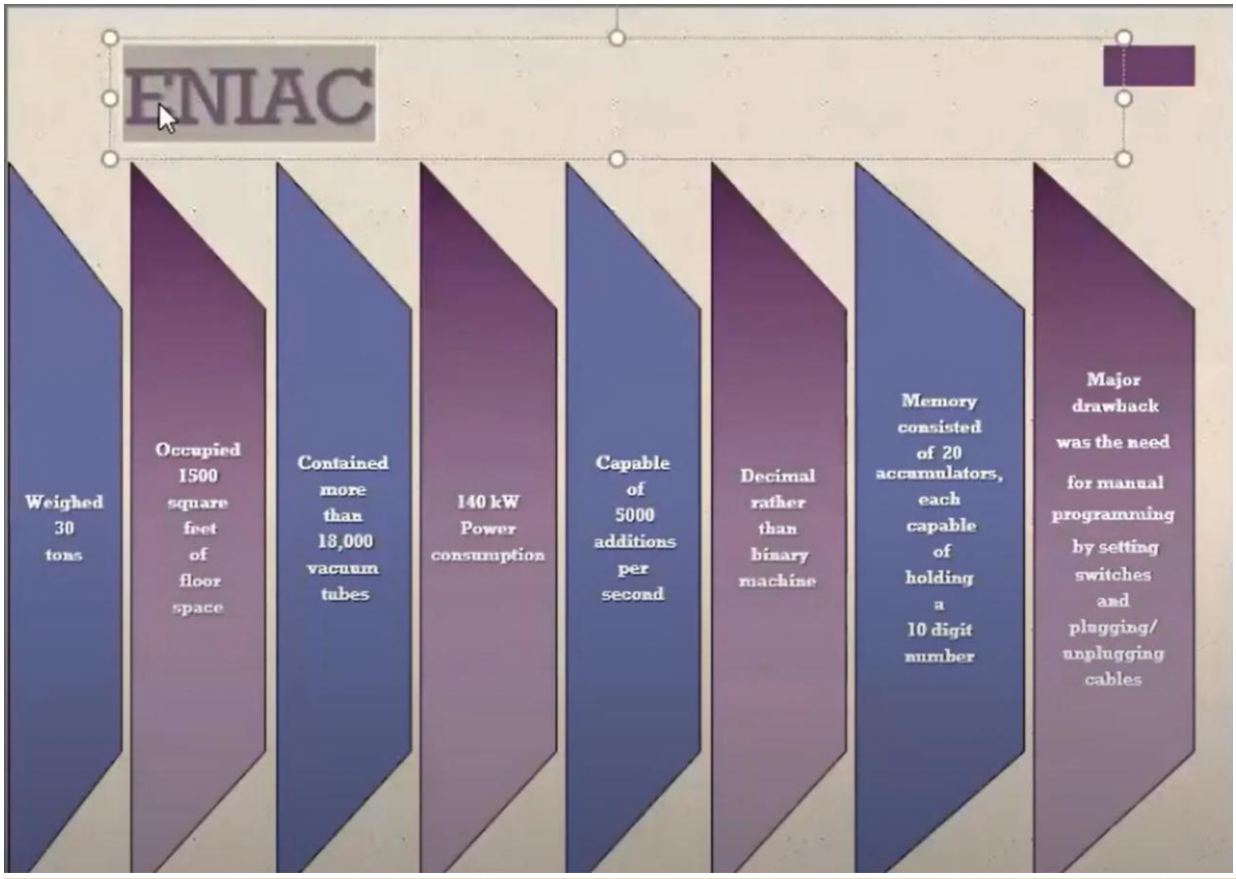


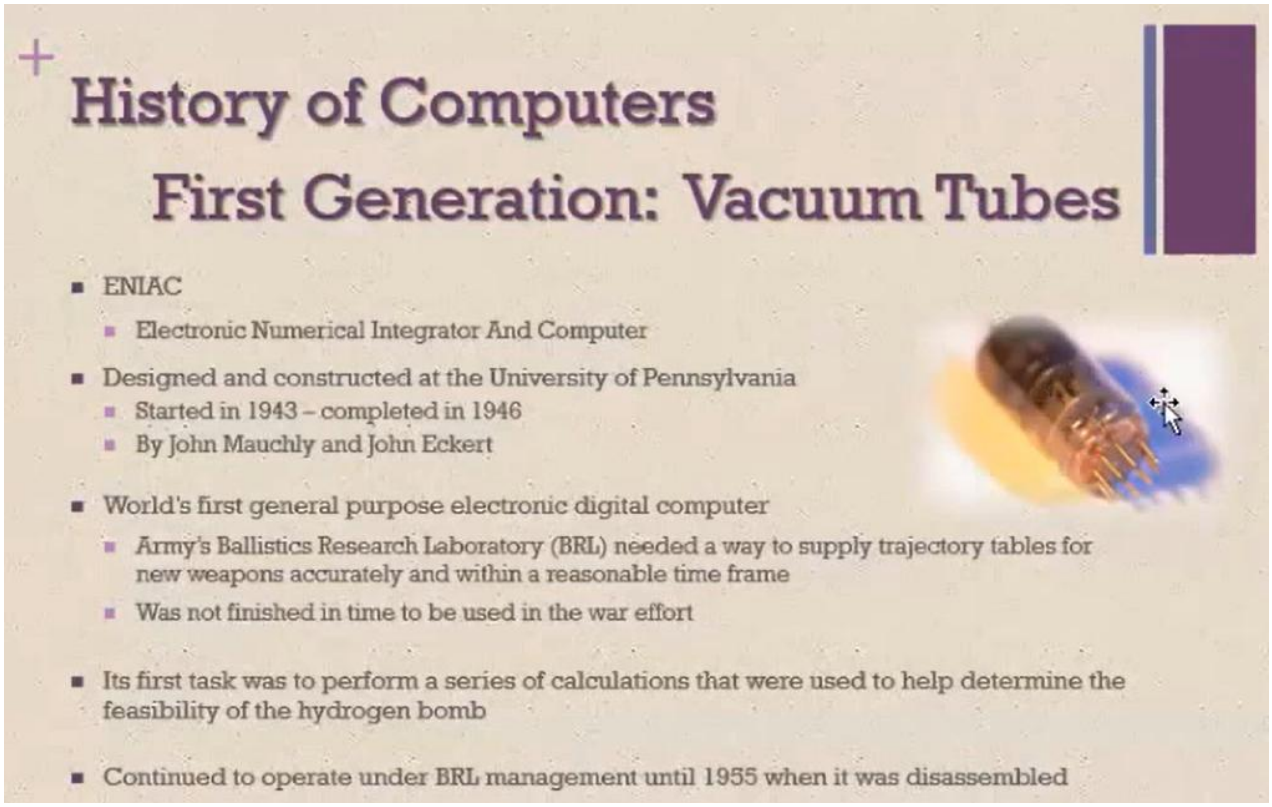
A. ENIAC
+ Electronic Numerical Integrator And Computer
+ Eckert and Mauchly
+ University of **Pennsylvania**
+ Trajectory tables for weapons
+ Started **1943**
+ Finished 1946
-Too late for war effort
+ Used until 1955
+ **Decimal (not binary)**
+ **30** tons

B. von Neumann/Turing
+ Stored **program** concept
+ Main memory storing **programs and data**
+ ALU operating on binary data

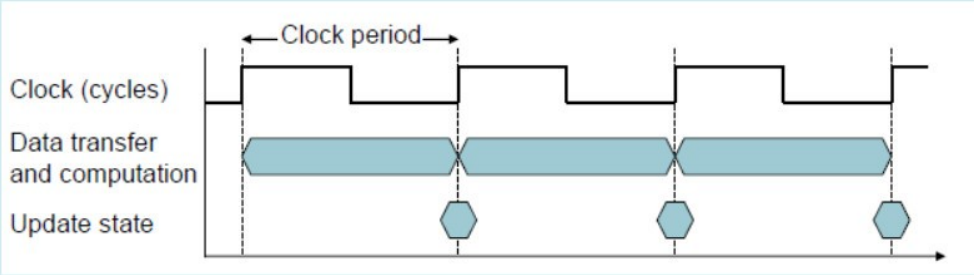
+ Control unit interpreting instructions from memory and executing
+ Input and output equipment operated by control unit
+ **Princeton** Institute for Advanced Studies
- **IAS**
+ Completed 1952

Option for A: 50; ~~Pennsylvania;~~ 1945; Decimal (not binary); ~~1943;~~ Princeton; Binary (not decimal); ISA; ~~30~~
Option for B: ~~Princeton, IAS, program, Pennsylvania, programs and data~~





35.



Clock period: duration of a clock cycle (s) - chu kì
Clock frequency (rate): **cycles per seconds** (Hz) - tần suất
Options: cycles per seconds, duration per seconds, duration of a clock cycle, cycles of a clock rate.
https://www.chegg.com/flashcards/architecture-the-processor-8acafa0c-8c5b-4dac-8413-126ec96c0c9e/deck

36. The … … routine determines the nature of the interrupt and performs whatever actions are needed.
a. interrupt handler
b. instruction signal
c. interrupt signal
d. program handler

> The processor now proceeds to the fetch cycle and fetches the first instruction in the interrupt handler program, which will service the interrupt. The interrupt handler program is generally part of the operating system. Typically, this program determines the nature of the interrupt and performs whatever actions are needed.

Want to know more about this Super Coaching ?

Types of ROM

- PROM (programmable read-only memory).
- EPROM (erasable programmable read-only memory).
- EEPROM(electrically erasable programmable ROM).
- Mask ROM.

Table 5.1 Semiconductor Memory Types

Memory Type	Category	Erasure	Write Mechanism	Volatility
Random-access memory (RAM)	Read-write memory	Electrically, byte-level	Electrically	Volatile
Read-only memory (ROM)	Read-only memory	Not possible	Masks	Nonvolatile
Programmable ROM (PROM)			Electrically	
Erasable PROM (EPROM)	Read-mostly memory	UV light, chip-level		
Electrically Erasable PROM (EEPROM)		Electrically, byte-level		
Flash memory		Electrically, block-level		

37. Which type(s) of memories that need(s) to be provided with an unchanged power supply

a. Flash memory
b. PROM
c. EEPROM
d. RAM
e. EPROM
f. ROM

DRAM and SRAM

All of the memory types that we will explore in this chapter are random access. That is, individual words of memory are directly accessed through wired-in addressing logic.

Table 5.1 lists the major types of semiconductor memory. The most common is referred to as **random-access memory (RAM)**. This is, in fact, a misuse of the term, because all of the types listed in the table are random access. One distinguishing characteristic of memory that is designated as RAM is that it is possible both to read data from the memory and to write new data into the memory easily and rapidly. Both the reading and writing are accomplished through the use of electrical signals.

The other distinguishing characteristic of traditional RAM is that it is volatile. A RAM must be provided with a constant power supply. If the power is interrupted, then the data are lost. Thus, RAM can be used only as temporary storage. The two traditional forms of RAM used in computers are DRAM and SRAM. Newer forms of RAM, discussed in Section 5.5, are nonvolatile.

38. Choose the conect statement about cache read operation: If a block is containing read address in cache, ……

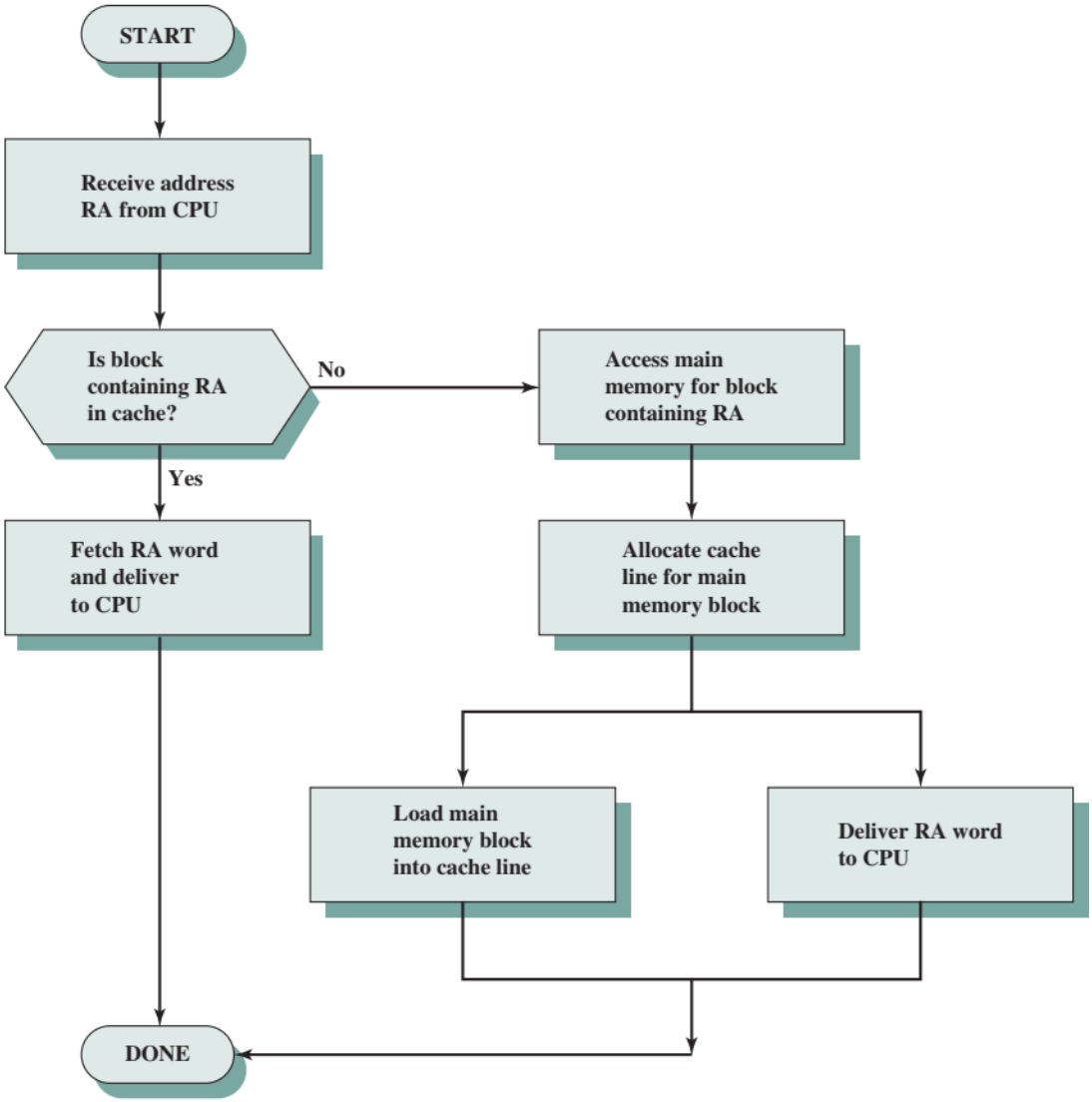


Figure 4.5 Cache Read Operation

a. the computer will allocate cache line for main memory block
b. the computer fetches this read address word and deliver to CPU
c. None is correct
d. All are correct
e. the computer accesses main memory for block containing read address

39. Choose the correct semiconductor memory type(s) tha**t can read or write**
a. PROM
b. DRAM
c. EEPROM
d. SRAM
e. EPROM
f. ROM
g. Flash memory

40. Choose the correct semiconductor memory type(s) t**hat can read only**
a. EPROM
b. EEPROM
c. SRAM
d. Flash memory
e. DRAM
f. ROM
g. PROM

41. For main memory, choose the best description for each terms below
Sequential access: Memory is organized into units of data. called records. Access must be made in a specific linear sequence.
Word: The "natural" unit of organization of memory. The size of it is typically equal to the number of bits used to represent an integer and to the instruction length.
Random access: Each addressable location in memory has a unique, physically wired- in addressing mechanism. The time to access a given location is independent of the sequence of prior accesses and is constant.
Direct access: Involves a shared read-write mechanism. Access is accomplished by this method access to reach a general vicinity plus sequential searching, counting, or waiting to reach the final location.
Unit of transfer: This is the number of bits read out of or written into memory at a time.

42. Three performance parameters are used to characterize memory:
Transfer rate: This is the rate at which data can be transferred into or out of a memory unit.

Memory cycle time: This concept is primarily applied to random-access memory and consists of the access time plus any additional time required before a second access can commerce.

Access time (latency) for random-access memory: this is the time it takes to perform a read or write operation, that is, the time from the instant that an address is presented to the instant that data have been stored or made available for use.

Access time (latency) for non-access memory: this is the time it takes to position the read-write mechanism at the desired location.

43. As one **goes down** the **memory hierarchy,** the following occur:

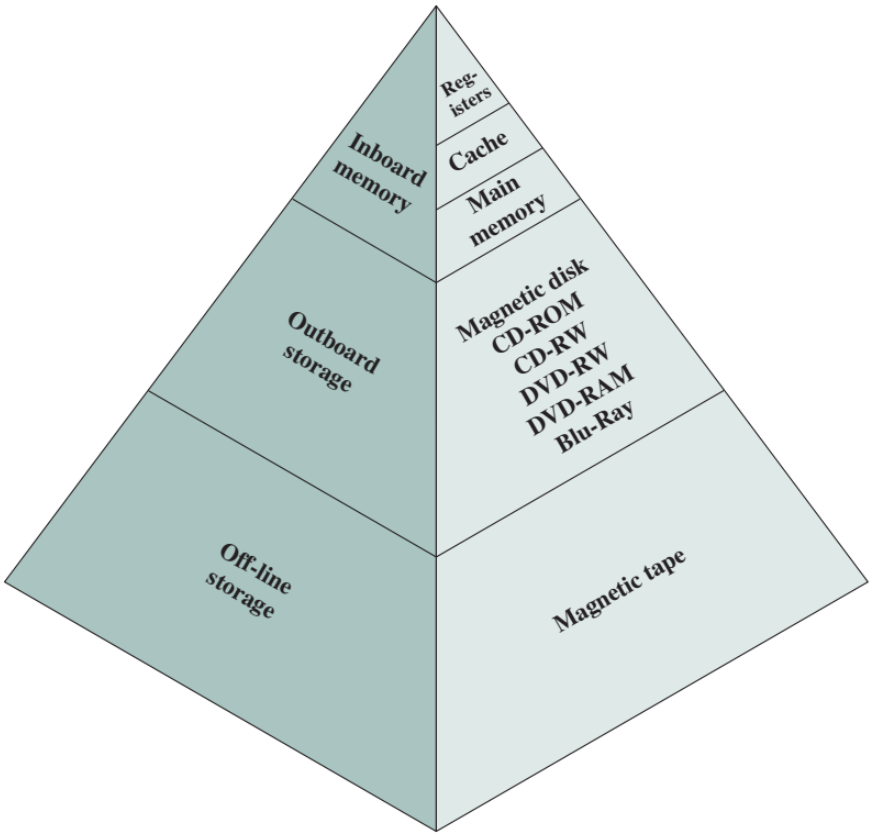


Figure 4.1 The Memory Hierarchy

a. Increasing cost per bit.
b. Increasing access time.
c. Unchanged access time.
d. Decreasing frequency of access of the memory by the processor.
e. Decreasing capacity.
f. Increasing frequency of access of the memory by the processor.
g. Increasing capacity.
h. Decreasing cost per bit.

The way out of this dilemma is not to rely on a single memory component or technology, but to employ a **memory hierarchy**. A typical hierarchy is illustrated in Figure 4.1. As one goes down the hierarchy, the following occur:

a. Decreasing cost per bit;
b. Increasing capacity;
c. Increasing access time;
d. Decreasing frequency of access of the memory by the processor.

44. Choose below listed type(s) belong(s) to **external memory type**
a. optical disks
b. tapes
c. cache
d. processor registers
e. magnetic disks
f. main memory

45. Choose the suitable statement(s) about **direct Mapping method** for mapping cache address and main memory

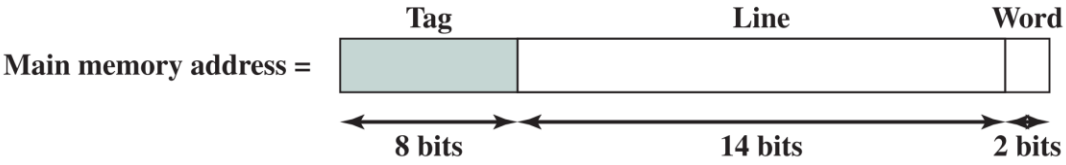


Figure 4.10 Direct Mapping Example

a. We have 2^8 cache line in a tag field
b. Main memory has in capacity 16MB if a word is 1 byte
c. All are correct
d. There are 2^8 tag fields have the same cache line

d. There are 2^8 tag fields have the same cache line (Image sent)

A direct mapping cache maps each main memory block to a specific cache line. This is done by using a tag field, which is a portion of the main memory address. The tag field is used to identify the main memory block that is stored in the cache line.

The number of tag fields in a direct mapping cache is equal to the number of cache lines. In the image you provided, there are 2^8 cache lines, so there must be 2^8 tag fields.

46. What type(s) of semiconductor memories that **can be erasable**
a. RAM
b. EPROM
C. ROM
d. PROM
e. EEPROM
f. Flash memory (flash is also a type of EEPROM)

5.4 FLASH MEMORY

Another form of semiconductor memory is flash memory. Flash memory is used both for internal memory and external memory applications. Here, we provide a technical overview and look at its use for internal memory.

First introduced in the mid-1980s, flash memory is intermediate between EPROM and EEPROM in both cost and functionality. Like EEPROM, flash memory uses an electrical erasing technology. An entire flash memory can be erased in one or a few seconds, which is much faster than EPROM. In addition, it is possible to erase just blocks of memory rather than an entire chip. Flash memory gets its name because the microchip is organized so that a section of memory cells are erased in a single action or "flash." However, flash memory does not provide byte-level erasure. Like EPROM, flash memory uses only one transistor per bit, and so achieves the high density (compared with EEPROM) of EPROM.

Flash Memory

Flash memorymay be considered as a development of EEPROM technology. Data can be written to it and it can be erased, although only in blocks, but data can be read on an individual ... See more

47. Choose below listed type(s) belong(s) to internal memory type
Select one or more:
Chưa trả lời
a. processor registers

b. main memory
c. magnetic disks
d. cache
e. optical disks

48. Choose the correct semiconductor memory type(s) that **can be read-mostly memory**
a. DRAM
b. Flash memory
c. ROM
d. SRAM
e. EPROM
f. PROM
g. EEPROM

49. SRAM versus DRAM
a. A DRAM requires the supporting refresh circuitry. (DRAM cần mạch làm "tươi" - vì truyền bằng transitor điện mức 0 1 nên khi truyền sẽ bị leak điện)
b. A SRAM requires the supporting refresh circuitry.
c. DRAMs tend to be favored for large memory requirements.
d. DRAMs are volatile and SDAMS are nonvolatile
e. A static memory cell is simpler and smaller than a dynamic memory cell.
f. SRAM is used for cache memory (both on and off chip), and DRAM is used for main memory because SRAMS are somewhat faster than DRAMs.
g. Both static and dynamic RAMs need a continuously supplied power.
h. Both static and dynamic RAMs are volatile.
i. A dynamic memory cell is simpler and smaller than a static memory cell. (mạch DRAM đơn giản hơn -> giá thành rẻ hơn SRAM)
j. SRAM is used for cache memory (both on and off chip), and DRAM is used for main memory because DRAMs are somewhat faster than SRAMS

50. Select one or more

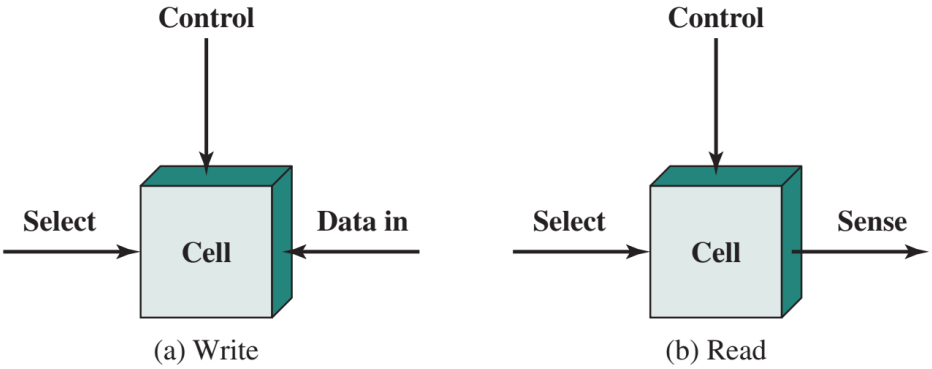
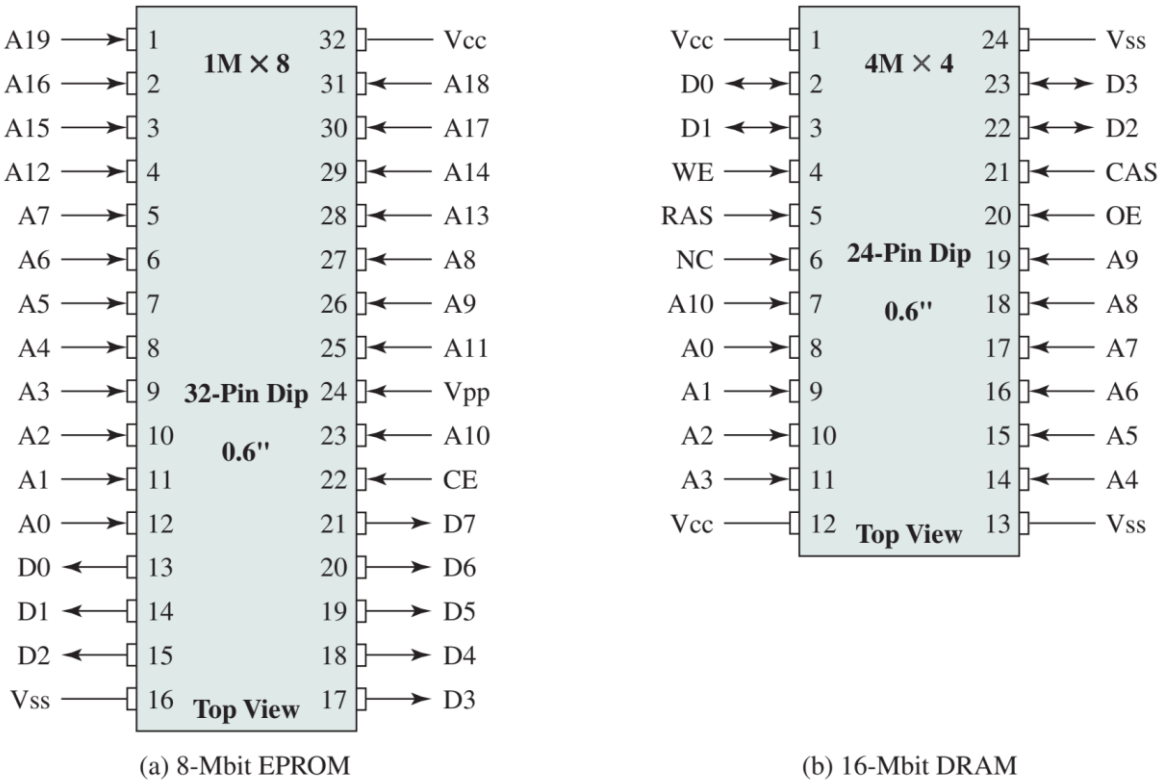


Figure 5.1 Memory Cell Operation

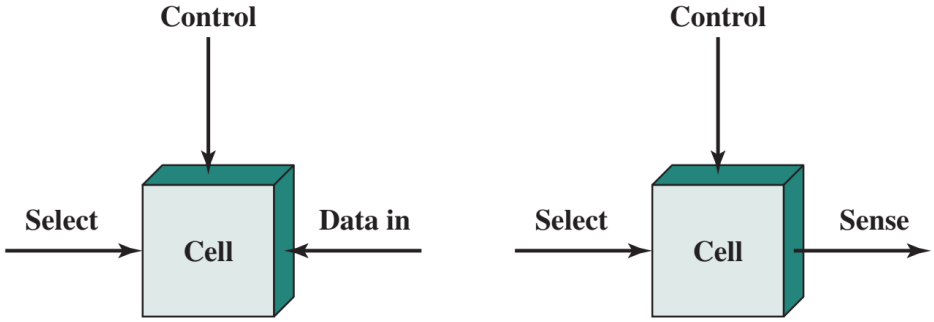


(a) 8-Mbit EPROM (b) 16-Mbit DRAM

Figure 5.4 Typical Memory Package Pins and Signals

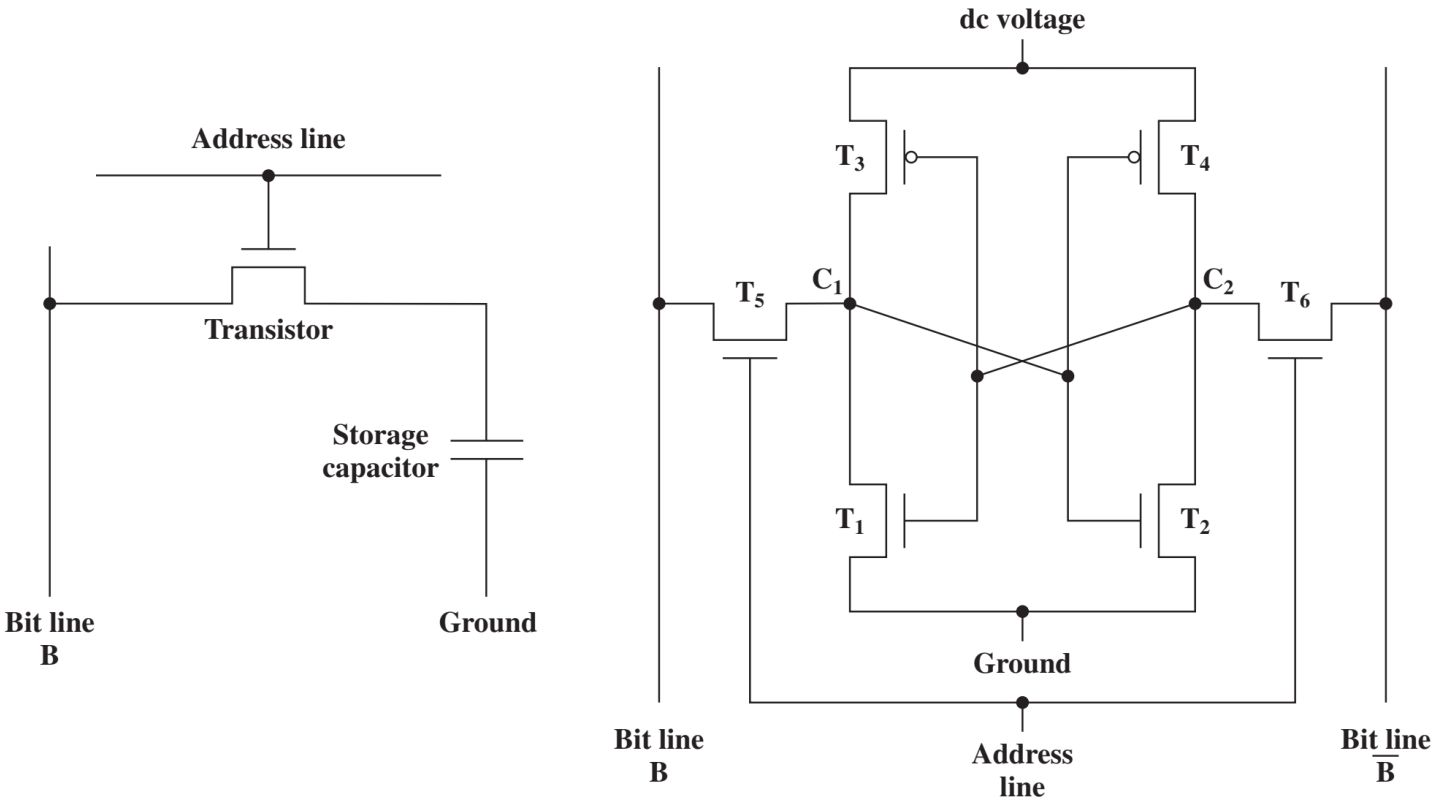
a. The data to be read out, consisting of 8 lines (Figure 5.4)
b. The data to be read out, consisting of 20 lines (Figure 5.4)
c. All are correct
d. Chip enable (CE) pin (Figure 5.4a) corresponds to Select line (Figure 5.1)

51. Matching the suitable statements



(a) Write (b) Read

Figure 5.1 Memory Cell Operation



(a) Dynamic RAM (DRAM) cell (b) Static RAM (SRAM) cell

Figure 5.2 Typical Memory Cell Structures

Type A:

In SRAM, no refresh is needed to retain data.

In SRAM, the address line (Figure 5.2b) corresponds to **the Select line (Figure 5.1)**

When a signal is applied to the Address line, the two transistors T5 and T6 are switched on, **allowing a read or write operation.**

The transistors T1, T2, T3, and T4 (Figure 5.2b) can **not be at the same state "on" or "off" at the same time.**

Options:

- allowing a read or write operation.
- be at the same state "on" or "off" at the same time.
- allowing only a write operation.
- the Control line (Figure 5.1)
- not be at the same state "on" or "off" at the same time.
- allowing only a read operation.
- we need to recharge the capacitor.
- the Select line (Figure 5.1)
- no refresh is needed to retain data.
- the Data in line or Sense line (Figure 5.1).

Type B:

The Select line (Figure 5.1) corresponds to: **the Address line (Figure 5.2).**

The Bit line (Figure 5.2) corresponds to: **the Data in line or Sense line (Figure 5.1)**

In the dynamic RAM cell, for the write operation, **a voltage signal is applied to the bit line.**

In the dynamic RAM cell, for the read operation, **the charge stored on the capacitor is fed out onto a bit line and to a sense amplifier.**

52. We can **achieve higher data rates** for DDR SDRAM by

a. A buffering scheme is used.

b. The data transfer is synchronized to both the rising and falling edge of the clock, rather than just the rising edge.

c. All are correct

d. DDR uses higher clock rate on the bus to increase the transfer rate.

DDR achieves higher data rates in three ways. First, the data transfer is synchronized to both the rising and falling edge of the clock, rather than just the rising edge. This doubles the data rate; hence the term *double data rate*. Second, DDR uses higher clock rate on the bus to increase the transfer rate. Third, a buffering scheme is used, as explained subsequently.

53. Choose the correct statement(s)

a. Special equipment is required for the writing or "programming" process for the PROM. (Pg. 170)

b. For comparable amounts of storage, the EPROM is more expensive than PROM, but it has the advantage of the multiple update capability. (Pg. 170)

c. If one bit is wrong, the whole batch of **RAMs** must be thrown out. à (ROMs) (Pg.169)

d. The **write** action by user can be done with a ROM. (ROM = **Read-only** memory)

e. There is no need for power resource required to maintain the bit values in **read-only memory**. (Pg 169 – types of ROM)

54. CLO2.1 – PI2.1 - BLOOM2

Choose the characteristic (s) of registers located within the CPU.

Select one or more:

a. The number of registers are the same in different types of computers.

b. They are used to create and store the results of CPU operations and other calculations.

c. All registers belong to a computer architecture are the same length of bits.

d. They are essentially extremely fast memory.

e. The number of registers in a particular architecture decides the instruction set design.

55. In a magnetic disk, The substrate consists of a partially shielded magnetoresistive (MR) sensor.

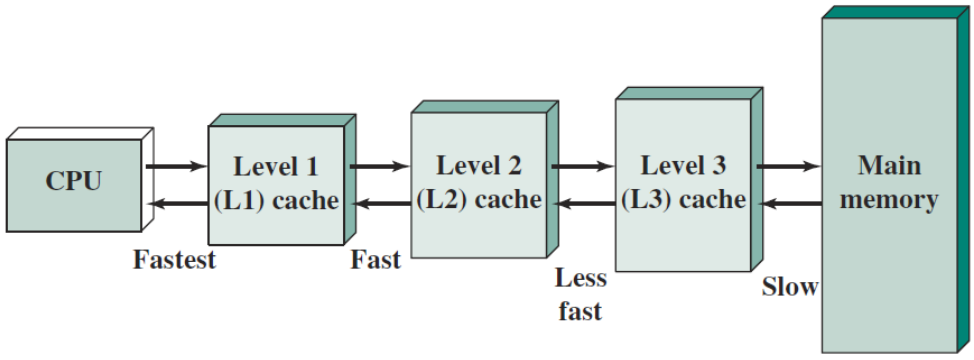
Đúng

Sai

Contemporary rigid disk systems use a different read mechanism, requiring a separate read head, positioned for convenience close to the write head. The read head consists of a partially shielded **magnetoresistive (MR)** sensor. The MR mate-

56. CLO2.1 – PI2.1 - BLOOM2

In a typical computer using three-level caches, choose the **wrong** statement about cache using:



Select one:

a. The capacity of L2 cache is larger than L3 cache.

b. Data from memory can be sent directly to the CPU. (?)

c. Data movement from L1 cache is faster than data movement from L3 cache.

d. Data can be either sent from CPU or from L1 cache.

57. CLO1.1 – PLO1 - BLOOM2

Choose correct statement about description of Bus Interconnection in a typical computer. *(AI check)*

(See 3.4 page 100) (Unchecked by book)

Select one:

a. Only one device is allowed to transmit its signal in bus system in any time period.

b. The address lines are used to transfer the data of the source.

c. A bus system consists of many data lines which are called address bus.

d. The width of the data bus determines the minimum possible memory capacity of the system.

58. CLO2.1 – PI2.1 - BLOOM2

In a typical computer, data are moved between registers or between ALU and registers by using _____.

Select one:

a. external buses

b. local buses

c. system bus

d. control bus

59. CLO1.1 – PLO1- - BLOOM2

Choose correct statement about description of von Neumann architecture.

Select one: **(See 3.1 Page 81)**

a. The contents of its memory are not addressable.

b. Data and instructions are stored in two separate memories.

c. A single read–write memory is used to store data and instructions.

d. The type of data contained its memory is use to calculate data's location.

3.1 COMPUTER COMPONENTS

As discussed in Chapter 1, virtually all contemporary computer designs are based on concepts developed by John von Neumann at the Institute for Advanced Studies, Princeton. Such a design is referred to as the *von Neumann architecture* and is based on three key concepts:

- Data and instructions are stored in a single read–write memory.
- The contents of this memory are addressable by location, without regard to the type of data contained there.

60. CLO2.1 – PI2.1 - BLOOM2

In 8086 architecture, bus width is _____ bits. (chuẩn)

Select one: **(See Table 1.3 Page 26)**

a. 4

b. 8

c. 16

d. 32

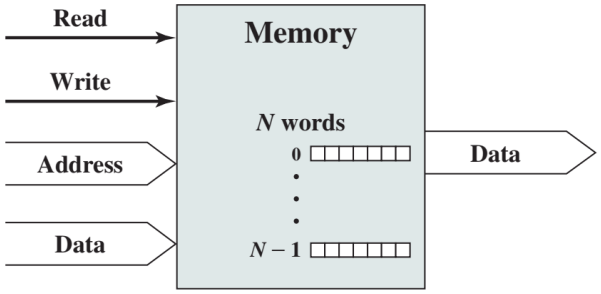
Table 1.3 Evolution of Intel Microprocessors (page 1 of 2)

(a) 1970s Processors

	4004	8008	8080	8086	8088
Introduced	1971	1972	1974	1978	1979
Clock speeds	108 kHz	108 kHz	2 MHz	5 MHz, 8 MHz, 10 MHz	5 MHz, 8 MHz
Bus width	4 bits	8 bits	8 bits	16 bits	8 bits
Number of transistors	2,300	3,500	6,000	29,000	29,000
Feature size (μm)	10	8	6	3	6
Addressable memory	640 bytes	16 KB	64 KB	1 MB	1 MB

61. CLO1.1 – PLO1 - BLOOM2

Choose correct statement about description of **Memory Module** below.



Select one: **(See Figure 3.15 Page 99)**

a. This module consist of N words in different length each.

b. Two types of control signals are Read and Write.

c. The Address bus is one type of control signals. (sai)

d. The Data bus at the input and the output of this module are different in number of bits.

- **Memory:** Typically, a memory module will consist of N words of equal length. Each word is assigned a unique numerical address $(0, 1, \ldots, N-1)$. A word of data can be read from or written into the memory. The nature of the operation is indicated by read and write control signals. The location for the operation is specified by an address.

62. CLO1.1 – PLO1 - BLOOM2

Choose correct statement about description of **instruction cycle**.

Select one:

a. The instruction contains bits that specify the data the processor is to take to perform the action.

b. The fetched instruction is loaded into a register named Instruction Register.

c. Data can only be transferred from processor to memory.

d. Data may be transferred to or from a peripheral device by transferring between the this device and memory directly.

The processing required for a single instruction is called an **instruction cycle**. Using the simplified two-step description given previously, the instruction cycle is depicted in Figure 3.3. The two steps are referred to as the **fetch cycle** and the **execute cycle**. Program execution halts only if the machine is turned off, some sort of unrecoverable error occurs, or a program instruction that halts the computer is encountered.

63. *(CLO1.1 – PLO1 - BLOOM2-2015 Null, Linda - The Essentials of computer organization and architecture)*

Choose statement that is **correct**.

Select one:

a. One DRAM cell includes more transistors than one SRAM cell. *(DRAM include more cells mới đúng)*

b. In static RAM, the number of OFF transistors when being read or written is at least four.
c. When executing programs, computer uses RAM to store lines of codes and data that the it needs.
d. Tiny capacitors that leak electricity is one type of static RAM component. *(DRAM mới đúng)*

64. The number of sectors in tracks typically are the same in tracks while using constant angular velocity
Đúng
Sai

65. CLO1.1 – PLO1 – BLOOM2
In a typical computer, system bus is used to transfer data from (A) to (B).
Select one or more:
a. (A) = registers; (B) = I/O devices
b. (A) = registers; (B) = memory (ĐÁP ÁN ĐÚNG)
c. (A) = registers; (B) = registers
d. (A) = I/O devices; (B) = registers (SAI VÌ IO CHỈ NHẬN TỪ CPU)
e. (A) = memory; (B) = registers (ĐÚNG)

66. In a magnetic disk, data are recorded on and later retrieved from the disk via a conducting coil named the head; in many systems, there are two heads, a read head and a write head. During a read or write operation, the **platter** is stationary while the head rotates above it.
Đúng
Sai **(là the head)**

Magnetic Read and Write Mechanisms

Data are recorded on and later retrieved from the disk via a conducting coil named the **head**; in many systems, there are two heads, a read head and a write head. During a read or write operation, the head is stationary while the platter rotates beneath it.

67. The organization of data on the platter in a concentric set of rings, called tracks.
Đúng
Sai

68. CLO1.1 – PLO1- - BLOOM2
In a typical computer, choose the best statement about types of memory.
Select one:
a. Memory type used in cell phones, digital cameras, solid-state disk drives and music players is mainly flash memory.
b. Flash memory provides byte-level erasure. *(provides BLOCK-LEVEL erasure)*
c. Flash memory uses two transistors per bit. *(flass has only 1 transitor)*
d. EEPROM is faster than than flash memory in *reading* data. *(erasing data chứ không phải reading)*

Memory Type	Category	Erasure	Write Mechanism	Volatility
Random-access memory (RAM)	Read-write memory	Electrically, byte-level	Electrically	Volatile
Read-only memory (ROM)	Read-only memory	Not possible	Masks	Nonvolatile
Programmable ROM (PROM)			Electrically	
Erasable PROM (EPROM)	Read-mostly memory	UV light, chip-level		
Electrically Erasable PROM (EEPROM)		Electrically, byte-level		
Flash memory		Electrically, block-level		

5.4 FLASH MEMORY

Another form of semiconductor memory is flash memory. Flash memory is used both for internal memory and external memory applications. Here, we provide a technical overview and look at its use for internal memory.

First introduced in the mid-1980s, flash memory is intermediate between EPROM and EEPROM in both cost and functionality. Like EEPROM, flash memory uses an electrical erasing technology. An entire flash memory can be erased in one or a few seconds, which is much faster than EPROM. In addition, it is possible to erase just blocks of memory rather than an entire chip. Flash memory gets its name because the microchip is organized so that a section of memory cells are erased in a single action or "flash." However, flash memory does not provide byte-level erasure. Like EPROM, flash memory uses only one transistor per bit, and so achieves the high density (compared with EEPROM) of EPROM.

69. CLO2.1 – PI2.1 - BLOOM2

A typical CPU has major components which are ____. (HINTS: choose 3).

Select one or more:

a. Register Set

b. Arithmetic Logic Unit (ALU)

c. Memory System

d. Control Unit (CU)

70. CLO2.1 – PI2.1 - BLOOM2

In 8086 architecture, memory space is defined the locations that are addressable. This memory space is _____.

Select one:

a. 32 MB

b. 8 MB

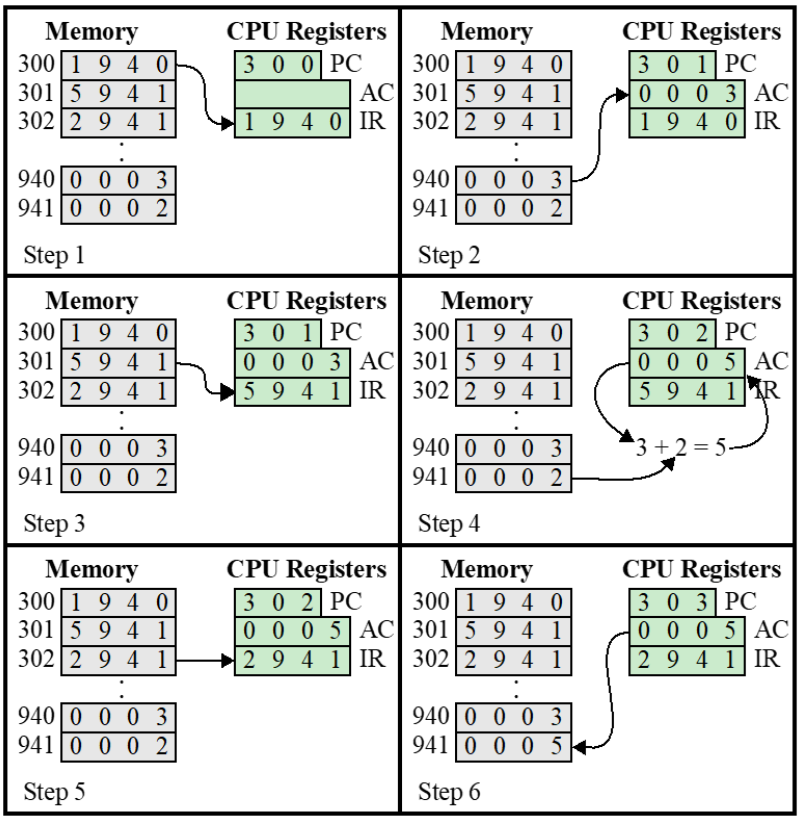
c. 16 MB

d. 1 MB

- **80286:** This extension of the 8086 enabled addressing a 16-MB memory instead of just 1 MB.

71. CLO1.1 – PLO1 - BLOOM2

Choose correct statement about description of **Program Execution** of a Hypothetical Machine.



Select one:

a. Steps 1, 3, 5 belong to fetch cycle whereas steps 2, 4, and 6 belong to execute cycle.

b. The result after executing 6 steps is an subtraction of two locations: 300 and 301.

c. The data located at the address 940 is changed after step 4.

d. The content of IR is unchanged from step 1 to step 6.

72. Each track in a platter has a larger width than the head.

Hãy chọn một:

Đúng

Sai (vì **same head chứ không phải larger head)**

Data Organization and Formatting

The head is a relatively small device capable of reading from or writing to a portion of the platter rotating beneath it. This gives rise to the organization of data on the platter in a concentric set of rings, called **tracks**. Each track is the same width as the head. There are thousands of tracks per surface.

73. CLO1.1 – PLO1 – BLOOM2

Choose correct statement about description of **instruction cycle**.

Select one:

a. At the beginning of each instruction cycle, the processor fetches an data from memory. (fetch opcode to to IR and address to memory)

b. The content of Program Counter always increases two units after each instruction fetch so that it will fetch the next instruction in sequence. (PC chỉ tăng 1)

c. One instruction cycle consists of two consecutive steps: executive cycle and fetch cycle.

d. In a typical processor, a register called the Instruction Register (IR) holds the address of the instruction to be fetched next. (IR hold the opcode – next intruction, chứ không phải là "hold address").

- **Instruction register (IR):** Contains the 8-bit opcode instruction being executed.

The IAS operates by repetitively performing an *instruction cycle*, as shown in Figure 1.8. Each instruction cycle consists of two subcycles. During the *fetch cycle*, the opcode of the next instruction is loaded into the IR and the address portion is loaded into the MAR. This instruction may be taken from the IBR, or it can be obtained from memory by loading a word into the MBR, and then down to the IBR, IR, and MAR.

Why the indirection? These operations are controlled by electronic circuitry and result in the use of data paths. To simplify the electronics, there is only one register that is used to specify the address in memory for a read or write and only one register used for the source or destination.

Once the opcode is in the IR, the *execute cycle* is performed. Control circuitry interprets the opcode and executes the instruction by sending out the appropriate control signals to cause data to be moved or an operation to be performed by the ALU.

CODE EMU 8086 (ANSWER IS GIVEN BY TEACHER)

74. Given assembly code: SUB 100,CX. ***Examine*** the type of the source operand's addressing mode.
Select one:
a. Implied addressing mode
b. Direct addressing mode
c. Immediate addressing mode
d. This code is invalid

75. **Determine** the addressing mode of the source operand in this line of code:
ADD AX,CX
Select one:
a. Register indirect
b. Immediate
c. Register
d. Memory

76. Choose the incorrect statement

```
MOV REG, memory
MOV memory, REG
MOV REG, REG
MOV memory, immediate
MOV REG, immediate
MOV memory, memory
```

Select one:
a. The "Immediate" can have the values of w5, -24, 3Fh, or 10001101b.
b. The command MOV memory, memory makes two memory locations have the same value.
c. The operands can be formatted as [BX], [BX+SI+7], and variable.
d. After executing the command Move REG, memory, the content of the REG is the same as the content of the memory whose address is "memory".

77. Choose the correct statement

```
include 'emu8086.inc'

ORG 100h
MOV AL, 2
CMP AL, 3
JNE  label1
PRINT 'AL = 3.'
JMP exit
label1:
PRINT 'Al <> 3.'
exit:
RET
```

Select one:

a. Both flags CF and ZF are zero after running the program.

b. The command PRINT 'AL = 3.' is never executed.

c. All are correct

d. The command JMP is never executed.

78. All instructions below can **make change of** all of the flags: CF, ZF, SF, OF, PF, AF

Select one:

a. CMP, TEST, SHR, SHL

b. TEST, OR, AAA, MUL

c. ADD, SUB, CMP, AND

d. JC, CMP, ADD, DIV

79. All instructions below can **make change of _____**: **AAA, MUL, CMP**

Select one:

a. Carry Flag (CF) and Zero Flag (ZF)

b. Overflow Flag (OF) and Interrupt enable Flag (IF)

c. Carry Flag (CF) and Auxiliary Flag (AF)

d. Sign Flag (SF) and Parity Flag (PF)

80. **Elicit** the result after running the line of code with AL=8Ah and CL=2 : **SHR AL,CL**

Select one:

a. AL=22h; CL=2

b. AL=8h; CL=2

c. AL=42h; CL=2

d. AL=10h; CL=2

81. We call an address formed with 2 registers *effective address*. By default, the DS segment register **works with _____** registers.

Select one:

a. SS and SI

b. BX and SI

c. DI and SP

d. SI and BP

CLO2.1 – PI2.1 - BLOOM2

82. In 8086 architecture, the instruction to copy operand2 to operand1 is _____

Select one:

a. **MOVSW** operand1, operand2

b. **MOVE** operand1, operand2
c. **MOVSB** operand1, operand2
d. MOV operand1, operand2

83. CPU makes a calculation of physical address by multiplying the segment register ___(1) by __(2)___ and adding general purpose register ___(3)___ to it .
Select one:
a. (1) DX; (2) 100; (3) DI
b. (1) SS; (2) 10; (3) SP
c. (1) DS; (2) 10 h; (3) SI
d. (1) CS; (2) 100 h; (3) SS

84. Choose the **right statement about the results** of the program below

```
05 org 100h
06
07 MOV AL, var11
08 MOV BX, var2
09
10 RET
11
12 VAR1 DB 7
13 var2 DW 1234h
```

Select one:
a. We get an error message for line 12.
b. The content of AL register is 7h.
c. The content of BX equals to the content of var2.
d. We get an error message for line 07.

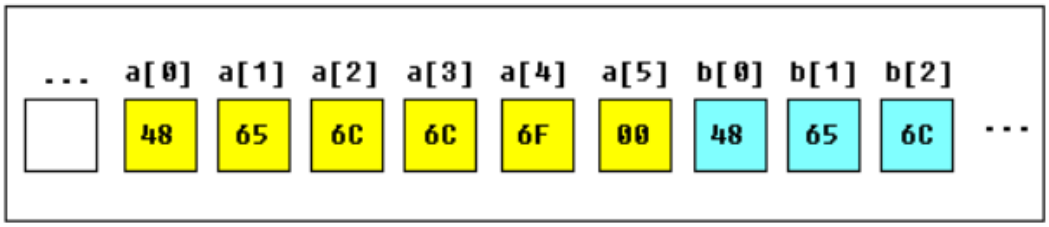
85. The **common characteristic** of segment registers (CS, DS, ES, SS) in x8086 is _____
Select one:
a. They all point at segment where variables are defined.
b. They all point at the segment containing the current program.
c. They all point at the segment containing the stack.
d. They all have a very special purpose - pointing at accessible blocks of memory.

86. Choose the right statement about the program below

```
include 'emu8086.inc'

    ORG 100h

     mov ah, 1
     int 21h

    RET
```

Select one:
a. The AL is always changed its content whenever a pressed ASCII code is entered by a user.
b. The AL is updated by the ASCII code entered by pressing a **key**, and the screen show only the visible character located in AL.
c. The AL is updated by the ASCII code entered by pressing a **key**, and the screen show this character located in AL.
d. The AL is updated by the ASCII code entered by pressing a **key**, and the screen does not show this character .

87. The chart below **shows a part of the memory** where the arrays named **a** and **b** are declared as: _____



Select one:

a. **a** DB 48, 65, 6C, 6C, 6F, 00h
b DB 'Hello', 0

b. **a** DB 48, 65, 6C, 6C, 6F, 00
b DB 'Hello', 0

c. **a** DB 48h, 65h, 6Ch, 6Ch, 6Fh, 00h
b DB 'Hello', 0

d. a DB 48h, 65h, 6Ch, 6Ch, 6Fh, 00h
b DB 'Hel', 0

88. After **compiling and executing** these line of codes with the input values AX=1000H; BX=2000H; CX=3000H, determine the value of the registers.

```
PUSH AX
PUSH BX
PUSH CX
POP AX
POP BX
POP CX
```

Select one:

a. AX=3000H; BX=1000H; CX=2000H

b. AX=2000H; BX=3000H; CX=1000H

c. AX=3000H; BX=2000H; CX=1000H

d. AX=1000H; BX=2000H; CX=3000H

89. Choose the **right statement about the results** of the program below

```
ORG 100h        ;
MOV AX, 0B800h  ;
MOV DS, AX      ;.
MOV CL, 'A'     ;.
MOV CH, 1101_1111b ;.
MOV BX, 15Eh    ;.
MOV [BX], CX    ;
RET             ;.
```

Select one:

a. Set CL to ASCII code of 'a'

b. Copy contents of DX to memory at 015E:B800

c. Copy contents of CX to memory at B800:015E

d. Set AH to hexadecimal value of 8Bh

90. Choose the right **statement about characteristic** of registers in x8086

Select one:

a. The the accumulator register AX is an eight-bit register.

b. When we modify any of the 8 bit registers which belong to general purpose registers (AX, BX, CX, DX) 16-bit register is also updated correspondingly, and vice-versa.

c. Because registers are located inside the CPU, they are much slower than memory.
d. Accessing data in a register located inside the CPU usually takes no time because this task always need the use of a system bus.

91. Choose correct statement about the result of line of codes:
mov ah,01b
int 21h
Select one:
a. Input a string.
b. Input a character.
c. Output a string.
d. Output a character.

92. Elicit the result after running all the assembly codes below.

```
mov ax, VALUE
mov bx, ax
shl ax, 2
add ax, bx
shl bx, 3
sub ax, bx
```

Select one:
a. AX=(-4)*VALUE
b. AX=(-5)*VALUE
c. AX=(-3)*VALUE
d. AX=(-2)*VALUE

93. The ____ register in x8086 **functions as** the PC (Program Counter) register in IAS computer architecture.
Select one:
a. SP - the stack pointer
b. IP - the instruction pointer
c. AX - the accummulator register
d. Si - the source index register

94. Choose the right statement about code lines below

```
include 'emu8086.inc'

ORG 100h
MOV CX, 5
label1:
PRINTN 'loop!'
LOOP label1
RET
```

Select one:
a. All are correct.
b. The address of the label "lable1" is called at least one time.
c. The phrase "loop!" appears 5 times.
d. The phrases "loop!" are in separate lines.

95. Choose the replacement instructions for code line number 2 below

```
ORG 100h            ; this directive required for a simple 1 segment .com program.
MOV AX, 0B800h      ; set AX to hexadecimal value of B800h.
MOV DS, AX          ; copy value of AX to DS.
MOV CL, 'A'         ; set CL to ASCII code of 'A', it is 41h.
MOV CH, 1101_1111b  ; set CH to binary value.
MOV BX, 15Eh        ; set BX to 15Eh.
MOV [BX], CX        ; copy contents of CX to memory at B800:015E
RET                 ; returns to operating system.
```

Select one:

a.
```
MOV AH, B8H
MOV AL, 0
```

b.
```
MOV AH, 0B8H
MOV AL, 00H
```
chia làm đôi vì AX gồm AH và

c.
```
MOV AX, B800h
```

d.
```
MOV AL, 0o
MOV AH, B8H
```

general purpose registers

8086 CPU has 8 general purpose registers, each register has its own name:

- **AX** - the accumulator register (divided into **AH / AL**).
- **BX** - the base address register (divided into **BH / BL**).
- **CX** - the count register (divided into **CH / CL**).
- **DX** - the data register (divided into **DH / DL**).
- **SI** - source index register.
- **DI** - destination index register.
- **BP** - base pointer.
- **SP** - stack pointer.

Despite the name of a register, it's the programmer who determines the usage for each general purpose register. The main purpose of a register is to keep a number (variable). The size of the above registers is 16 bit, it's something like: **0011000000111001b** (in binary form), or **12345** in decimal (human) form.

4 general purpose registers (AX, BX, CX, DX) are made of two separate 8 bit registers, for example if AX= **0011000000111001b**, then AH=**00110000b** and AL=**00111001b**. Therefore, when you modify any of the 8 bit registers 16 bit register is also updated, and vice-versa. The same is for other 3 registers, "H" is for high and "L" is for low part.

96.

```
include 'emu8086.inc'

ORG 100h
MOV AL, 2
CMP AL, 3
JNE  label1
PRINT 'AL = 3.'
JMP exit
label1:
PRINT 'Al <> 3.'
exit:
RET
```

a. The command JMP is never executed.

b. All are correct. **MOV** operand1, operand2

c. The command PRINT 'AL = 3.' is never executed.

d. Both flags CF and ZF are zero after running the program.

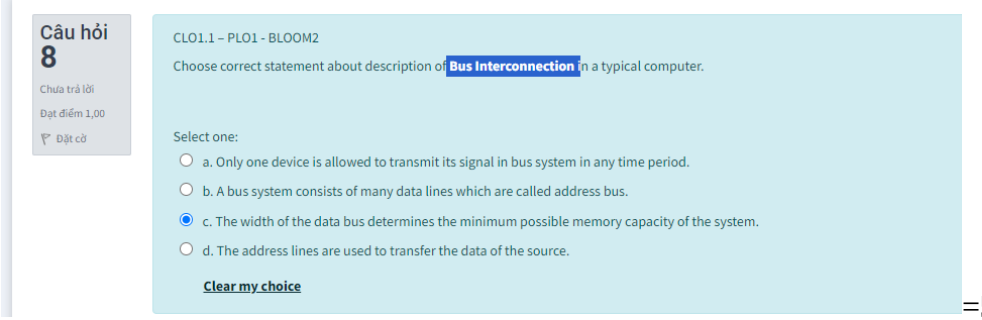
TEST (unchecked)

97. A computer has one cache that can hold 64 kB with each line contains 4 byte binary data. This computer also has one main memory consists of 16 MB. Determine the fields Tag, Line, Word if this computer uses direct mapping method.

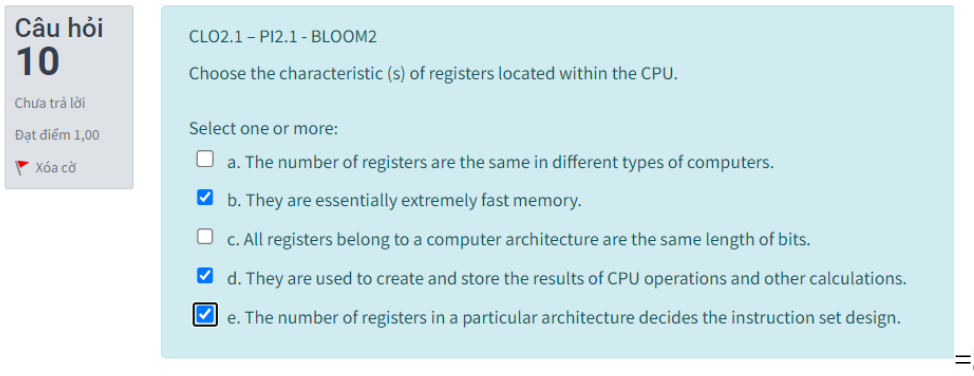
a. 8,14,2

b. 8,12,4
c. 10,8,6
d. 10,6,2

98. Identify which is not a function of CONTROL UNIT inside a CPU:
Select one:
a. It increases the value stored the PROGRAM COUNTER to turn this value to become the address of the next instruction to be fetched.
b. It gives out control signals to fetch the instructions.
c. It transfers data from REGISTERS to MEMORY.
d. It directly receives instructions from MEMORY and stores these instructions in the INSTRUCTION REGISTER (IR).



=57



=54

99. The aluminum or aluminum alloy material substrate has a number of benefits than the glass substrate, including the following:
Select one:
a. all are correct
b. reduce read-write errors
c. increase disk reliability
d. have greater ability to withstand shock and damage
e. have lower fly heights
f. reduce disk dynamics
g. none is correct

100. In 8086 architecture, assume that the CF flag is set to one.

After running the lines of code below, what are the content of AL and CF?

```
MOV AL, 3Ch        ;
ROL AL, 1          ;
RET
```

a. AL = 87, CF = 0
b. AL = 78, CF = 0
c. AL = 78, CF = 1 (GPT)
d. AL = 87, CF = 1