TRƯỜNG ĐẠI HỌC GIAO THÔNG VẬN TẢI TP. HỒ CHÍ MINH

VIỆN ĐÀO TẠO CHẤT LƯỢNG CAO

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UTH UNIVERSITY OF TRANSPORT HOCHIMINH CITY
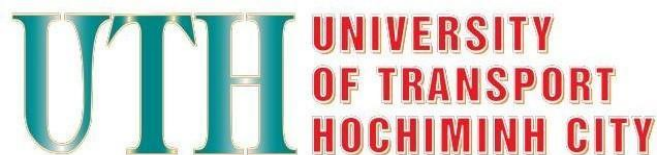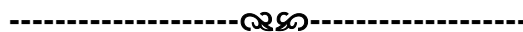
BÁO CÁO BÀI TẬP LỚN

ĐỀ TÀI: TỔNG QUAN VỀ BỘ VI XỬ LÝ IBM z15 T02

Ngành: **CÔNG NGHỆ THÔNG TIN**

Chuyên ngành: **CÔNG NGHỆ THÔNG TIN**

Học phần: **KIẾN TRÚC MÁY TÍNH**

Giảng viên: TS. Trần Thiên Thanh

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TP. Hồ Chí Minh – 2023

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CHAPTER 1: OVERVIEW OF IBM z15 T02

Businesses of all sizes are transforming for digital and shifting to cloud so they need to move critical workloads to the cloud and integrate core operations with engagement systems.

IBM Z servers are designed to help enable cloud native development and deployment, achieve encryption everywhere, and provide cyber resiliency to ensure isolation of workloads at scale to protect from threats while ensuring continuous availability of services.

Figure 1. Outside of IBM z15 T02

Some features of IBM z15 T02:

1. Air-cooled, single frame design

The z15 T02 delivers an agile cloud platform that can be the base for transforming your applications and infrastructure. It makes it easy for administrators, developers, and architects to deliver and deploy cloud native applications, with no special skills required. The z15 T02 can protect data and simplify compliance with its highly resilient, secure platform.

The z15 T02 is housed in a single 19-inch frame, designed with redundant power, cooling, and line cords. It also has the option of single or three phase power to

accommodate data center requirements. These factors can help reduce power costs, reduce footprint cost, and install in virtually any existing data center helping facility standardization.

2. Differentiated value at the core

The z15 T02 twelve core processor chip leverages the density and efficiency of 14 nm siliconon-insulator technology to deliver a new 98 Processor Capacity Index (PCI) entry point and 156 capacity options available for a wide range of workloads.

The system offers up to 16 TB of Redundant Array of Independent Memory (RAIM)

The Integrated Accelerator for Z Sort, standard on IBM z15, can help optimize elapsed time for eligible sort workloads, which typically occur during customer batch windows.

3. Cloud native development

The Integrated Accelerator for Z Sort, standard on IBM z15, can help optimize elapsed time for eligible sort workloads, which typically occur during customer batch windows.

4. Transforming with agility

IBM Z can help transform your mission-critical applications for multicloud environments, using DevOps principles across the entire application development cycle, without sacrificing stability, security, or agility.

5. Encryption everywhere

It allows business to defend and protect critical assets with encryption, without compromising transactional throughput or response times. With pervasive encryption adopted, the z15 has a goal of protection of data beyond the platform

6. Cyber resilience

The z15 T02 provides resiliency and continuous service availability across your hybrid multicloud platform and provides protection from both internal and external cyber attacks.

7. Fast and secure access to data

Protect, optimize, and manage data can slow down an organization and make it difficult to take advantage of the power of the data. High-speed connectivity to data is critical to achieve exceptional transaction throughput.

Some of the highlights:

- Optimization of cost, density, and flexibility all within a 19" frame
- Designed for integration with IBM storage for a complete cloud solution
- Encryption everywhere, wherever it resides in your ecosystem
- Simplify development with open standard tools
- Reduce the impact of downtime with instant recovery
- Aligns with z/OS and Linux on IBM Z co-located workloads

Configuaration of IBM z15 T02 single frame:

- Maximum numbers of engines: 65
- Maximum numbers of drawers: 2
- Maximum numbers of IO drawers: 3
- Numbers of frames: 1
- Co-locate with storage/switch:
- Frequency: 4.6 GHz
- Maximum memory: 16 TB
- Sizes: 4, 13, 21, 31 and 65

CHAPTER 2: IBM z15 T02 COMPONENTS

1. Doors

Inside the door is the 19-inch air-cooled single frame model of the IBM® z15™ family, which is an ideal choice for any Z client, as well as service providers and cloud providers, seeking powerful, secured computing along with environmental efficiencies.

Rated at ASHRAE Class A3, along with intelligent power distribution unit (iPDU)-based design, the z15 single frame can help you lower energy costs while delivering high reliability.

Figure 2: Door and inside the doors

2. Processor Drawer
2.1. Overview of Processor Drawer

2 CPC drawers

Figure 3: Processor Drawer

It supports processors, memory and I/O connectivity. There can be one or two drawers providing up to 65 customer configurable cores.

The z15 T02 supports up to 6 central processors (CPs) and offers up to 156 capacity settings, allowing for very granular capacity purchase options with room for future growth.

Up to 8 TB of Redundant Array of Independent Memory (RAIM) are orderable per CPC drawer and up to 16 TB total per IBM z15 T02, dependent on the configuration. RAIM provides extremely robust memory error detection and recovery. The z15 supports up to 4 PCIe+ I/O Drawers with up to 4 PCIe+ Fanouts.

It can hold up to two CPC drawers, each of them contains the following elements:

- ✓ **SCMs:** 1 - 4 PU SCMs, each containing 7 - 11 PU cores (air-cooled); One Storage Controller (SC) SCM, with a total of 960 MB L4 cache.
- ✓ **Memory:** A minimum of 64 GB and a maximum of 16224 TB of memory is available for use; Up to 20 dual inline memory modules (DIMMs) are plugged in a CPC drawer (32 GB, 64 GB, 128 GB, 256 GB, or 512 GB).

- ✓ **Fanouts:** up to 12 PCIe+ fanout adapters to connect to the PCIe+ I/O drawers, and Integrated Coupling Adapter Short Reach (ICA SR) coupling links:

  – Two-port PCIe 16 gigabytes per second (GBps) I/O fanout, each port supports one domain in the 16-slot PCIe+ I/O drawers.

  – ICA SR1.1 and ICA SR PCIe fanouts for coupling links (two links, 8 GBps each).

- ✓ Two to four Power Supply Units (PSUs), depending on the configuration, which provide power to the CPC drawer and are accessible from the rear. Loss of one PSU leaves enough power to satisfy the power requirements of the entire drawer. The PSUs can be concurrently maintained.

- ✓ Two dual-function Flexible Support Processor (FSP) oscillator cards (OSCs), which provide redundant interfaces to the internal management network and clock synchronization to the Z CPCs.

- ✓ Five fans are installed at the front of the drawer to provide cooling airflow for the resources that are installed in the drawer except for the PU SCMs, which are water-cooled.

- ✓ **Max4, Max13, Max21, and Max31:**

  – One to four PU single chip modules, each containing 7 - 11 active processor unit cores (air-cooled). The processor unit cores run at 4.5 GHz each.

  – One System Controller single chip module, with a total of 672 MB L4 cache. Max65 has four PU SCMs (7 - 11 active cores each) and one SC SCM per CPC drawer, air cooled

  – z15 T02 Max31 also supports concurrent drawer add while z15 T02 Max65 supports concurrent drawer repair.
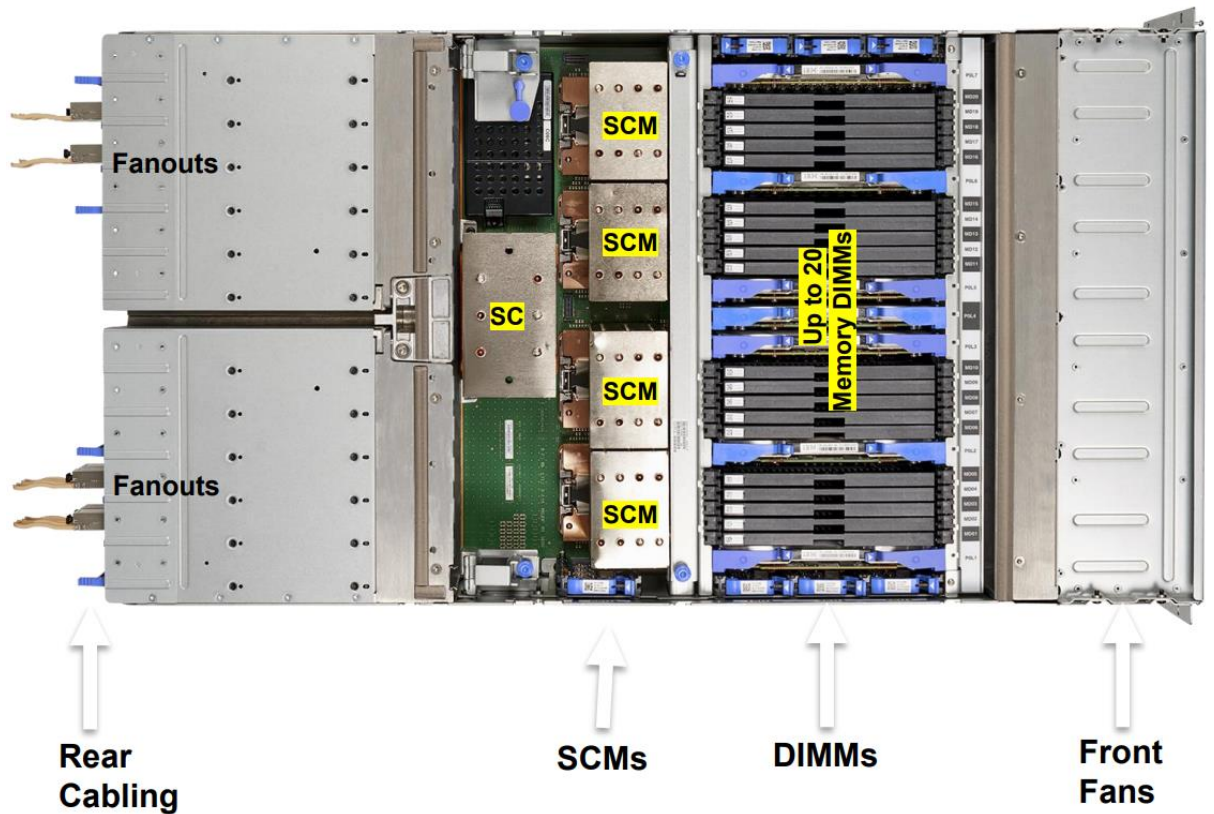
Figure 4: Components of CPC Drawer

All CPC drawers are interconnected with high-speed communications links (A-Bus) through the SC chip L4 shared caches. Symmetric multiprocessor (SMP) cables are used to interconnect the CPC drawers. The X-Bus provides connectivity between PUs within the logical clusters and the SC on the drawer.
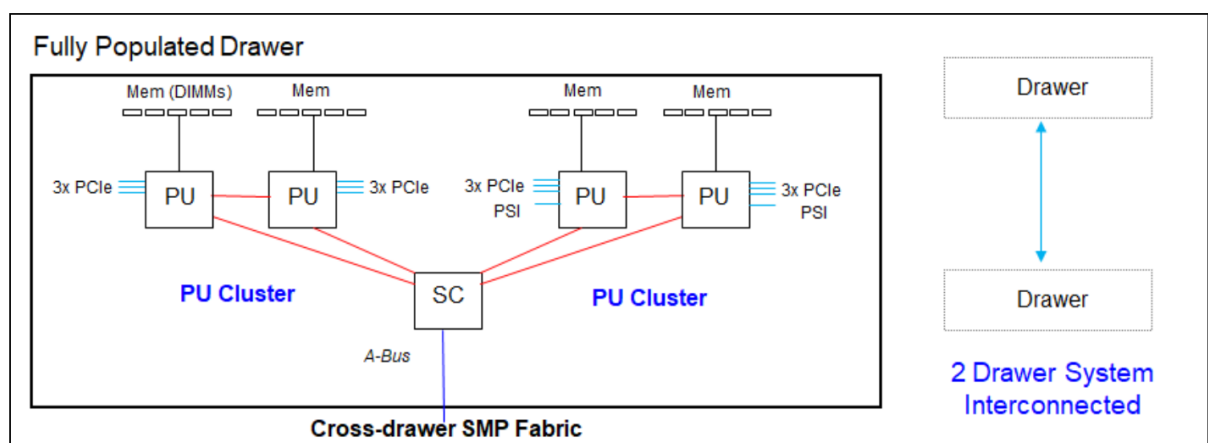
Figure 5: z15 T02 CPC drawer communication topology

The design that is used to connect the PU and storage control allows the system to be operated and controlled by the IBM Processor Resource/Systems Manager (PR/SM) facility as a memory-coherent SMP system.

Technology of z15 T02:

- **Processor**: uses a twelve-core processor chip that leverages the density and efficiency of 14 nm silicon-on-insulator technology. It delivers a new 98 Processor Capacity Index (PCI) entry point and 156 capacity options available for a wide range of workloads.

- **Design**: The z15 T02 is housed in a single 19-inch frame, designed with redundant power, cooling, and line cords. It also has the option of single or three-phase power to accommodate data center requirements.

- **I/O Drawers**: The I/O drawers can handle 16 I/O Cards and 2 Switch cards. If your work is I/O-bound, you have the option of including up to four I/O drawers.

- **Encryption**: is designed for encryption everywhere, wherever it resides in your ecosystem.

- **Instant Recovery**: reduces the impact of downtime.

- **Cloud Integration**: integration with IBM storage for a complete cloud solution.

- **Open Standard Tools**: simplifies development with open standard tools.

2.2. Processor Single-Chip Module (SCM)

- *Cores:* The SCM has 12 cores. These cores can be used for up to 65 cores for business workloads in a maximum configuration in a two-CPC drawer system.
- *Transistors:* The SCM has a whopping 9.2 billion transistors on a 14 nm chip surface.

- *Coprocessor:* A coprocessor on the chip module is responsible for compression and encryption.
- *Frequency:* The SCM operates at 4.5 GHz.
- *Interfaces:* The SCM has 3 PCle Gen4 interfaces.
- *Memory:* The SCM supports up to 40 LPARs and up to 16TB of memory.
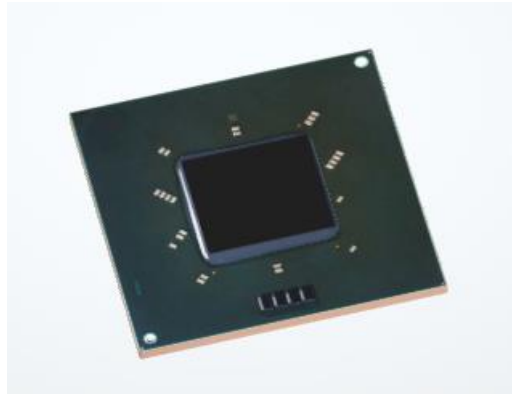
Figure 6: Processor Single-Chip Module

A single CPC drawer system has one to four PU SCMs and one SC SCM. Each PU SCM supports up to 11 active PU cores, and L1, L2, and L3 caches. The SC SCM includes 960 MB shared eDRAM cache, interface logic to the four PU SCMs, and SMP fabric logic. The SC SCM is configured to provide L4 cache that is shared by all PU cores in the CPC drawer.

Dependent on configuration, there are up to 4 Processor Chips (CPs) with 7-11 cores (processor units) per chip. Each CP has implemented one compression accelerator unit that has been designed to reduce storage requirements and costs, as well as boost data throughput without adversely impacting response times. For example, the On-Chip Sort Acceleration pre-integrated with IBM z15, helps to reduce CPU usage and improve elapsed time for eligible sort workloads.

The processor features Max4, Max13, Max21, and Max31 have one CPC drawer with up to 38 active PUs per CPC drawer. The high-capacity feature (Max65) has two processor (CPC) drawers with 38 PUs per drawer.

2.3. PCIe+ Fanout

The PCIe+ Fanout resides in the CPC drawer. It is part of the system's I/O infrastructure, provides the physical connection points for I/O devices. The design of the PCIe+ Fanout allows for efficient use of space within the system frame, be compatible with a range of I/O devices, providing flexibility for system configuration; be energy-efficient, contributing to the overall power efficiency of the system.

The z15 T02 supports the PCIe-based infrastructure for the PCIe+ I/O drawers. The PCIe I/O infrastructure consists of the Dual Port PCIe fanouts in the CPC drawers that support 16 GBps connectivity to the PCIe+ I/O drawer.

Feature name	PU SCMs	Max. PCIe fanouts	Max. PCIe+ I/O drawers
Max4 (FC 0649)	1	3	3
Max13 (FC 0650)	2	6[a]	4
Max24 (FC 0651)	3	9[a]	4
Max30 (FC 0652)	4	12[a]	4
Max65 (FC 0653)	8	24	3[b]

Table 1: z15 T02 fanouts per feature

Ordering of I/O features: Ordering I/O feature types determines the appropriate number of PCIe+ I/O drawers. Older PCIe I/O drawers are not supported on z15 T02.
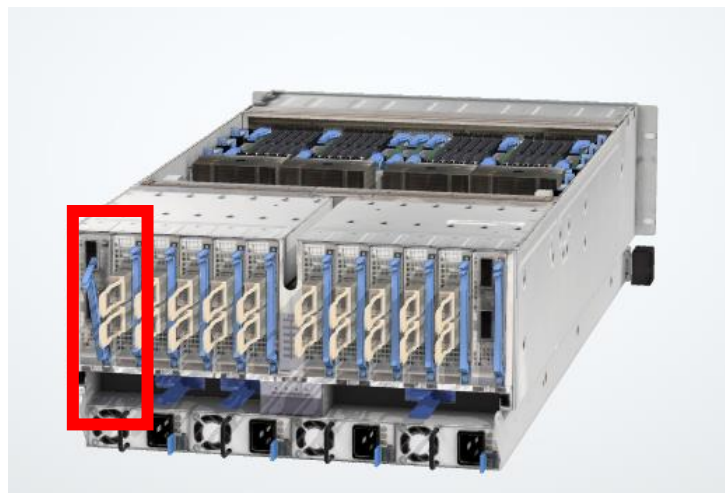
Figure 7: Loacation of PCIe+ Fanout in the Processor Drawer
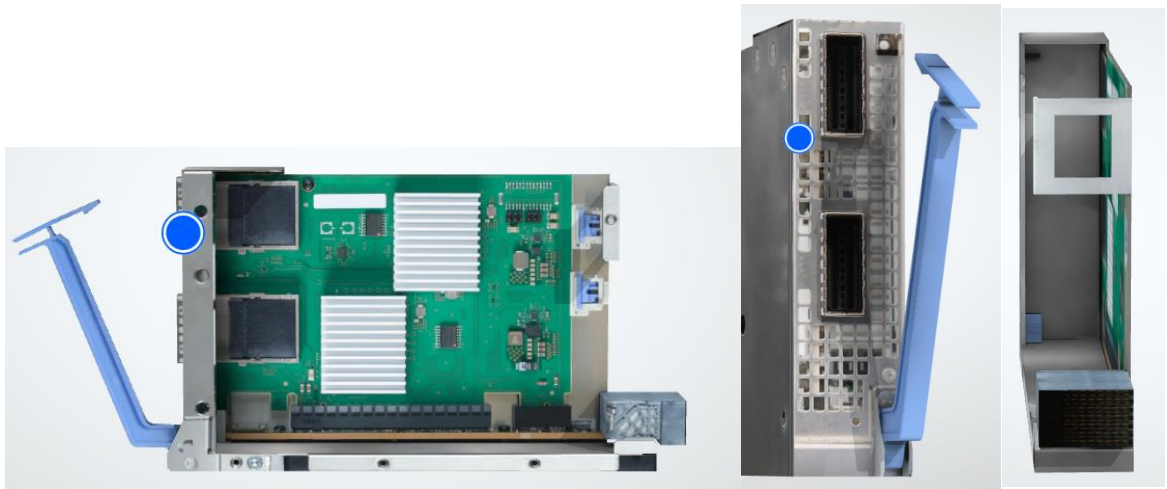
Figure 8: PCIe+ Fanout and its sides
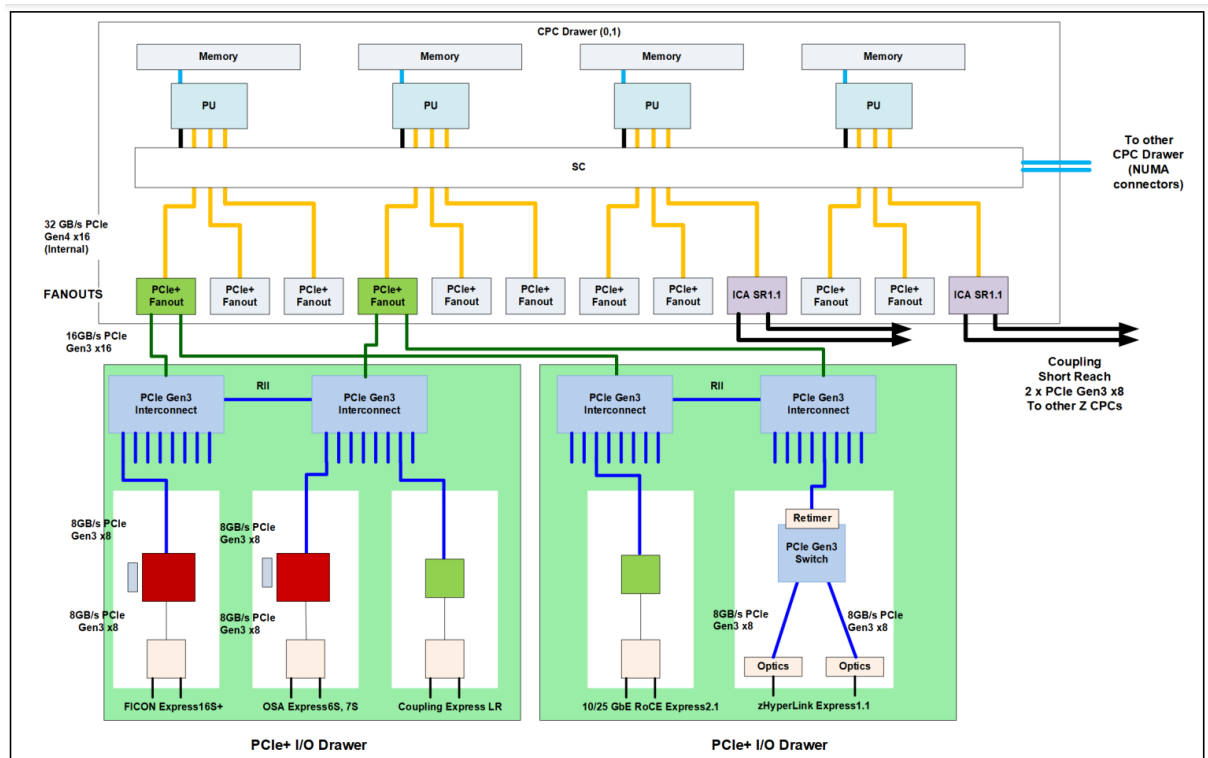
Figure 9: A high-level view of the I/O system structure for the z15 T02

The z15 T02 CPC drawer has 12 fanouts (numbered LG01 - LG12), which can be one of the following types:

- ✓ Dual-port PCIe+ fanouts for PCIe+ I/O drawer connectivity
- ✓ ICA SR fanouts for coupling
- ✓ Filler plates to assist with airflow cooling
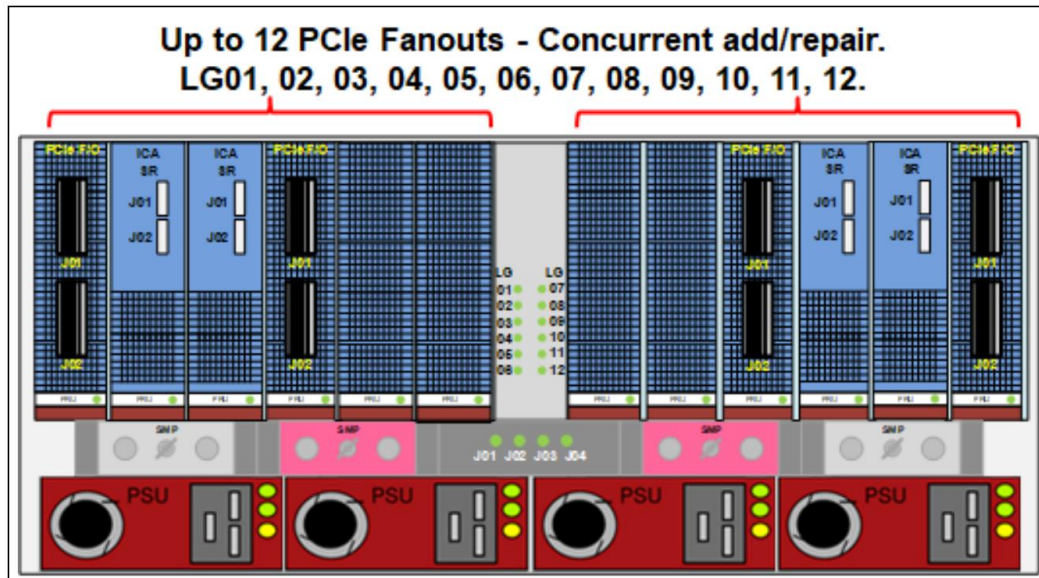
Figure 10: z15 T02 CPC drawer, rear view

For coupling link connectivity (Parallel Sysplex and Server Time Protocol (STP) configuration), the z15 T02 supports the following link types:

- ✓ ICA SR1.1 and ICA SR (installed in a CPC drawer)
- ✓ Coupling Express Long Reach (CE LR) (installed in a PCIe+ I/O drawer)

2.4. Integrated Coupling Adapter Short Reach1.1 (ICA SR1.1)

The Integrated Coupling Adapter Short Reach (ICA SR) feature (introduced with IBM z13®) is a two-port fanout that is used for short distance coupling connectivity and can be carried forward to z15. It uses PCIe Gen3 technology, with x16 lanes that are bifurcated into x8 lanes for coupling.

The ICA SR is designed to drive distances up to 150 m (492 feet) and support a link data rate of 8 GBps. The ICA SR fanout takes one PCIe I/O fanout slot in the z15 CPC drawer. It is used for coupling connectivity between z15, z14, z13, and z13s CPCs, and cannot be connected to HCA3-O or HCA3-O LR coupling fanouts. The ICA SR is compatible with another ICA SR or ICA SR 1.1 only.

The Integrated Coupling Adapter Short Reach (ICA SR1.1) is for high-speed short range coupling connectivity. The ICA SR1.1 is a two-port, short-distance

coupling fanout. Note that InfiniBand coupling links are not supported on the IBM z15.

Figure 11: Location of PCIe+ Fanout in the Processor Drawer

Figure 12: ICA SR1.1 and its sides

It uses PCIe Gen3 technology, with x16 lanes that are bifurcated into x8 lanes for coupling.
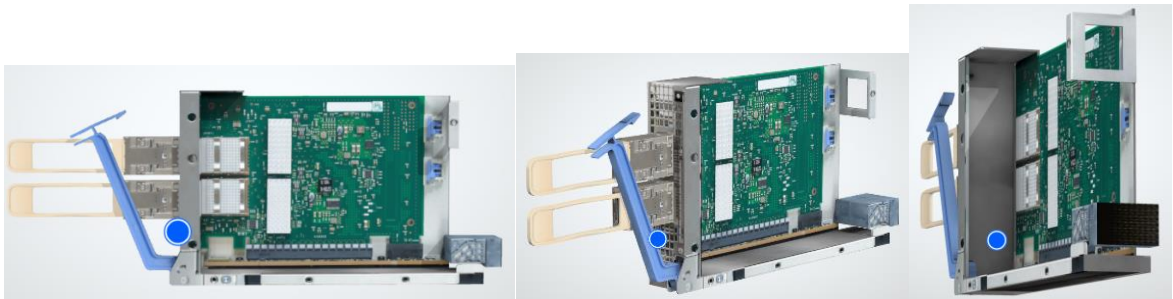
The ICA SR1.1 is designed to drive distances up to 150 m and support a link data rate of 8 GBps. The ICA SR1.1 fanout takes one PCIe fanout slot in the z15 CPC drawer.

It is used for coupling connectivity between z15, z14, z13, and z13s CPCs, and cannot be connected to HCA3-O or HCA3-O LR coupling fanouts. The ICA SR1.1 is compatible with another ICA SR1.1 or ICA SR only.

3. RoCE Express

The 25 GbE and 10 GbE RoCE Express2.1 features10 use Remote Direct Memory Access (RDMA) over Converged Ethernet (RoCE) to provide fast memory-to-memory communications between two Z platforms.

These features are designed to help reduce consumption of CPU resources for applications that use the TCP/IP stack (such as IBM WebSphere® that accesses an IBM Db2 database). They can also help reduce network latency with memory-to-memory transfers by using Shared Memory Communications over RDMA (SMC-R).

With SMC-R, you can transfer huge amounts of data quickly and at low latency. SMC-R is transparent to the application and requires no code changes, which enables rapid time to value.

The RoCE Express features help reduce the use of CPU resources for applications that use the TCP/IP stack. It might also help to reduce network latency with memory-to-memory transfers that use SMC-R in z/OS V2R1 and later versions. It is transparent to applications, and can be used for system-to-system communication in a multiple Z platform environment.

3.1. 10 GbE RoCE Express2.1

The 10 GbE RoCE Express2.1 provides increased virtualization/ sharing capability over the 10 GbE RoCE Express. Use of the adapter provides optimized communications across supported systems (i.e. z/OS, Linux on IBM Z, Linux on Power, AIX, etc.) with an application transparent solution called Shared Memory Communications - Remote Direct Memory Access (SMC-R). SMC-R is designed to deliver low latency, and low processor and operating system overhead.

Each 10 RoCE Express2.1 feature occupies one I/O slot but does not include a CHPID type. The 10GbE RoCE Express2.1 can be defined to up to 126 virtual functions (VFs) per feature (port is defined in z/OS Communications Server). The 10GbE RoCE Express2.1 features support up to 63 VFs per port (up to 126 VFs per feature).

SFP+ Optical Transciever
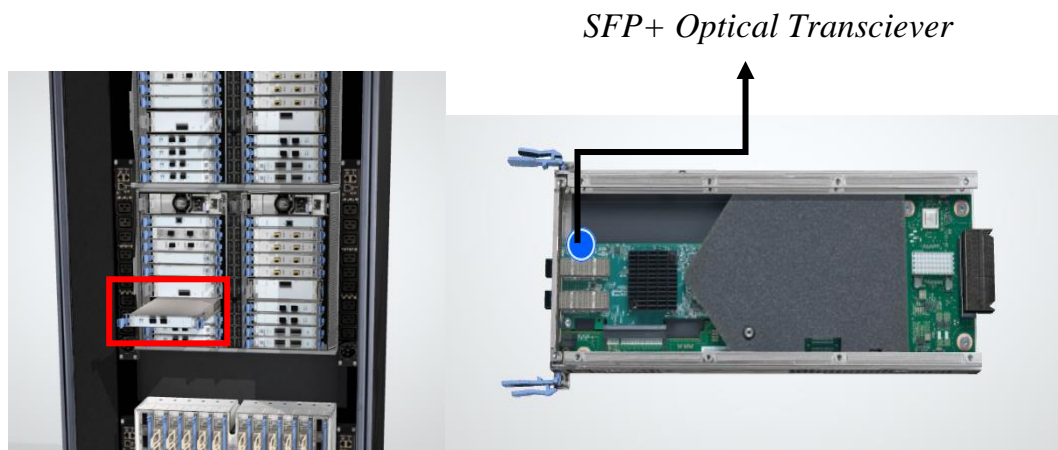
Figure 13: 10 GbE RoCE Express2.1's location and its inside

- Maximum number of adapters: 8*

- Speed: 10 GbE

* 10 GbE RoCE Express2.1 has two ports per adapter and is ordered new

3.2. 25 GbE RoCE Express2.1

25GbE RoCE Express2.1 (FC 0450) is installed in the PCIe+ I/O drawer and is supported only on IBM z15 servers. The 25GbE RoCE Express2.1 is a native PCIe feature. It does not use a CHPID and is defined by using the IOCP FUNCTION statement or in the hardware configuration definition (HCD).

The 25 GbE RoCE Express2.1 adapter provides optimized communications with Shared Memory Communications- Remote Direct Memory Access (SMC-R) across supported systems (i.e. z/OS, Linux, Linux on IBM Z, Linux on Power, AIX, etc.). The increased bandwidth of 25 GbE helps to meet increasing network performance demands.
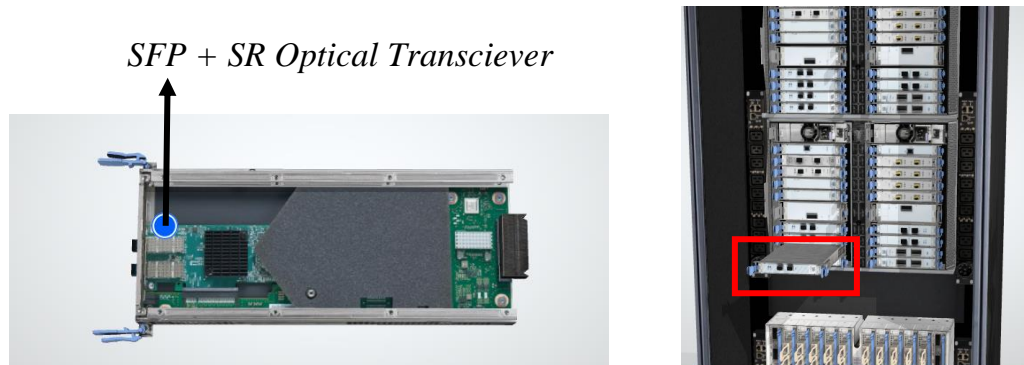
Figure 14: 25GbE RoCE Express2.1's location and its inside

- Maximum number of adapters: 8**

- Speed: 25 GbE

*** 25 GbE RoCE Express2.1 has one port per adapter and is ordered new*

Feature	Feature Code	Bit rate in Gbps (or started)	Cable type	Maximum unrepeated distance	Ordering information z15 T02
25 GbE RoCE Express2.1	0450	25	MM 50 µm	70 m (2000) 100 m(4700)	New build
10 GbE RoCE Express2.1	0432	10	MM 62.5 µm MM 50 µm	33 m (200) 82 m (500) 300 m (2000)	New build

*Table 2: Network connectivity features of 25 GbE RoCE Express2.1 and 10 GbE RoCE Express2.1*

Note: The 25 GbE RoCE Express should not be mixed with any type of 10 GbE RoCE Express in the same SMC-R link group. The 10 GbE RoCE Express adapters can be mixed in any combination in the same SMC-R link group.

4. Coupling Express Long Reach

The Coupling Express Long Reach (CE LR) is based on industry standard converged Ethernet technology and is used for long range coupling connectivity from the PCIe+ I/O drawer. Note that InfiniBand coupling is not supported on the IBM z15.

Coupling connectivity on the z15 use CE LR and Integrated Coupling Adapter Short Reach (ICA SR) features. The ICA SR feature supports distances up to 150 meters (492 feet), while the CE LR feature supports unrepeated distances of up to 10 km (6.21 miles) between Z platforms.

Coupling connectivity for Parallel Sysplex on z15 uses ICA SR and CE LR. ICA SR and CE LR technologies allow all of the z/OS-to-CF communication, CF-to-CF traffic, or Server Time Protocol (STP).

Coupling Express Long Reach (2 port)

SFP+ LR Optical Transceiver
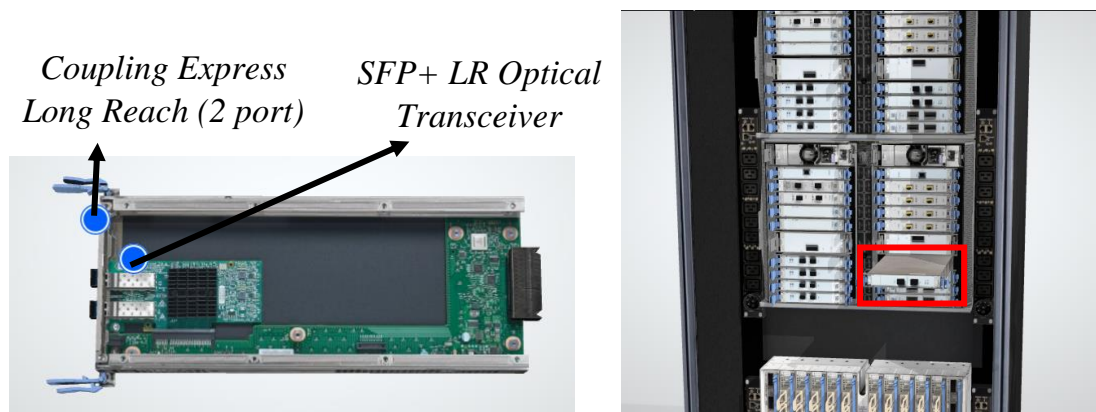
Figure 15: Coupling Express Long Reach's location and its inside

Feature	Feature code	Bit rate	Cable type	Maximum unrepeated distance	Ordering information
CE LR	0433	10 Gbps	SM 9 μm	10 km (6.2 miles)	New build or carry forward

Table 3: Coupling Express Long Reach features

- Maximum number of adapters: 32

5. Crypto Express7S

The Crypto Express7S is the latest generation of PCIe cryptographic coprocessors, available as an optional feature on the z15. These coprocessors, functioning as hardware security modules (HSMs), deliver high-security cryptographic processing essential for industries like banking.

This feature creates a secure programming and hardware environment for cryptographic processes, featuring general-purpose processors, non-volatile storage, and specialized cryptographic electronics. Housed in a tamper-sensing and tamper-responsive enclosure, the Crypto Express7S erases keys and sensitive data on any tampering attempt. Its security aligns with FIPS 140-2, Level 4 standards, the highest security level defined.

The Crypto Express7S (2-port) feature (0898) includes two PCIe cryptographic coprocessors, while the Crypto Express7S (1-port) feature (0899) includes one. A minimum of two features is required for the one-port variant due to availability reasons. The z15 T01 supports up to 30 Crypto Express7S (2-port) features, while z15 T02 supports 20. The maximum for the 1-port features is 16.

Each Crypto Express7S feature occupies one I/O slot in a PCIe+ I/O drawer. It can be configured as a Secure IBM Common Cryptographic Architecture (CCA) coprocessor, a Secure IBM Enterprise PKCS #11 (EP11) coprocessor, or as an accelerator. Crypto Express7S supports up to 85 LPARs (40 for z15 T02) and provides domain support for secure, long-term storage of keys or secrets.

The Secure IBM CCA coprocessor emphasizes specialized functions for banking and payment card systems. The Secure IBM EP11 coprocessor adheres to the PKCS #11 specification v2.20, introducing the PKCS #11 secure key function. When configured as a secure IBM CCA coprocessor, the Crypto Express7S provides accelerator functions, with up to 3x better performance achievable when configured as an accelerator.

The Crypto Express7S supports triple-length (192-bit) Triple Data Encryption Standard (TDES) keys, strengthening security. It also extends support for the

cryptographic requirements of the German Banking Industry Committee. Additional features include AES-related key management and AES ISO Format 4 (ISO-4) PIN blocks. IBM continues to enhance CCA to align with evolving AES finance industry standards.

(**) **The Crypto Express7S has two Hardware Security Modules (HSMs)** available to protect sensitive data and enables high volume secure web transactions. Each HSM is designed to meet FIPS 140-2 Level 4 compliance, can be configured as a PKCS#11 coprocessor or digital signatures), a CCA coprocessor, or as an accelerator for SSL/TSL transactions. The IBM z15 Model T02 now supports up to 20 2-HSM features, and up to 40 crypto HSMs in conjunction with 1-HSM features, supporting 40 domains, which provides over 1600 virtual HSMs for ultimate scalability.

Crypto Express7S (feature code 0898) has two Hardware Security Module (HSM) per adapter and is ordered new. Crypto Express7S (feature code 0899) has one HSM per adapter and is ordered new.
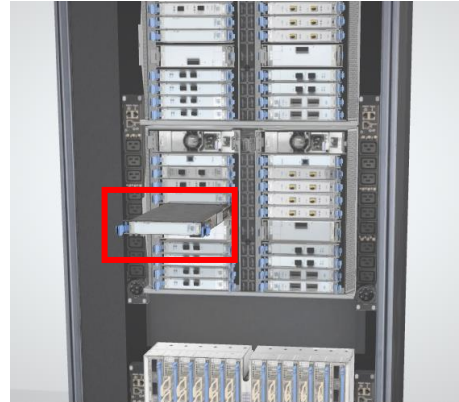
Figure 16: Crypto Express7S (1-port)'s location and its inside
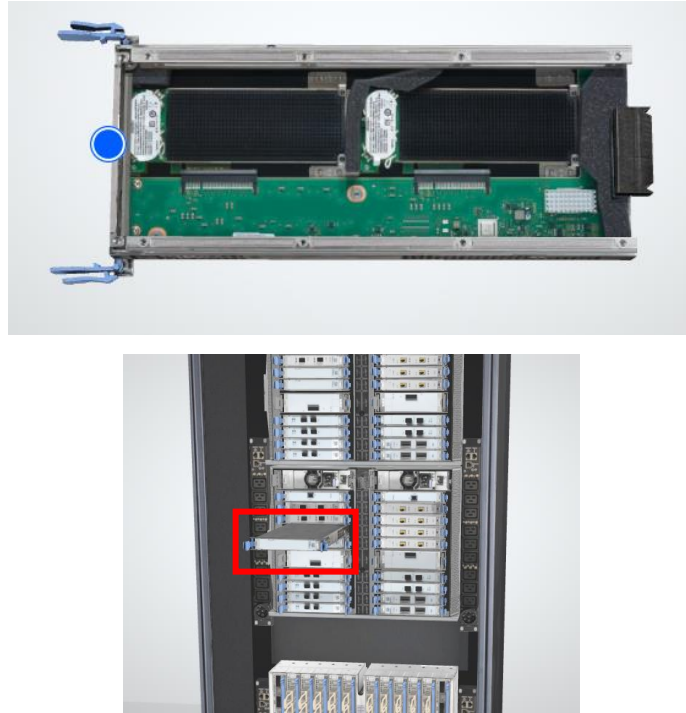
Figure 17: Crypto Express7S (2-ports)'s location and its inside

Cryptography – Maximum adapters §§	
Crypto Express7S – two Hardware Security Modules (HSM) per adapter	20
Crypto Express7S, Crypto Express6S, Crypto-Express5S – all have 1 HSM per adapter	16

Table 4: Crytography – Maximum adapters

6. FICON Express16S+
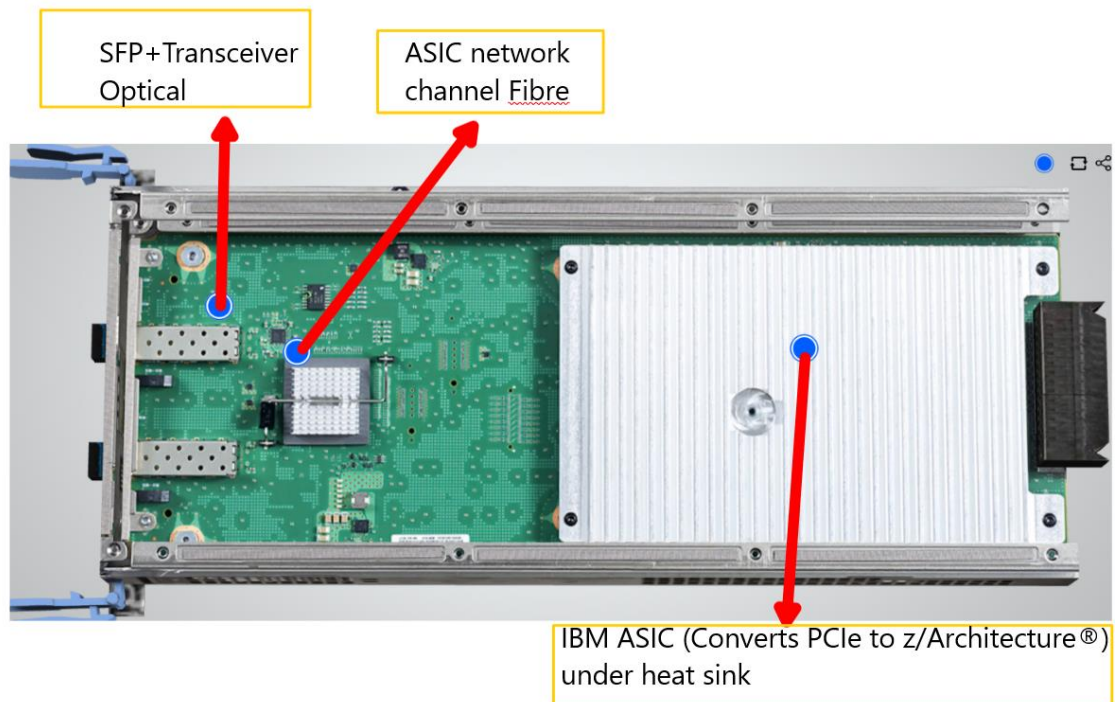
Figure 18: Inside of FICON Express16S+ with explaination some main parts

The FICON Express16S+ with 2-port feature connects your IBM z15 T02 to switches, directors and storage devices at speeds up to 16 Gbps. FICON, High Performance FICON (zHPF), channel-to-channel (CTC), and Fiber Channel Protocol (FCP) modes of operation are all supported.

Support maximum and minimum: The FICON Express16S+ features have 2 independent ports. Each feature occupies a single I/O slot by using one CHPID per channel. Each channel supports 4 Gbps, 8 Gbps, and 16 Gbps link data rates with auto-negotiation. The Maximum adapters o FICON Express 16S+ are 64 adapters. The FICON Express16S+ features are designed for connectivity to systems, switches, directors, disks, tapes, and printers, and can be defined in two ways:

- **CHPID type FC:**

– Native FICON, zHPF, and FICON CTC traffic

– Supported in the z/OS, IBM z/VM hypervisor, IBM z/VSE V6.2 (earlier z/VSE versions have no zHPF support), IBM z/Transaction Processing Facility (z/TPF), and Linux on IBM Z and the KVM hypervisor environments.

- **CHPID type FCP:**

– FCP traffic for communication with SCSI devices.

– Supported in IBM z/VM, z/VSE, and Linux on IBM Z and the KVM hypervisor environments.

Technology of FICON Express16S+ : The FICON Express16S+ features are ordered in two channel increments and added concurrently. This concurrent update capability allows you to continue to run workloads through other channels when the FICON Express16S+ features are being added.

All FICON Express16S+ features are in the Peripheral Component Interconnect Express (PCIe) I/O drawer or PCIe+ I/O drawer6 and use SFP optics to permit each channel to be individually serviced during a fiber optic module failure. Traffic on the other channels on the same feature can continue to flow if a channel requires servicing.

FICON Express features continue to evolve and deliver improved throughput, and reliability, availability, and serviceability (RAS). In the z15, these features can provide connectivity to other systems, such as Fibre Channel (FC) switches and various devices in a SAN environment. The FICON Express features are fully supported on the z15. They are commonly used with IBM z/OS, IBM z/VM (and guest systems), Linux on Z, IBM z/VSE, and IBM z/TPF.

Feature	Feature codes	Bit rate in Gbps (or stated)	Cable type	Maximum unrepeated distance	Ordering information z15 T01	Ordering information z15 T02
FICON Express16S+ LX	0427	4, 8, or 16	SM 9 µm	10 km (6.2 miles).	Carry forward	New build and carry forward
FICON Express16S+ SX	0428	4, 8, or 16	OM2, OM3, and OM4	See Table 4-3.	Carry forward	New build and carry forward

Table 5: Storage connectivity features

Cable type (Modal bandwidth)	2 Gbps	4 Gbps	8 Gbps	16 Gbps
OM2 (50 µm at 500 MHz·km)	300 meters	150 meters	50 meters	35 meters
	984 feet	492 feet	164 feet	115 feet
OM3 (50 µm at 2000 MHz·km)	500 meters	380 meters	150 meters	100 meters
	1640 feet	1247 feet	492 feet	328 feet
OM4 (50 µm at 4700 MHz·km)	N/A	400 meters	190 meters	125 meters
	N/A	1312 feet	623 feet	410 feet

Table 6: The expression FICON for types cable optic fiber multimode for distances.

7. zHyperLink Express1.1
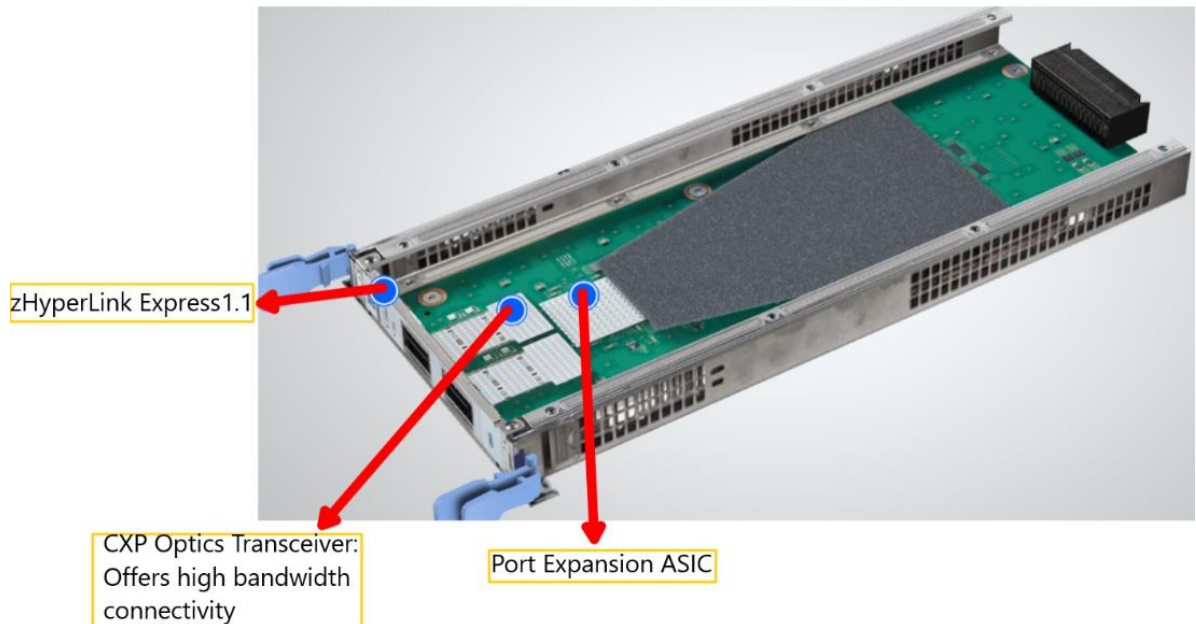
Figure 19: Inside of zHyperLink Express1.1 and explaination

zHyperLink was created to provide fast access to data by way of low-latency connections between the Z platform and storage.

Support maximum and minimum: The maximum adapters of IBM zHyperLink Express1.1 are 16 adapters. It has 2 ports I/O per adapter and is ordered new. IBM zHyperLink has two ports per adapter and can be carried forward. It offers direct connect, short distance (up to 150m - 492 feet) at a link data rate of 8 gigabytes

per second (GBps), low latency connectivity to FICON storage systems. A 24-fiber cable with MTP connectors is required for the ports of the zHyperLink Express feature. Internally, a single cable contains 12 fibers for transmit and 12 fibers for receive. zHyperLink significantly improves application response time for I/O sensitive workloads, and delivers the next generation of I/O for IBM Z storage.

Technology: Working with the FICON SAN Infrastructure, zHyperLink can improve application response time, which cuts I/O-sensitive workload response time in half without requiring application changes. IBM zHyperLink Express is a short-distance Z I/O adapter with up to 5x lower latency than High-Performance FICON, for read requests. This feature is housed in the PCIe+ I/O drawer and is a two-port adapter that is used for short distance (direct connectivity between a z15 and a DS8880 or newer).

Feature	Feature codes	Bit rate in Gbps (or stated)	Cable type	Maximum unrepeated distance	Ordering information z15 T01	Ordering information z15 T02
zHyperLink Express1.1	0451	8	OM3 and OM4	See table below	New build	New build

Table 7: Storage connectivity features of zHyperLink Express1.1

Cable type[a] (Modal bandwidth)	8 GBps
OM3 (50 µm at 2000 MHz·km)	100 meters (328 feet)
OM4 (50 µm at 4700 MHz·km)	150 meters (492 feet)

Table 8: Unrepeated distances for multimode fiber optic cable types for zHyperlink Express

8. OSA-Express6S 1000BASE-T

Figure 20: Inside of OSA-Express6S 1000BASE-T

Support maximum and minimum: OSA-Express6S 1000BASE-T support maximum 48 addapters. The Open Systems Adapter-Express6S (OSA-Express6S) 1000BASE-T 2-port feature connects to LANs at 100 and 1000 Mbps (1 Gbps) in Full Duplex only using copper cabling. Each port has an SFP with an RJ-45 receptacle for cabling to an Ethernet switch. The RJ-45 receptacle is required to be attached by using an EIA/TIA Category 5 or Category 6 UTP cable with a maximum length of 100 meters (328 feet). A 1 Gbps and 10 Gbps optical OSA-Express6S features are also available. On both cards, 1000 Mbps rates are only attainable via Auto Negotiate modes.

Technology: The OSA-Express6S 1000BASE-T feature supports auto-negotiation when attached to an Ethernet router or switch. If you allow the LAN speed and duplex mode to default to auto-negotiation, the OSA-Express port and the attached router or switch auto-negotiate the LAN speed and duplex mode settings between them. They then connect at the highest common performance speed and duplex mode of interoperation. If the attached Ethernet router or switch does not support auto-negotiation, the OSA-Express port examines the signal that it is receiving and connects at the speed and duplex mode of the device at the other end of the cable.

The OSA-Express6S 1000BASE-T feature can be configured as CHPID type OSC, OSD, or OSE. Non-QDIO operation mode requires CHPID type OSE.

Channel feature	Feature code	Bit rate in Gbps	Cable type	Maximum unrepeated distance[a] (MHz - km)	Ordering information z15 T02
OSA-Express6S 1000BASE-T	0426	100 or 1000 Mbps	Cat 5, Cat 6 unshielded twisted pair (UTP)	100 m	New build and carry forward

Table 9: Network connectivity features of OSA-Express6S 1000BASE-T

9. OSA-Express7S 25 GbE SR

SFP + SR Optical Receiver

IBM I/O ASIC

Figure 21: OSA-Express7S 25 GbE SR components

The OSA-Express7S 25 Gigabit Ethernet (GbE) Short Reach adapter offers increased throughput. It is multi-mode (SR) fiber only with 1 port and does not auto-negotiate to a slower speed. This adapter allows for potential consolidation of prior-level adapters, depending on usage characteristics.

Support maximum and minimum: OSA-Express7S 25 GbE SR support maximum 48 addapters.OSA-Express7S 25 GbE SR has one port per adapter and can be ordered new or carried forward.

Feature	Feature code	Bit rate in Gbps (or stated)	Cable type	Maximum unrepeated distance[a]	Ordering information z15 T02
OSA-Express7S 25 GbE SR	0429	25	MM 50 µm	70 m (2000) 100 m (4700)	New build and carry forward

Table 10: Network connectivity features of OSA-Express7S 25 GbE SR compo

10. PCIe Interconnect Gen3

Figure 22: PCIe Interconnect Gen3

PCIe Interconnect Gen3 supports 8 features in the PCIe+ I/O drawer. It also provides the Redundant I/O Interconnect (RII) functionality.

The PCIe Generation 3 uses 128b/130b encoding for data transmission. This configuration reduces the encoding overhead to about 1.54% versus the PCIe Generation 2 overhead of 20% that uses 8b/10b encoding.

The PCIe standard uses a low-voltage differential serial bus. Two wires are used for signal transmission, and a total of four wires (two for transmit and two for receive) form a lane of a PCIe link, which is full-duplex. Multiple lanes can be aggregated into a larger link width. PCIe supports link widths of 1, 2, 4, 8, 12, 16, and 32 lanes (x1, x2, x4, x8, x12, x16, and x32).

The data transmission rate of a PCIe link is determined by the link width (numbers of lanes), the signaling rate of each lane, and the signal encoding rule. The signaling rate of one PCIe Generation 3 lane is eight gigatransfers per second (GTps), which means that nearly 8 gigabits are transmitted per second (Gbps).

Note: I/O infrastructure for z15 T02 is implemented as PCIe Generation 3. The PU chip PCIe interface is PCIe Generation 4 (x16 @32 GBps), but the CPC I/O Fanout infrastructure uses PCIe Generation 3 connectivity

A PCIe Gen3 x16 link features the following data transmission rates: The maximum theoretical data transmission rate per lane: 8 Gbps * 128/130 bit (encoding) = 7.87 Gbps=984.6 MBps The maximum theoretical data transmission rate per link: 984.6 MBps * 16 (lanes) = 15.75 GBps Considering that the PCIe link is full-duplex

mode, the data throughput rate of a PCIe Gen3 x16 link is 31.5 GBps (15.75 GBps in both directions).

Link performance: The link speeds do not represent the performance of the link. The performance depends on many factors, including latency through the adapters, cable lengths, and the type of workload.

PCIe Gen3 x16 links are used in z15 servers for driving the PCIe+ I/O drawers, and for coupling links for CPC to CPC communications.

11. Top Exit Cabling

Figure 23: Top Exit Cabling

The single 19-inch frame design of the IBM z15 Model T02 is capable of supporting top or bottom exit I/O, as well as top or bottom exit power.

For the z15 Model T02 server, the top exit of all cables for I/O or power is always an option with no feature codes required. Adjustable cover plates are available for the openings at the top rear of each frame. The Top Exit feature code (FC 7898) provides an optional Top Exit cover enclosure. The optional Top Exit cover enclosure provides cable retention hardware and mounting locations to secure Fiber Quick Connector MPO3 brackets on the top of the frames. All external cabling enters the system at the rear of the frames for all I/O adapters, management LAN, and power connections. Feature code 7898 provides a top hat assembly to be installed at the top of each frame in the configuration. This assembly is designed to assist with fiber

trunking management. Overhead I/O cabling is contained within the frames. Extension "chimneys" that were featured with previous Z systems are no longer used.

12. Ethernet Switches
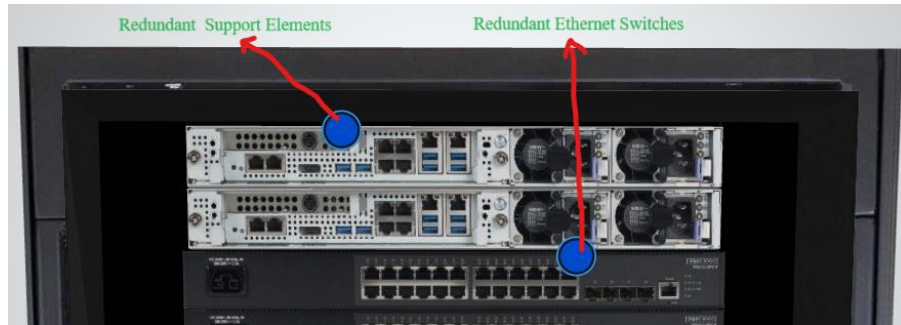
Figure 24: Ethernet Switches

Two redundant Ethernet top of rack switches are provided for internal hardware management communications.

Ethernet switches for HMC and SE connectivity are provided by the client. Existing supported switches can still be used. Ethernet switches and hubs often include the following characteristics: A total of 16 auto-negotiation ports 100/1000 Mbps data rate Full or half duplex operation Auto medium-dependent interface crossover (MDIX) on all ports Port status LEDs.

Note: The recommendation is to use a switch with 1000 Mbps/Full duplex support.

13. Intelligent Power Distribution Unit
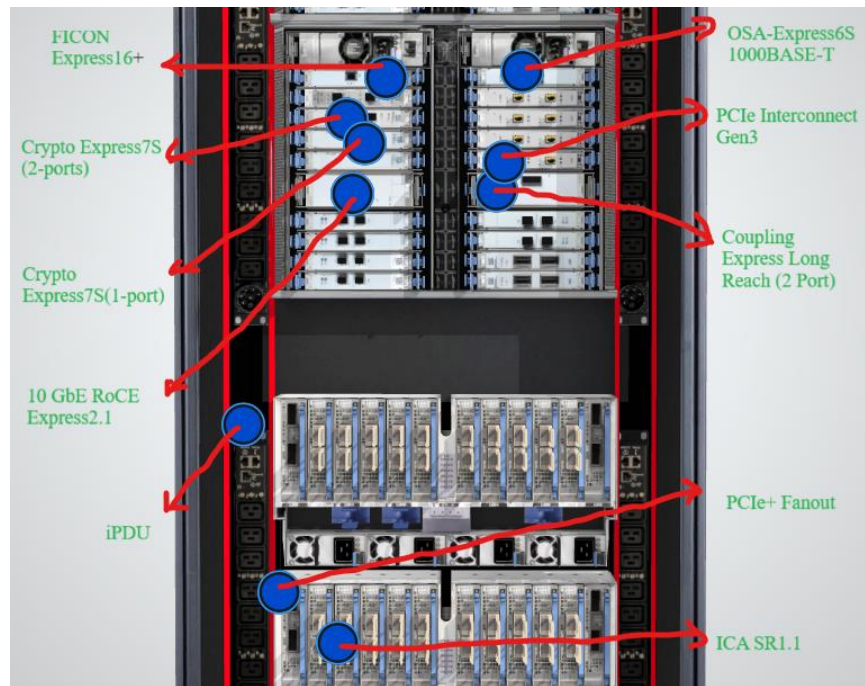
Figure 25: Intelligent Power Distribution Unit

The IBM z15 offers an intelligent power distribution unit (iPDU) power option. The iPDU design comes in pairs of iPDUs with up to two pairs in a fully configured system. Use of iPDUs creates an opportunity to utilize common data center power drops while maintaining the redundant power, cooling and line cords that are intrinsic to high-reliability IBM Z offerings.

The iPDU is designed to provide RAS functions such as system reset power control, Support Element (SE) power cycling, Ethernet switch power cycling, power redundancy check for site power maintenance, concurrent firmware updates and concurrent repair.

The internal intelligent Power Distribution Unit (iPDU, or PDU) provide the following capabilities: Individual outlet control by way of Ethernet:

– Provide a System Reset capability

– Power cycle an SE if a hang occurs – Verify a power cable at installation

14. Spine

Figure 26: Spine

The spine is shipped with configurations that contain more than two PCIe+ I/O drawers or more than one CPC drawer. All external cabling to the system (from top or bottom) can use the spine to minimize interference with the PDUs mounted on the sides of the frame. If necessary, the spine easily can be relocated for service procedures.

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GROUP DISCUSSIONS

17:12

@Bảo Huỳnh cái phần " chip" nhứa kiếm mấy cái thiết kế chip ntn nha, nếu có

17:15

Có tin nhắn mới

Bảo Huỳnh
okok

Nhập @, tin nhắn tới KTMT - Báo Cáo IBM

mn cô kêu viết = TA zị cái bìa có viết = TA không?

hay để TV
13:18

Nguyễn Ngọc Quỳnh Như
Cái bìa tiếng việt

Nhưng nội dung tiếng anh hết á

40

Hôm nay

@All
1. Bảo: làm 5 phần đầu "door -> ica"
2. Như: làm 5 phần "10 gb -> crypto (2ports)"
3. Vũ: làm 5 phần "pci ->spine"
4. Nam 4 phần "ficon ->osa 1.1" + 1 phần overview

❤️ 1

🕐 GHIM TIN NHẮN

HD
03
Components

Doors — **Close**

Processor Drawer — **Replace**

Processor Single-Chip Module
(SCM) — **Remove**

PCIe+ Fanout — **Replace**

ICA SR1.1 — **Remove**

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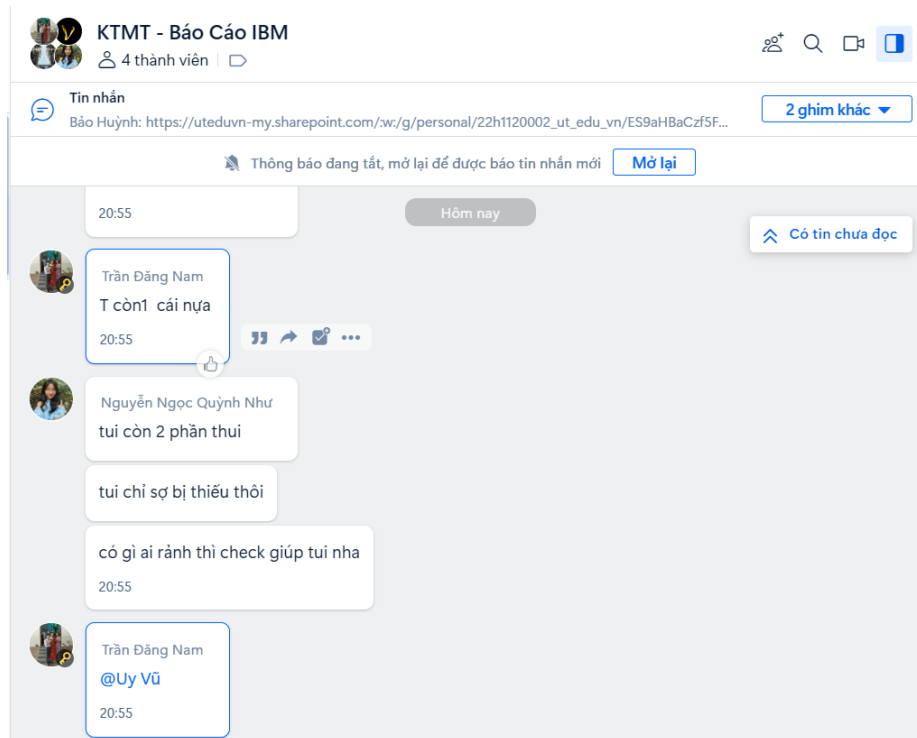
KTMT - Báo Cáo IBM
4 thành viên

Tin nhắn
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2 ghim khác ▾

17:08 Hôm nay

Uy Vũ
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chứ trong kia ít quá
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Uy Vũ
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@Uy Vũ thiếu thì tìm thêm

❤️ 1 👍

Trần Đăng Nam
1. z15 technical intro https://www.redbooks.ibm.com/redbooks/pdfs/sg248850.pdf 2. z15...

tìm ở 2 trang này vẫn thiếu à @Uy Vũ

Nhập @, tin nhắn tới KTMT - Báo Cáo IBM

nên coi như làm đến đâu phụ trước 1 phần cho mau
17:37

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Bảo Huỳnh
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17:55

👍 1 👍

@All t biết cách tìm thông số rồi ?
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18:03

Bảo Huỳnh
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👍 1 👍

@Uy Vũ kiếm phụ tui cái này dới Integrated Coupling Adapter Short Reach1.1 (ICA SR1.1)

tui kiếm mờ mắt gòi :<
18:15

Uy Vũ

> **Bảo Huỳnh**
> @Uy Vũ kiếm phụ tui cái này dới Integrated Coupling Adapter Short Reach1.1 (ICA SR1.1)

@Bảo Huỳnh để t gắn mấy phần t xong r t kiếm đc ko
18:17

👍

❤️

Uy Vũ đang soạn tin trên máy tính ● ● ●

Nhập @, tin nhắn tới KTMT - Báo Cáo IBM

Thông báo đang tắt, mở lại để được báo tin nhắn mới   Mở lại

20:55   Hôm nay   Có tin chưa đọc

Trần Đăng Nam
T còn1 cái nựa
20:55

Nguyễn Ngọc Quỳnh Như
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có gì ai rảnh thì check giúp tui nha
20:55

Trần Đăng Nam
@Uy Vũ
20:55

Bảo Huỳnh
ok   Hôm nay

phần k chắc là t bỏ dô đúng phần max min :< tại số liệu nó ẩn thân qá kiếm hông thấy

2.3 trong tài liệu có phần PCIe+ drawer mà chỗ component thấy nó chỉ ghi mỗi chữ fanout thui nên t lược bớt phần drawer I/o của nó r, ổn hông mấy bợn

còn ổn hông bây
20:32

Nguyễn Ngọc Quỳnh Như
hơi ổn
20:32

Bảo Huỳnh
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20:33

Nguyễn Ngọc Quỳnh Như

Nhập @, tin nhắn tới KTMT - Báo Cáo IBM

🔕 Thông báo đang tắt, mở lại để được báo tin nhắn mới   **Mở lại**

Hôm nay

Trần Đăng Nam

> **Nguyễn Ngọc Quỳnh Như**
> tui kh dám xài AI luôn =)))

@Nguyễn Ngọc Quỳnh Như đọc 2 file á

nó khá đủ

> **Bảo Huỳnh**
> có j mn liếc qua phần tui 1 xí nha

@Bảo Huỳnh chỉnh layout 2 cái của t vừa làm xong nha, t chỉnh sơ r phần 11 12

❞ TRẢ LỜI

@Uy Vũ ok chưa ô
20:21