Long Chung Chan **Harry**

FPGA Researcher · Embedded Software Developer · Android Developer · Tech Enthusiast

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Education

University of Waterloo

Sept. 2015 - Apr. 2020	**BASc**, Electrical and Computer Engineering	*Waterloo, Canada*
May. 2020 - Jan. 2022	**MASc**, Electrical and Computer Engineering	*Waterloo, Canada*

Full Time Experience

Efinix Canada, Inc — *Toronto, CA*

Senior Software Engineer — *Jan. 2022 - now*

Coop Experience

Smartwave Technologies — *Toronto, CA*

Embedded Software Engineering — *Aug. - Dec. 2019*

- Designed a custom advertising format allowing various products to communicate under the **Bluetooth 5** standard using only the advertising channel reducing battery consumption
- Implemented a firmware targeting **Scilicon Labs Bluetooth Low Energy Series** to send data in periodic, burst and random patterns

Envieta System LLC — *Maryland, US*

FPGA Crypto Developer — *Aug. - Dec. 2018*

- Implemented a post-quantum cryptosystem - **CRYSTALS-Kyber** on **FPGA** board using **VHDL** allowing future-proof security standard to increase product value
- Verified the implementation on **DE10-Nano board** running drivers written in C to ensure run-time requirements and security standards

Sensibill Inc. — *Toronto, CA*

Android Developer — *Jan. - Apr. 2018*

- Integrated a smoother UI experience allowing the user to capture longer receipts by using **shape and contour detection** in **OpenCV**, resulting in better image quality and higher accuracy data extraction from the receipt
- Redesigned receipt capture function using **Kotlin** from scratch for higher readability and cleaner architecture

Ritual Technologies Inc. — *Toronto, CA*

Mobile Development Engineering — *May. - Aug. 2017*

- Accomplished smooth transition to **Android Oreo** by restructuring notifications using **Notification Channels** and adding **AutoFill** onto the sign-in flow
- Added easy-switching between testing servers to visualize in-progress features in the compiled application, resulting in 30% shorter development time for new features

Academic Research

UWaterloo Configurable Architecture Group — *University of Waterloo*

Undergraduate Research Assistant — *Jan. - Aug. 2019*

- Pubished a paper called - **'Partitioning FPGA-Optimized Systolic Arrays for Fun and Profit'** and **presented** in the **ICFPT 2019** hosted in TianJin and received the **Best Paper Award**

Real-Time Embedded Software Group — *University of Waterloo*

Engineering Project Course - ECE499 — *Jan. 2020 - Present*

- Studied and designed a benchmark suite for testing **Apache Flink**'s **Data Streaming API** measuring the latency created by the framework

Skills

Programming Languages	Python, C/C++, JAVA, Kotlin, VHDL, Verilog
Web	Django with Python, React
Tools	Docker, Adobe PhotoShop, Adobe XD
Languages	English, Madarin, Cantonese