Harry Hu

Computer Engineering | University of Toronto
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Education

University of Toronto Toronto, Ontario
Bachelor of Applied Science and Engineering *Sept 2018 – May 2024*

- Edward S Rogers Sr. Admission Scholarship & J. Edgar Mcallister Award
- **Relevant courses**: Algorithms & Data structures, Statistics, Database, Software Design, Computer Networks, Operating Systems, Computer Security

Experience

Backend Software Engineer, Intern
Originforest ltd. *May 2021 – Aug 2022*

- Help test a highly scalable, efficient, and robust system for Alibaba cloud management platform.
- Implemented test automation, design, and collaborated with ML engineers & cross functional teams to productionize models and deliver new features

Student Technician, Work-Study *May 2022 – April 2023*
TIL University of Toronto

- Worked closely with professors in providing technical expertise and real-time troubleshooting campus-wide
- Managed technical equipment at the University and performed consultation on enhancing classroom experience

Selected Projects

NOBS GIS Application, Software Design and Communications (C++) *Winter 2021*

- Implemented an inexpensive A* Heuristic pathfinding algorithm with multi-threading.
- Graphically mapped 18 major cities using callback functions and with street data extracted from OpenStreetMap API.
- Developed familiarity with VM and collaborative coding on version control systems like Git.

Secure Multi-threaded Webserver (C) *Fall 2022*

- Implemented a server that handles http static and dynamic content requests from client on a listening socket
- Created a fixed pool of worker threads and scheduler to service requests efficiently.
- Enhanced performance and avoided underutilization of cores on multicore machines significantly
- Improved security by filtering inputs to prevent Cross-Site Scripting attacks and added SSL protocols to secure TCP connection using SHA1 and SSLv3

Reliable UDP File transfer Program (C) *Winter 2021*

- Added flow and congestion control to a UDP based connectionless network protocol
- Uses ACK and flags at packet headers to ensure a more reliable delivery of files (various types)
- Monitored packet traffic and congestion

Enhanced Processor (Verilog and Assembly) *Winter 2021*

- Implemented a x32 bit processor with basic operations and assembly commands to read/write to memory using Verilog on an Altera Cyclone V FPGA
- A thorough understanding of CPU and memory architecture as well as memory mapped I/O devices

Technical Skills

Programs: Matlab, LTspice, Typhoon HIL, Wireshark, AutoCAD, GNS3
Languages and frameworks: Java, Python, C/C++, HTML, Javascript, REACT, flask, ARMS Assembly, SQL, Verilog