

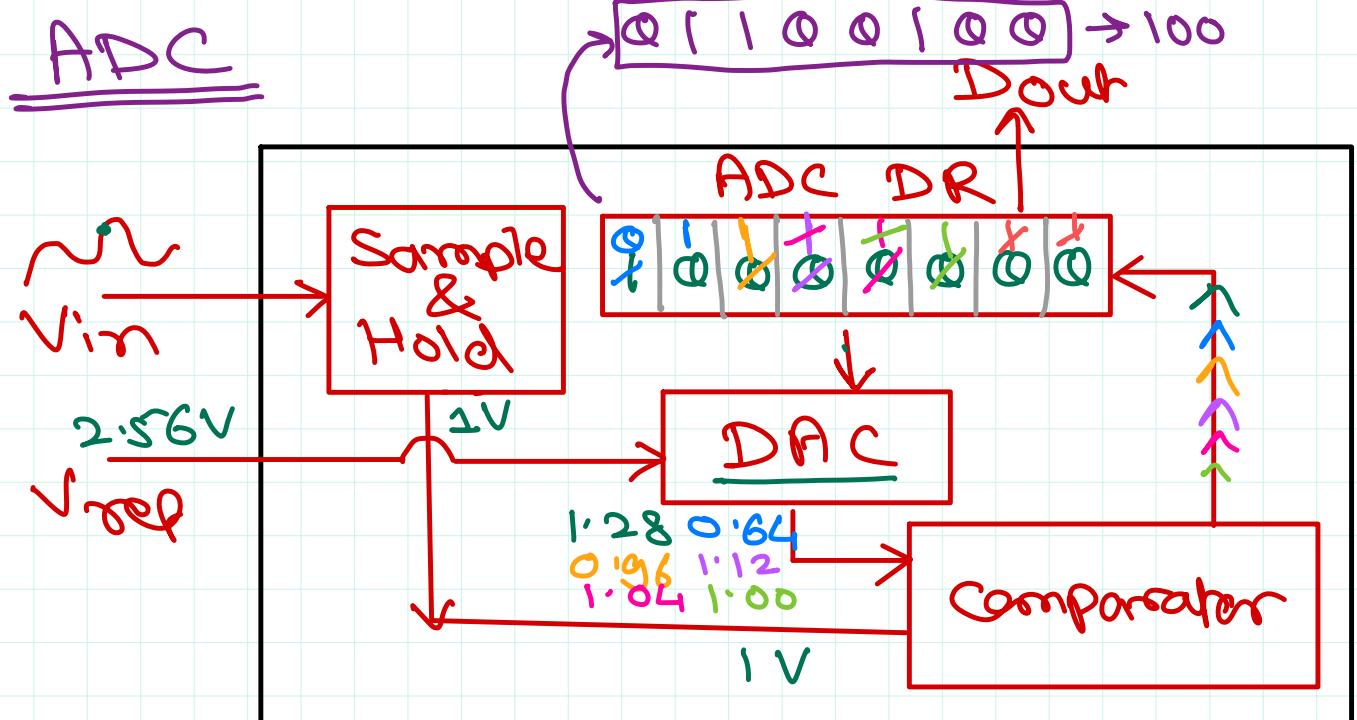


Advanced Micro-controllers - ARM

DESD @ Sunbeam Infotech



ADC



Successive Approx ADC

Digital Output from Wa:

$$D_{out} = \frac{V_{in}}{V_{ref}} \times 2^n$$

$$\text{e.g. } V_{in} = 1V$$

$$= \frac{1}{2.56} \times 256$$

$$= \underline{\underline{100}}$$

Num of Cycles
(ADC clock)
= min
num of bits + 1
e.g. 9-11 cycles.

ADC resolution: n-bits.

e.g. 8-bit ADC.

Number of Steps: 2^n

$$\text{e.g. } 2^8 = 256$$

Reference voltage: V_{ref}
External / internal
Voltage required for
ADC conversion.

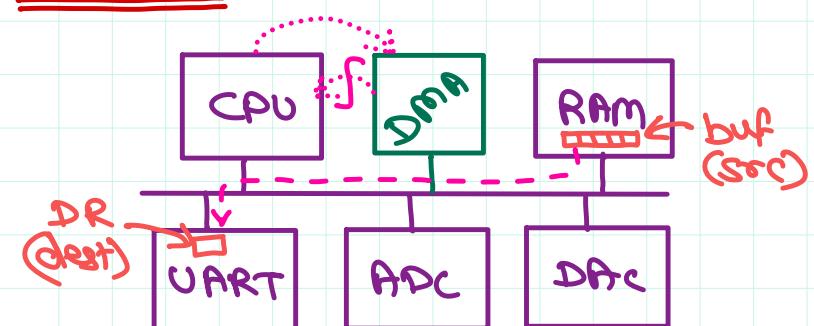
$$\text{e.g. } 2.56V.$$

Step size: Smallest change
in V_{in} (input analog
voltage) which will
cause O/P to change.

$$\text{Step size} = \frac{V_{ref}}{\text{Step cnt}}$$

$$\text{e.g. } \frac{2.56}{2^8} = 0.01V = 10mV.$$

DMA



UART Tx Polling

- ① CPU get first char from RAM buffer (buffer → data to tx).
- ② CPU write it to UART DR.
- ③ CPU will wait for data tx.
- ④ repeat steps 1-3 for next char.

UART Tx Interrupt

- ① Init: UART will generate int after Tx of each byte.
- ② CPU will execute int handler.
 - ⓐ get next char from RAM buffer
 - ⓑ write it to UART DR.
- ③ when CPU not executing int handler, it can be used for some other task

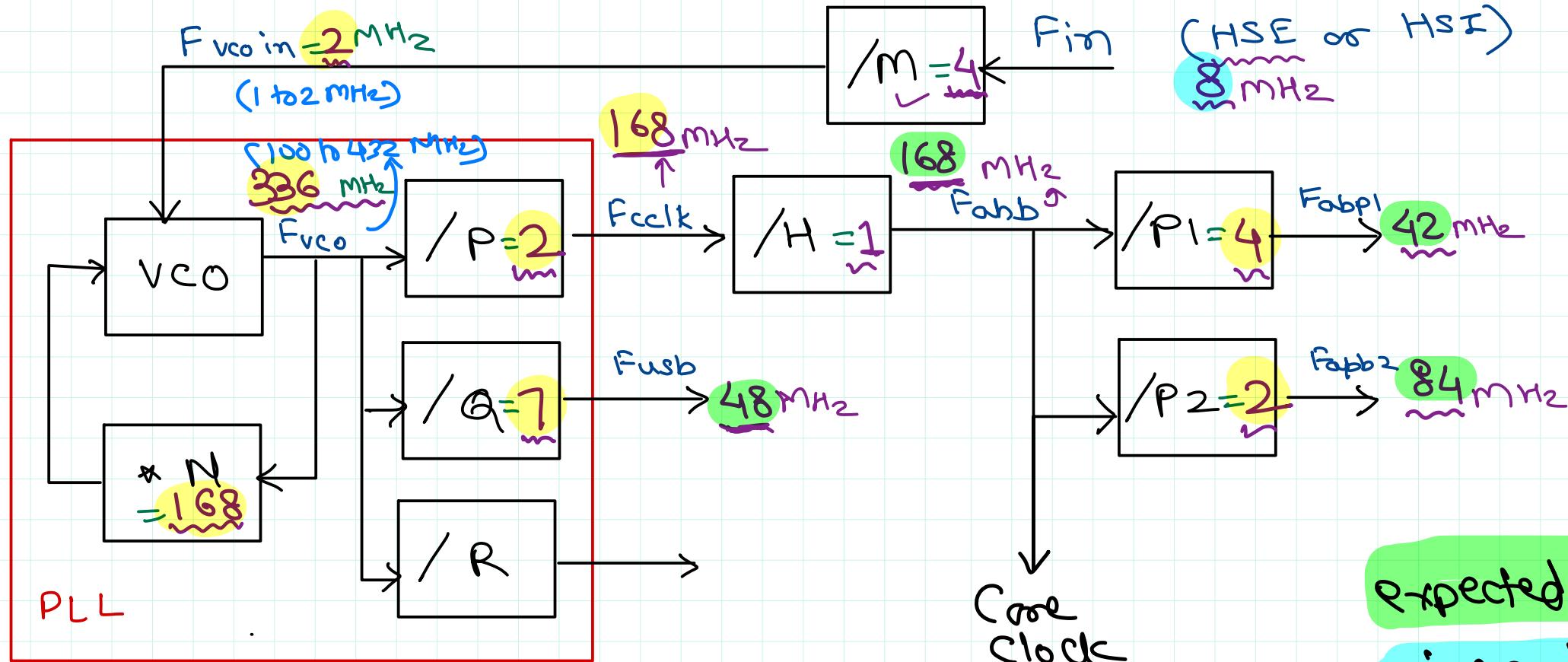
UART Tx - DMA

- ① Init: CPU will init DMA controller.
 - ⓐ source addr
 - ⓑ dest addr
 - ⓒ size
 - ⓓ enable DMA & its intr.
- ② DMA will now transfer data from src to dest without intervention of CPU.
- ③ when transfer completes, DMA controller inform to CPU via interrupt.

DMA transfers

- ① M2M → Memory to Memory (buffer copy).
- ② P2M → Peripheral to memory (e.g. UART Rx, ADC, ...)
- ③ M2P → Memory to Peripheral (e.g. UART Tx, DAC, ...)

STM32 PLL 168 MHz Config



expected output
given input



Thank You!

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