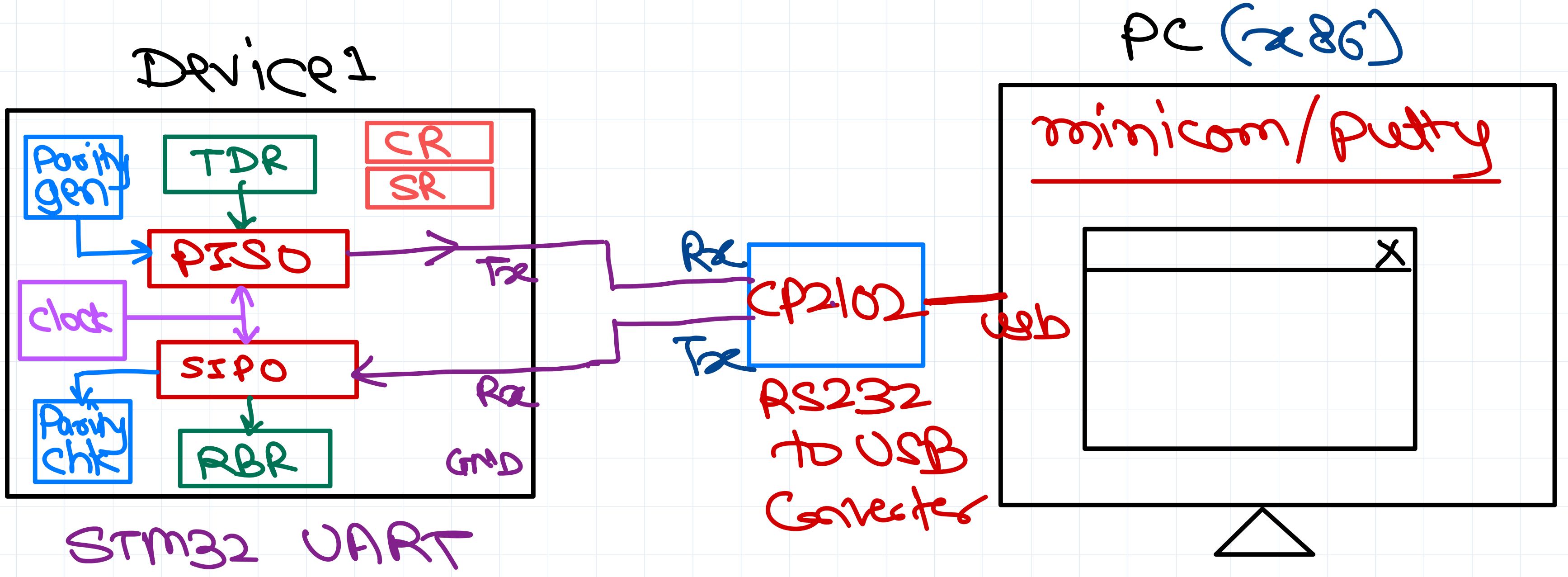
Advanced Micro-controllers - ARM

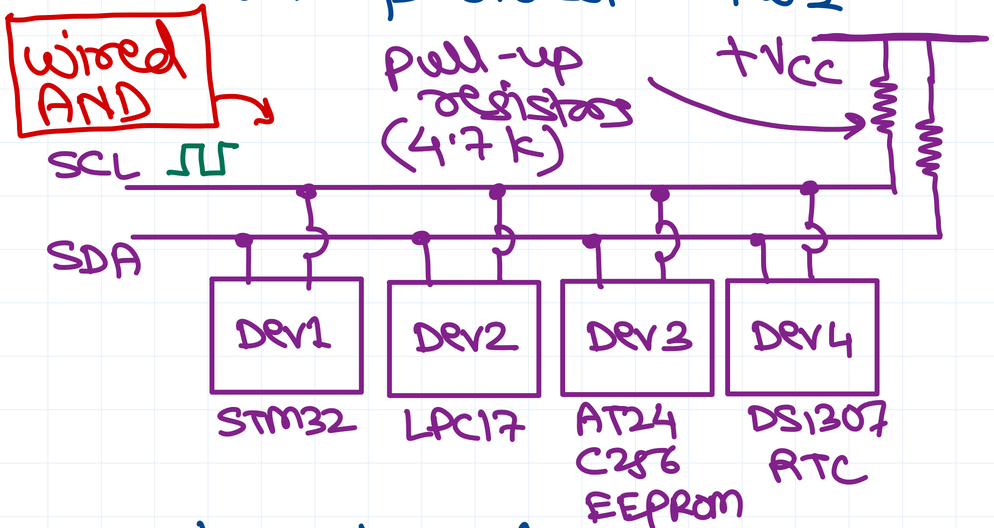
DESD @ Sunbeam Infotech



Nilesh Ghule

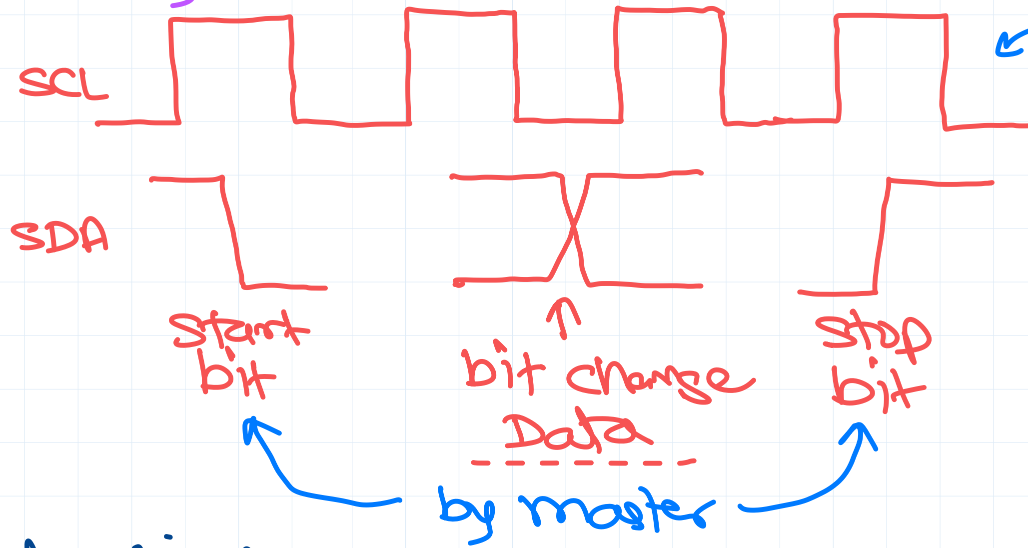
I2C → IIC → Inter-IC Commⁿ

- Philips
- Synchronous serial commⁿ
- bus protocol
- TTL voltage (0V-5V, 0-3.3V)
- Frequency (bit-rate): 100 KHz (standard)
  - 400 KHz (fast)
  - 1 MHz+ (fast plus)
- 2-wire protocol → TWI

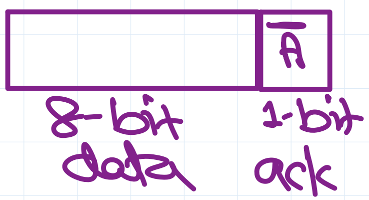


- master-slave bus.
  - master: generate clock
    - start/stop commⁿ
- multi-master bus
  - multiple devices are capable to become master → only 1 master at a time.

- half duplex protocol.
- each device has unique i2c addr.
  - → 7 bit addr → $2^7 \approx 128$ addresses
    upto 120 devices can be connected on a bus (few addr reserved).
  - → I2C new specs → 10 bit addr
- I2C bus wires form wired AND cct. When any one device pull the line low, effective line level will be zero. If no device pulling line low, the line level will be one (high).
- bit change (on data line) will happen only when clock line is low.



I2C frame



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Thank You!

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