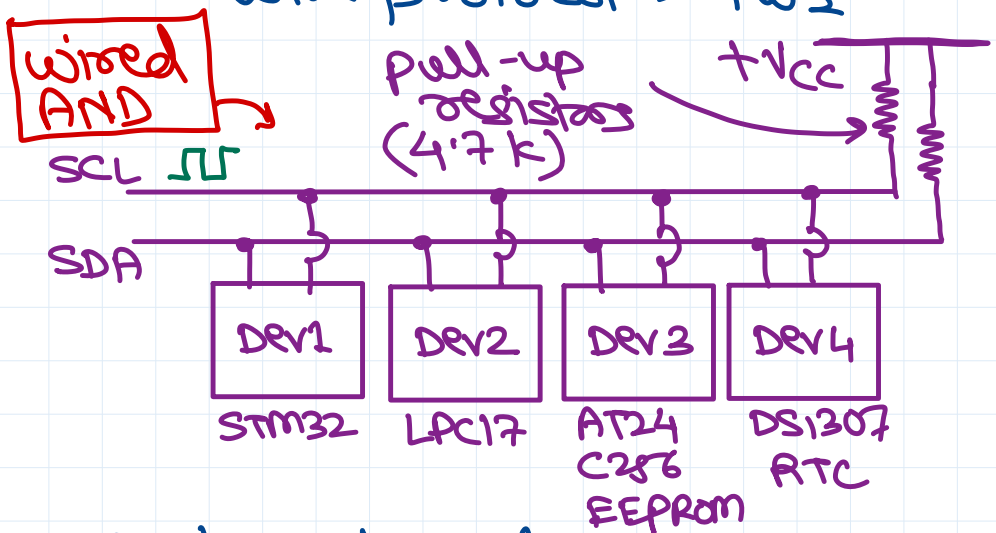
Advanced Micro-controllers - ARM

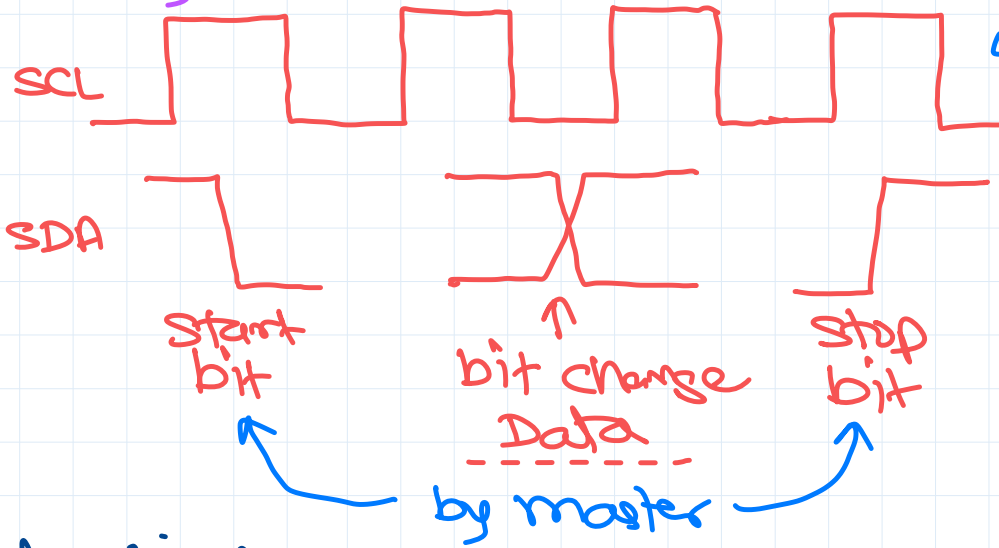
DESD @ Sunbeam Infotech

I2C → IIC → Inter-IC Comm^n

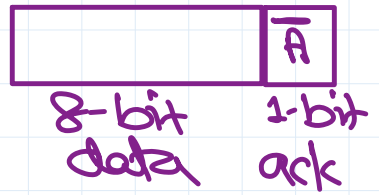
- Philips – short distance comm^n
- Synchronous serial comm^n
- bus protocol
- TTL voltage (0V–5V, 0–3.3V)
- Frequency: 100 KHz (standard) (bit-rate) 400 KHz (fast) 1 MHz+ (fast plus)
- 2-wire protocol → TWI



- master-slave bus.
  - master: generate clock
    - start/stop comm^n
- multi-master bus
  - multiple devices are capable to become master → only 1 master at a time.
- half duplex protocol.
- each device has unique I2C addr.
  - → 7 bit addr → $2^7 \approx 128$ addresses
    upto 120 devices can be connected on a bus (few addr reserved).
  - → I2C new specs → 10 bit addr
- I2C bus wires form wired AND cct. When any one device pull the line low, effective line level will be zero. If no device pulling line low, the line level will be one (high).
- bit change (on data line) will happen only when clock line is low.



I2C frame



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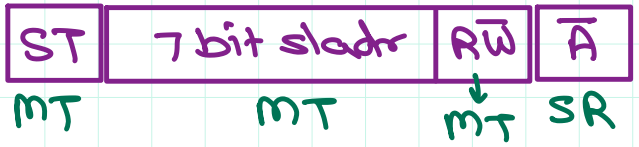
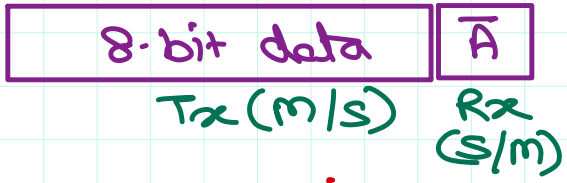
I2C frames (9-bit)

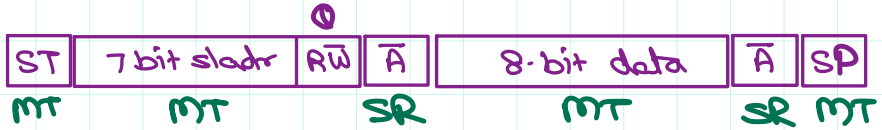
① addr frame



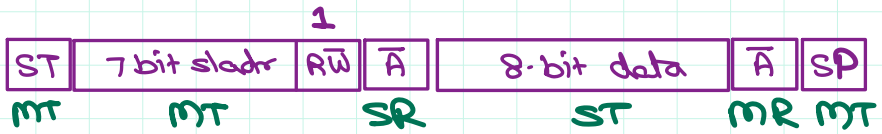
② data frame



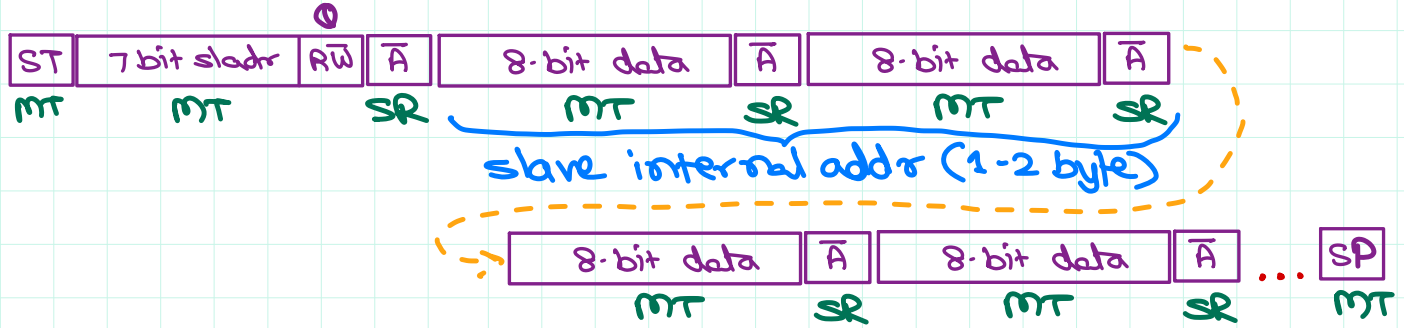
Single Byte write (M→S)



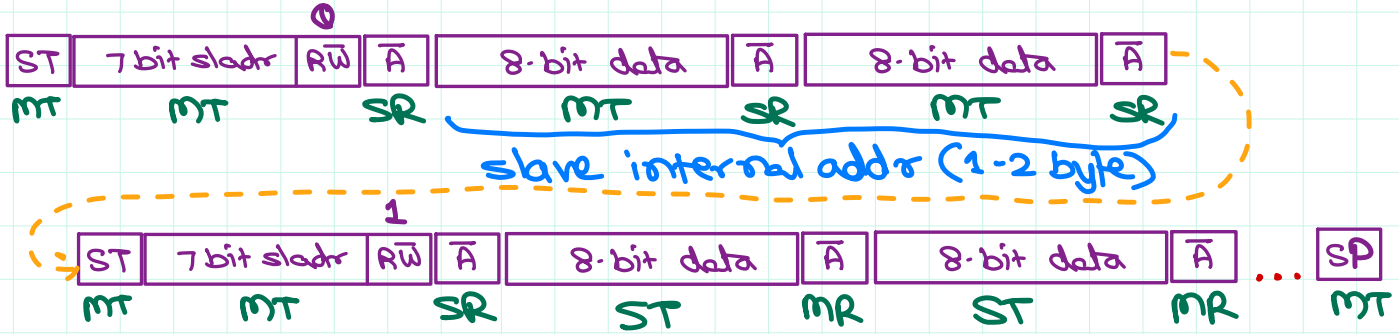
Single Byte Read (M←S)



Multi- Byte write (M→S)



multi-byte read operation.



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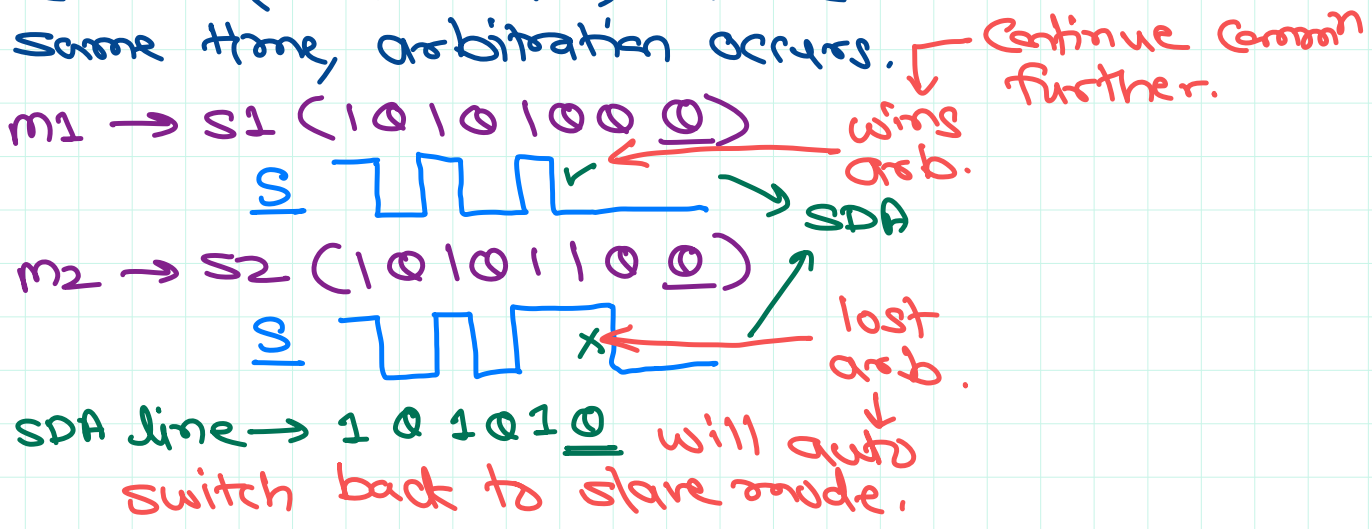
Arbitration

- multi-master bus.
- master can initiate comm^n, if bus is available (not in use by other master).
- when multiple masters initiate comm^n (send START) at the same time, arbitration occurs.



clock stretching

when slave is not ready to process the next data byte (busy), it will make clock line low.

So master clock is disabled (due to wired AND) and no further transfers are done.

The clock resumes only after slave release the clock line.

Thank You!

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