Advanced Micro-controllers - ARM

DESD @ Sunbeam Infotech

STM32

i2c

SDA —— SDA
SCL —— SCL

PCF8754

data   cmd

P0 1 1 1 1 ← data cmd
    0 0 0 0   RS
P1 0 0 0 0   RW
P2 1 0 1 0   EN
P3 1 1 1 1   BL
P4 x x y y   D4
P5 x x y y   D5
P6 x x y y   D6
P7 x x y y   D7

HD44780

Data
x x x x   y y y y

① RS=0/1, RW=0, EN=1
② nibble → x x x x
③ EN=0

① RS=0/1, RW=0, EN=1
② nibble → y y y y
③ EN=0

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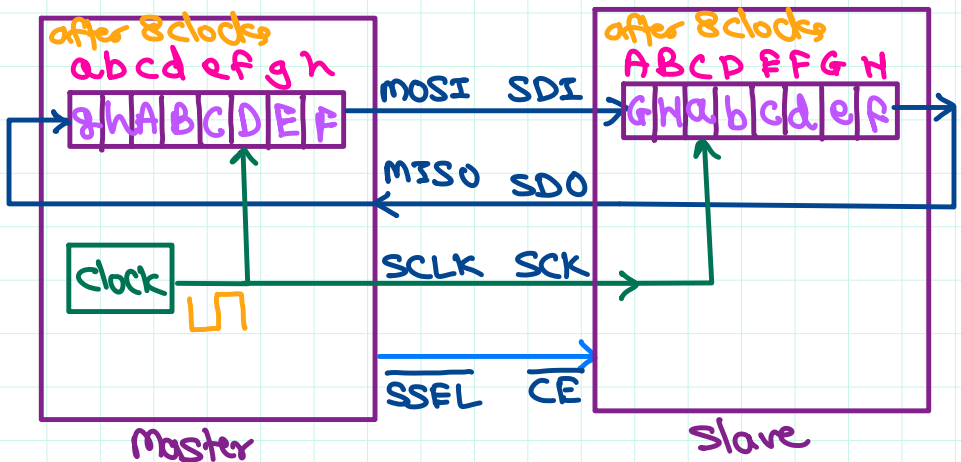# SPI = Serial Peripheral Interface

① Motorola (NXP)
② Short-distance protocol
③ 4-wire protocol
④ Synchronous serial protocol
⑤ full duplex (always)
⑥ TTL voltage
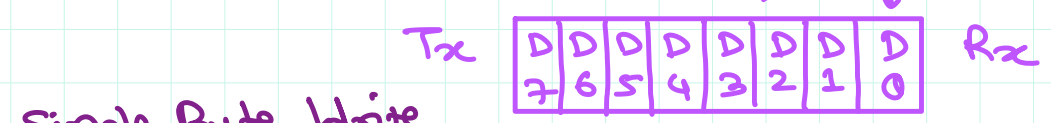⑦ frequency: MHz (1-10) (SPAD)
⑧ bus protocol
⑨ multi-master bus

SPI clock config:

CPOL → clock polarity 0 = base low   1 = base high
CPHA → clock phase
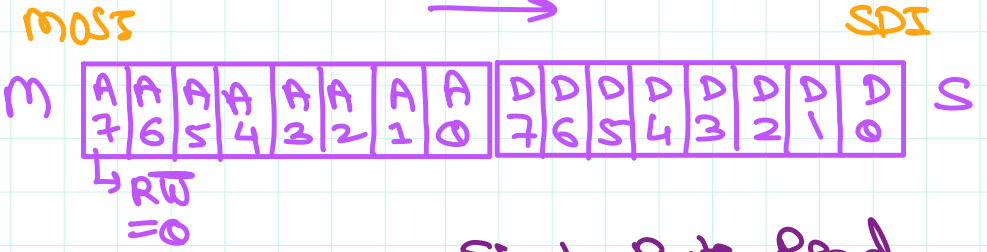↳ 0 = read on leading edge (1st)   1 = read on falling edge (2nd)

CPOL = 0

CPOL = 1

CPHA = 0   CPHA = 1
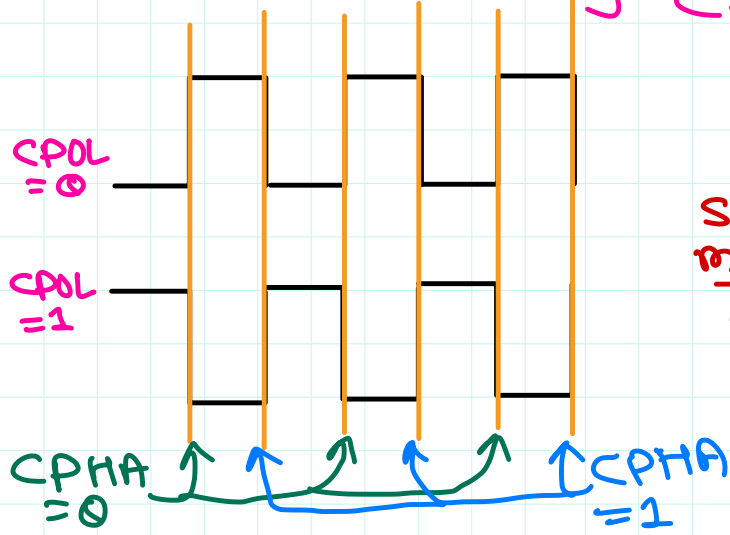
SPI mode	CPOL	CPHA	(sample) read edge	(change) write edge
0	0	0	rising ↑	falling ↓
1	0	1	falling ↓	rising ↑
2	1	0	falling ↓	rising ↑
3	1	1	rising ↑	falling ↑

SPI data frame

LSB First

Tx | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Rx

Single Byte Write

MOSI →   SDI

M | A7 A6 A5 A4 A3 A2 A1 A0 | D7 D6 D5 D4 D3 D2 D1 D0 | S
↳ R/W = 0

Single Byte Read

MOSI →   SDI

M → | A7 A6 A5 A4 A3 A2 A1 A0 | →
↳ R/W = 1

| D7 D6 D5 D4 D3 D2 D1 D0 | ← S
MISO   SDO

after 8 clocks
a b c d e f g h
g h A B C D E F

MOSI SDI

after 8 clocks
A B C D E F G H
G H a b c d e f

MISO SDO

Clock

SCLK SCK

SSEL   CE
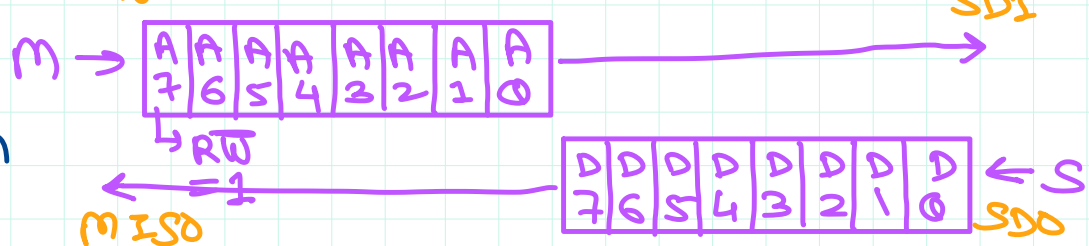
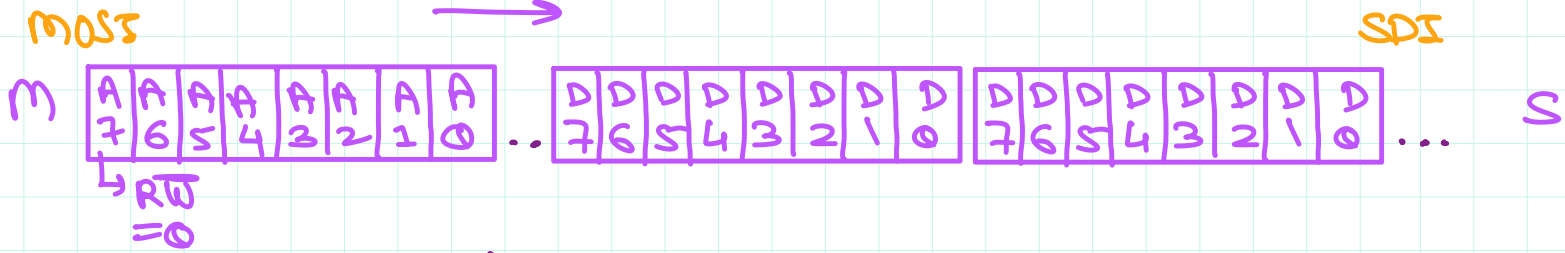Master   Slave
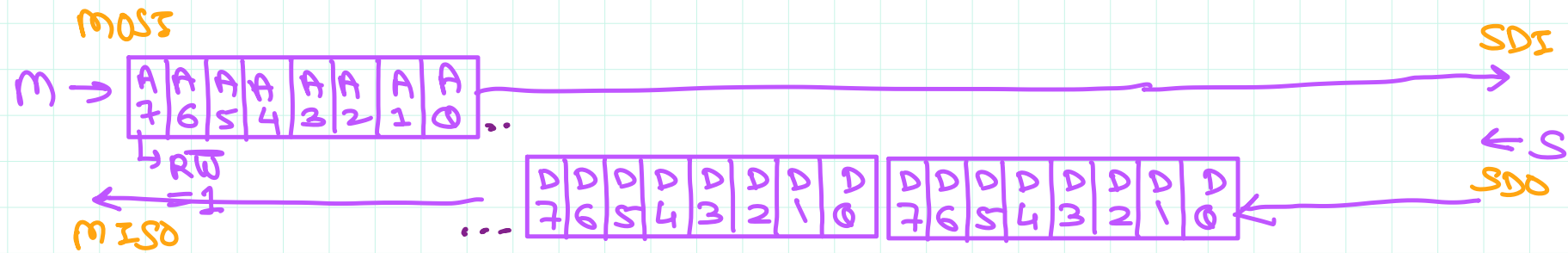
⑩ bit is written (data line change) on first edge of the clock & bit is read (data line sampled) on second edge of the clock.

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Multi Byte Write

MOSI →

SDI

M | A7 A6 A5 A4 A3 A2 A1 A0 | .. | D7 D6 D5 D4 D3 D2 D1 D0 | D7 D6 D5 D4 D3 D2 D1 D0 | ...   S

↳ R/W = 0

Multi Byte Read

MOSI

SDI

M → | A7 A6 A5 A4 A3 A2 A1 A0 | ..

↳ R/W = 1

← S

SDO

MISO ← ... | D7 D6 D5 D4 D3 D2 D1 D0 | D7 D6 D5 D4 D3 D2 D1 D0 |
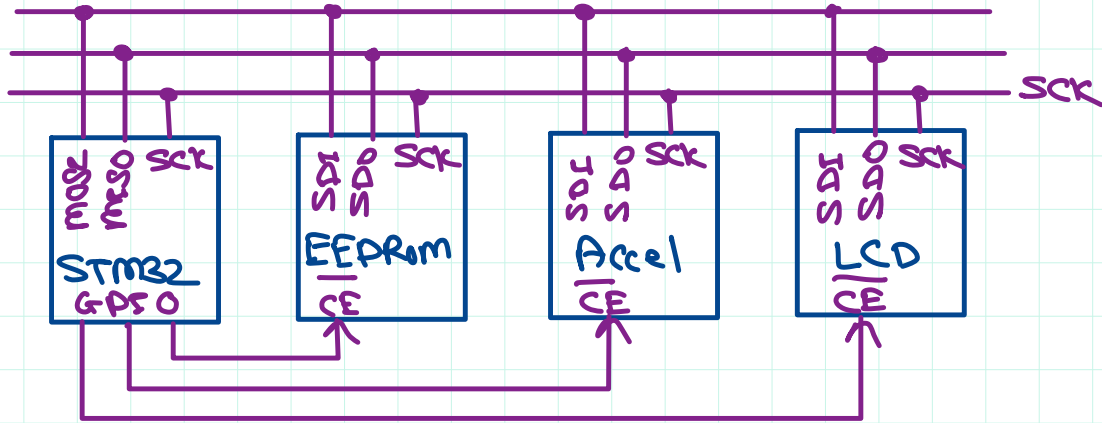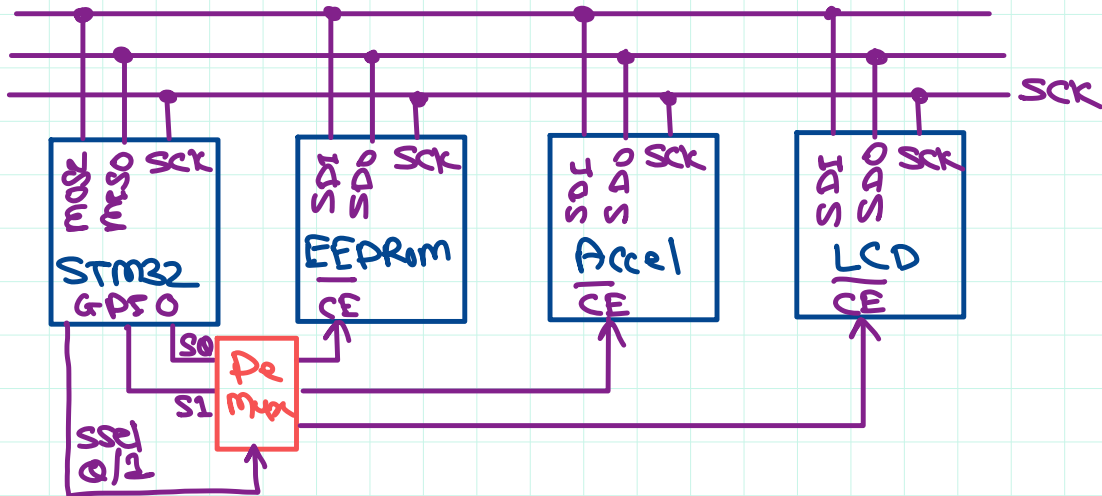
Before master start read/write to slave,
   the slave must be enabled $\overline{CE} / \overline{SS} = 0$
After master finish read/write to slave,
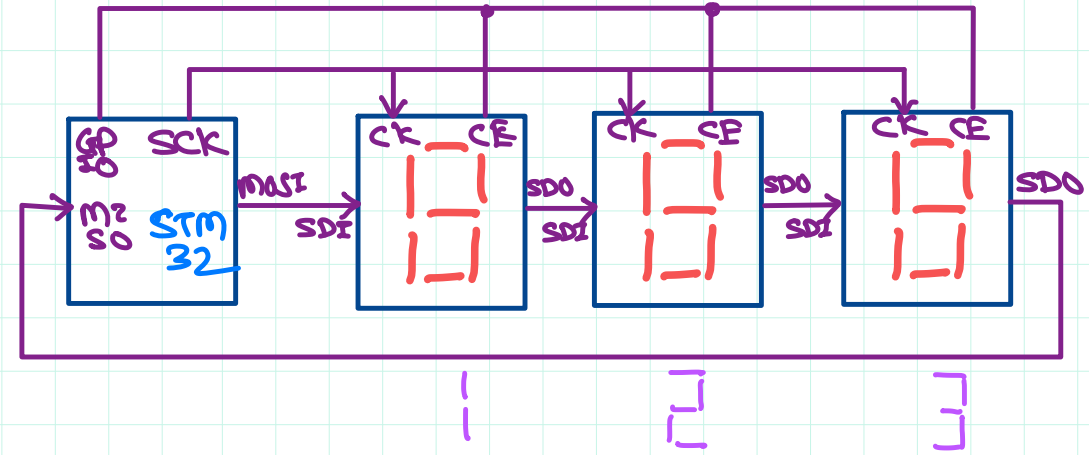   the slave must be disabled $\overline{CE} / \overline{SS} = 1$

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SPI Bus

① Master – one gpio pin for each slave

SCK

STM32
GPIO
MOSI MISO SCK

EEPROM
SDI SDO SCK
CE

Accel
SDI SDO SCK
CE

LCD
SDI SDO SCK
CE

② Master – Use Demux to select slave with fewer GPIO.

SCK

STM32
GPIO
MOSI MISO SCK

EEPROM
SDI SDO SCK
CE

Accel
SDI SDO SCK
CE

LCD
SDI SDO SCK
CE

De mux
S0
S1
SSel 0/1

③ SPI daisy chain

STM32
SCK
MOSI
MISO

CK CE   MOSI   SDI
SDI
SDO

CK CE   SDO   SDI
SDI
SDO

CK CE   SDO
SDI
SDO

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Thank You!

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