



ARM®

Advanced Micro-controllers - ARM

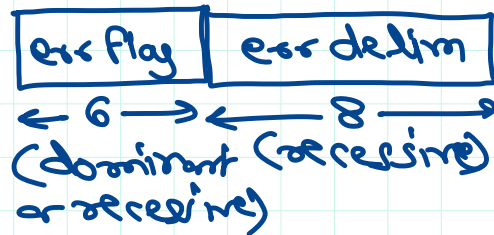
DESD @ Sunbeam Infotech

CAN error handling

- ① error types \rightarrow 5
- Ⓐ CRC Ⓑ Form
 - Ⓒ Ack Ⓓ Bit
 - Ⓔ Stuff

- ② When err is seen by a node, it reports the error \rightarrow CAN err frame.

err frame \rightarrow 14-bits



Overload frame

- looks like err frame



- indicate that device is busy.
- sent during/after IFS.

③ Node States

- CAN errors are counted in each CAN node.

TEC \rightarrow Tx Error Cnt

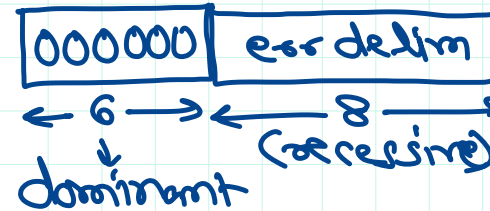
REC \rightarrow Rx Error Cnt

Ⓐ Error Active State. \downarrow

TEC < 128 and Comm'n Okay

REC < 128

Report err as err frame

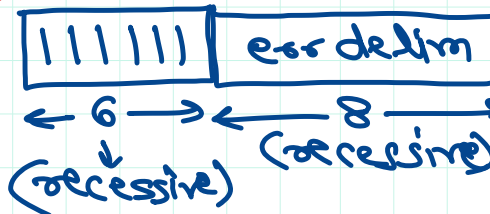


Ⓑ Error Passive State. \downarrow

TEC ≥ 128 or Comm'n Okay

REC ≥ 128

Report err as err frame



* Err frames sent while Rx/Tx of current frame (in-betn).

Ⓒ Bus off

TEC > 255 (threshold)

- Node Comm'n on CAN bus is stopped.

\rightarrow Automatic Recovery

- \rightarrow monitors bus
- \rightarrow 11 recessive $\times 128$ - waiting
- \rightarrow reset TEC & REC

\rightarrow Comm'n start again

\rightarrow manual recovery

- \rightarrow repair faulty node
- \rightarrow reset MCU
- \rightarrow reconnect.

CAN Timing

CAN1 → APB1

CCLK = 72 MHz

PCLK = 36 MHz

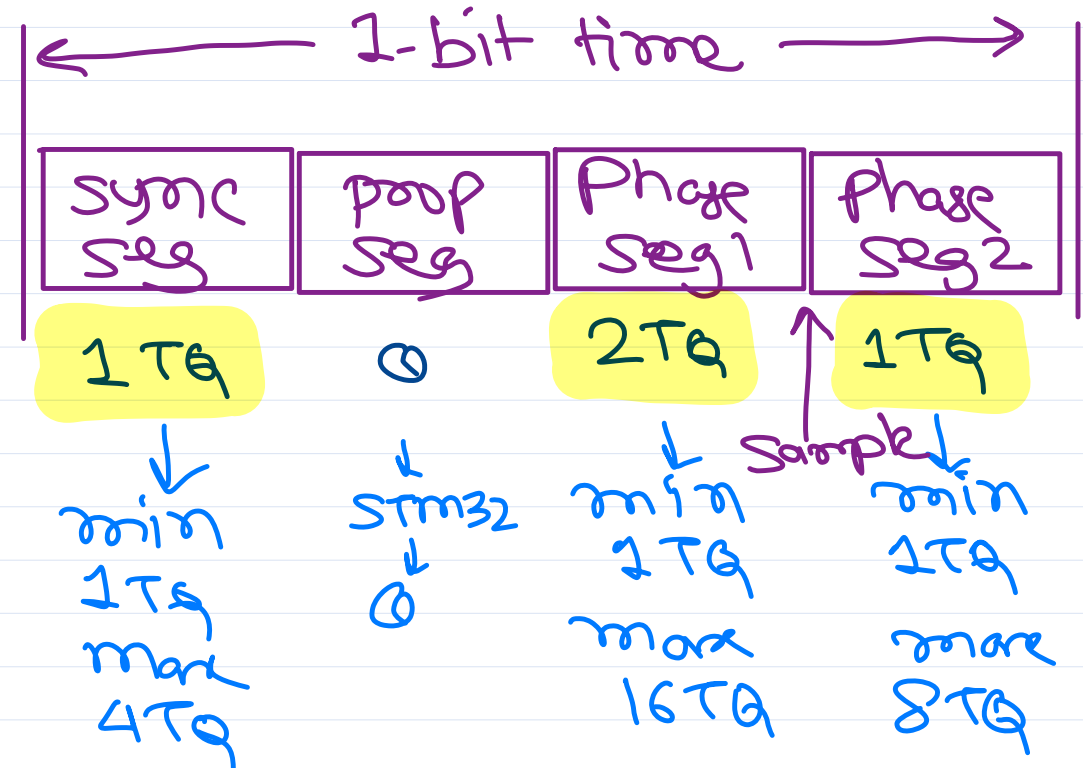
CAN PR = 18 ← (1 to 1024)

$$\text{CAN peri freq} = \frac{\text{PCLK}}{\text{PR}} = \frac{36 \text{ MHz}}{18} = 2 \text{ MHz}$$

$$\begin{aligned} \text{Time Quanta} &= \frac{1}{\text{CAN Peri Freq}} \\ &= \frac{1}{2} \mu\text{s} = 0.5 \mu\text{s} = 500 \text{ ns} \end{aligned}$$

$$\begin{aligned} \text{Nominal Bit Time} &= 1Tq + 2Tq + 1Tq \\ &= 4Tq \\ &= 4 \times 500 \text{ ns} = 2 \mu\text{s} \end{aligned}$$

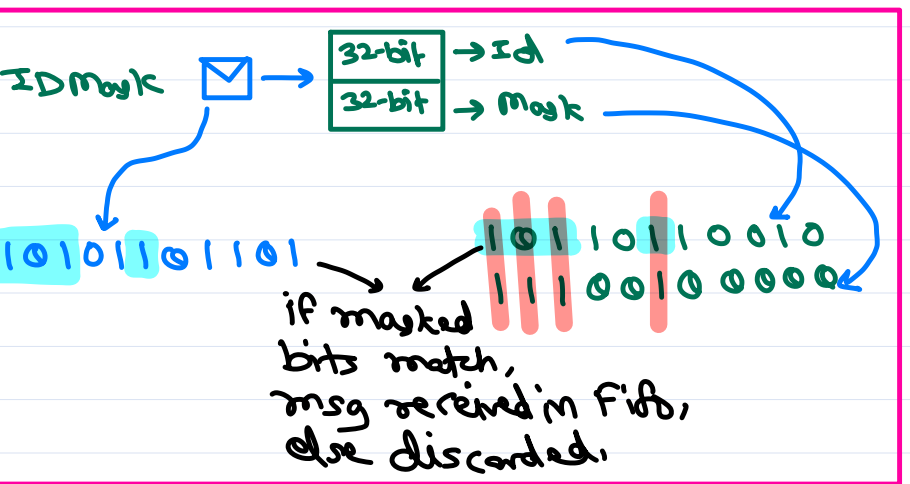
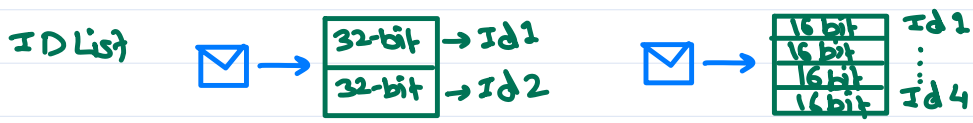
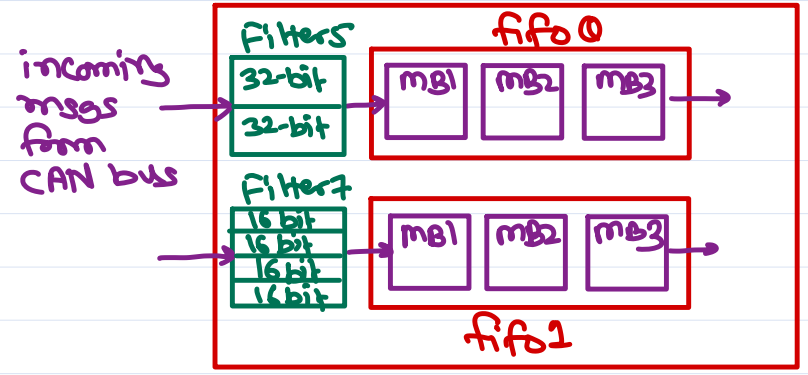
$$\text{CAN o/p bit rate} = \frac{1}{2} \text{ MHz} = 0.5 \text{ MHz}$$



CAN

Acceptance Filter

STM32 CAN



Acceptance Filter Config: 32-bit ID Mask

e.g. ID (to comp) → 0x0A8: 000 1010 1000
mask (bits to comp) → 0x7F8: 111 1111 1000

e.g. incoming msg id: 0x0A8 → 000 1010 1000
0A9 → 000 1010 1001
0AA → 000 1010 1010
0AB → 000 1010 1011
0AC → 000 1010 1100
0AD → 000 1010 1101
0AE → 000 1010 1110
0AF → 000 1010 1111
0A5 → 000 1010 0101

accepted.

not accepted

Time Management

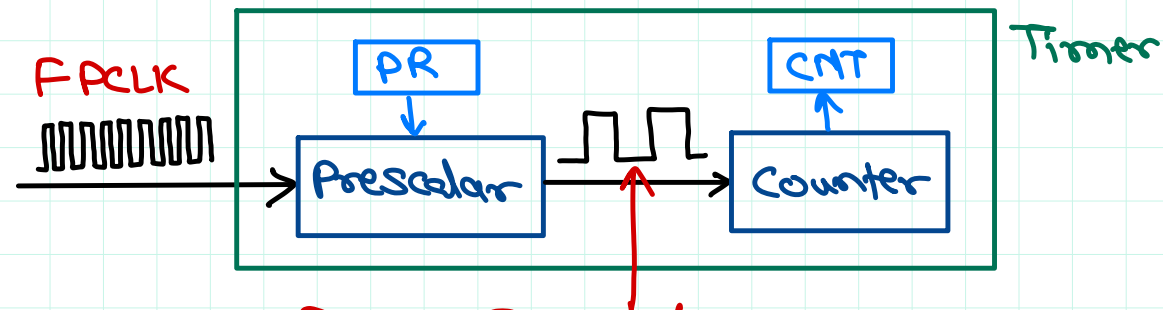
Absolute Time

a.k.a. Wall time

- calendar date & clock time
- Hw: RTC

Relative time

- Time w.r.t. Event
- Hw: SysTick
 - STM32 Timers
 - Basic/Advanced
 - 16-bit/32-bit
 - WDT
 - DWT (Debug Timer)



$$Freq = FPCLK / PR \text{ Hz.}$$

$$Period = \frac{PR}{FPCLK} \text{ sec}$$

Example 1: $FPCLK = 16 \text{ MHz}$, $PR = 16$, $CNT = 1000$, $time = ?$

$$time = period \times CNT = \frac{PR}{FPCLK} \times CNT$$

$$= \frac{16}{16000000} \times 1000 = \frac{1}{1000} \text{ sec} = 1 \text{ ms}$$

$$time = \frac{PR}{FPCLK} \times CNT \times 1000 \text{ ms}$$

$$CNT = \frac{time_ms}{1000} \times \frac{FPCLK}{PR}$$

$$CNT = \frac{FPCLK}{1000} \times \frac{time_ms}{PR}$$

Timer vs Counter

Counter: Ckt that counts ext. pulses/edges

Timer: is a counter that counts pulses with a fixed freq. Usually timer hw also produces intrs.



Thank You!

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