EXPERIMENT - II

ANALYSIS OF FULL AND HALF ADDERS AND SUBTRACTORS USING LT SPICE

SLOT: L37+L38

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EXPERIMENT - II

	AIM:
	To analyse the Address and Subtractions in LT spice and verify theoretical outputs with simulated outputs.
_	Hoterials Required Latest version of LT Spice on with The (Digital Logic) Library.
Up.	PRE-PREQUIST KNOWLEDGE .
	depending on the input from the voltage source.
	How to construct and use Halt and full adder and subtraction.
	How to use LT spice and install the necessary libraries.
	Brocedure:
	Download and install It spice with the correct libraries
2.	Once operational create a new simulation profile and name it
3.	Drag and drop all necessary components to complete the circuit
4.	completed make sure to add ground and voltage sources. Configure the voltage sources as such.
	a. yo to advance settings and select PUISE as the function. (. Vinitial =0
	ji . Ven - 5
	iii. Vdelay = 0 N. Toise = In
	v. Tfall = in
	vi. And depending on number of inputs 1. First input
	a. Tfall = im

	b. Ton - 2m
	2. Second input
- 1	a. Tfall = Im
-	b. Ton = 2m
	3. Third input
	a. Tfall = 4m
	b. Ton = 8m
(1)	and the same of the same of the same of the same
	b. Connect them accordingly and make sure to ground all
5.	Once done sum a simulation under trans for com and plot all corresponding values.
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-	THEORY: Was Mary was a said and the said and the said
J.	Ciauit that takes the logical decision and the process are
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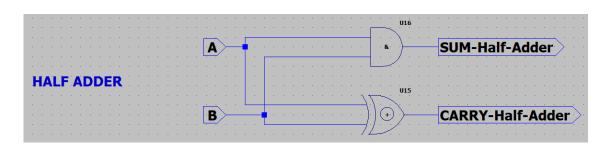
ADDER:

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							imposet		
th	e co	mputer	but	also in	many	types	of dig	ital sy	tems in
wh	ich .	tue re	meric.	data	are n	Accessed	1	0	

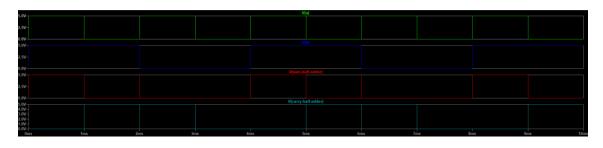
HALF ADDER:

TI.	ADDER:	1.1.	alel men	6	
ine.	may an	des_ecce	pto two	binary digits	on its inputs
and_	-produce	_two_	pinary di	its output,	a sum bit
and	a carre	y bit 7	re hall	adder in an	example of a
simp	le Juni	tional a	digit our	with hailt d	on two loois
onten	. T. h	11 000	all t	are only	com two logic
7	and to	y dade	adds 16	one-bit bu	nony rumbers (A
/he	output_	is the	sum of the	re two bits cs	and carry (c)
					0
	Α	•	M	-	
) xox	-5	
1 -	В				
			1 0	2	Α
_				0	- 0
	()	A	ND	C	0
			7 9		0
		В	Sum	Carry-out	0.4
	A				
	0	0	0	0	
	0	0	0	0	
	1	0 1	1 1	0	

SCHEMATIC DIAGRAM:



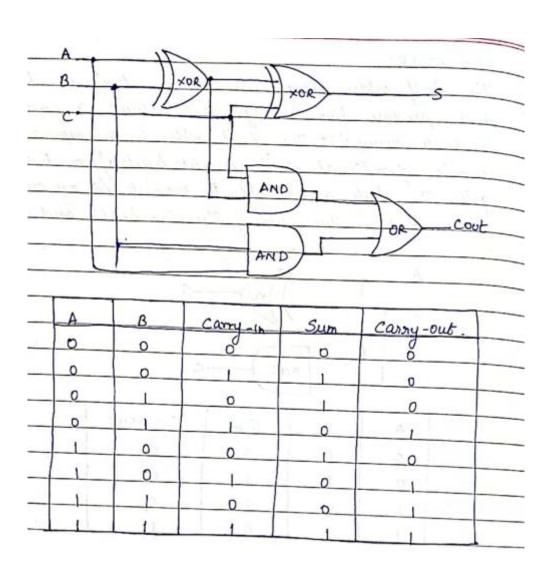
OUTPUT WAVEFORMS



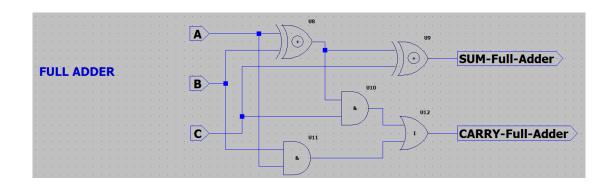
FULL ADDER:

FULL- ADDER:

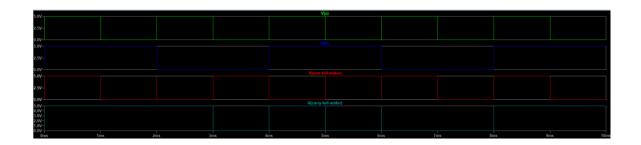
The full adders accepts two inputs bits and an input carry and generates a sum output and an output carry. The full-adder circuit adds three one-bit binary rumbers (Cim, A, B) and outputs two one-bit binary rumbers, a sum (s) and a carry (cout). The full-adder is usually a component in a cascade of adders, which add 8, 16, 32 etc. binary numbers. If you look storely, you'll see the full adder is simply two half adders joined by an OR.



SCHEMATIC DIAGRAM:



OUTPUT WAVEFORMS

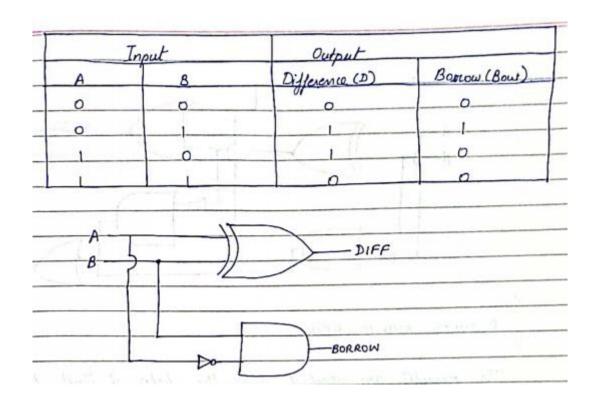


SUBTRACTOR

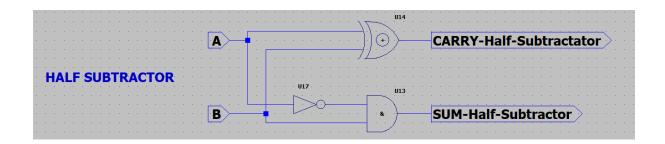
Subtractor to an electronic logic circuit for calculating the difference between two binary rumbers which provides the difference and borrow as output:

HALF-SUBTRACTOR:

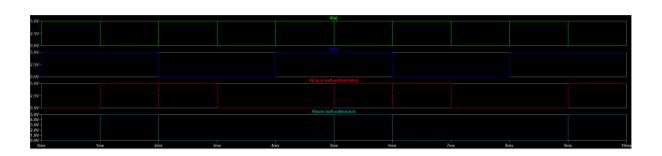
-	HALF SUBTRACTOR
	Half subtractor is used for subtracting one single but
1	binary number from another single bit binary rumber. It
	has two must me single bit binary rumber It
	The state of and suite is all all
	two outputs: Difference (D) and Barrow (Bout)
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SCHEMATIC DIAGRAM:

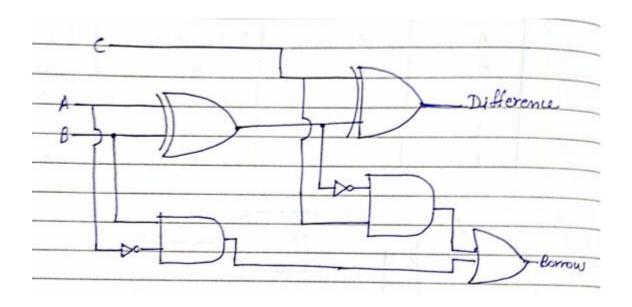


OUTPUT WAVEFORMS

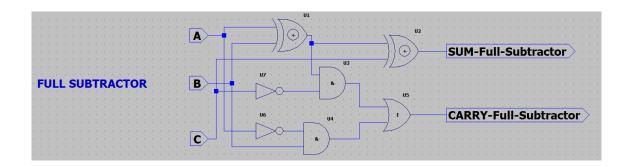


FULL SUBTRACTOR:

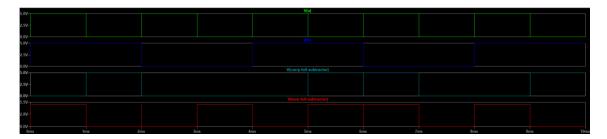
FULL SUBTI	RACTOR:		Vallent :			
A logic bit bind inputs; M	circuit which	is known of ubtahend (as Full Suc B) and foll	acting Horse so Litraction. It he lowing Subtrah (Bout)	as House	
	Input		Οω			
A_	B		D	B (out)		
	0	0	0	0		
	0			1		
		0	1	1		
			o	1		
	0			О		
	0			00		
	1		0	0	-	



SCHEMATIC DIAGRAM:



OUTPUT WAVEFORMS



RESULTS AND INFERENCE:

The results are verified with the help of truth tables and LT SPICE results and hence the logic gates are verified.