EXPERIMENT - V

ANALYSIS OF COMBINATIONAL LOGIC CIRCUITS FOR 2:1 MULTIPLEXER AND D & T FLIP FLOP

SLOT: L37 + L38

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AIM

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To design a combinational logic current circuit for a 2:1 Multiplexer and T flip flop.

MATERIALS

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Latest version of LT Spice with the [Digital Logic] Library.

PRE-REQUISITES

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Know how logic gates, combinational circuits work and how the output varies depending on the input from the voltage source.

How to construct and operate decoders, multiplexers and encoders

How to use LT spice and install the necessary libraries.

PROCEDURE

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1. Download and install LT Spice with the correct libraries.
2. Once operational create a new simulation profile and name it.
3. Drag and drop all necessary components to construct the circuit, once completed.
4. Go to advance settings and select PULSE under functions for Voltage sources Clock, D-Input, D_0, D_1 and S.
   - I. V(initial) = 0
   - II. V(on) = 5
   - III. T(rise) = 1n
   - IV. T(fall) = 1n

v. And depending on name of inputs.

a. Clock

i = V(delay) = 1m

ii. - T(on) = 1m

iii. T(period) = 2m

b. D-Input

i. V(delay) = 1m

ii. T(on) = 4m

iii. T(period) = 10m

c. Do Input

i. V(delay) = 1m

ii. T(on) = 4m 1m

iii. T(period) = 2+0m

d. Dφ Input

i. V(delay) = 2m

ii. V(on) = 2m

iii. T(period) = 2m

e. S Input

i. V(delay) = 4m

ii. T(on) = 4m

iii. T(period) = 8m

f. Reset-TFF Input

i. V(delay) = 8m

ii. T(on) = 8m

iii. T(period) = 16m

g. Clock-TFF Input

(i). V(delay) = 1m

ii T(on) = 1m

iii T(period) = 2m

h. T-Input

i. V(delay) = 4m

ii. T(on) = 4m

iii. T(period) = 8m

VI. Connect all of them accordingly using the appropriate labels and make sure to ground all negative ends of the voltage sources.

5. For Voltage source Reset.

a. V = 5

6. Once done run the simulation under trans for 10m plot the output wave forms in three separate plots.

a. D Flip Flop

i. Input plots

1. D-Input

2. Clock

3. Reset

ii. Output plots

1. Q

2. Q_0

b. 2:1 Multiplexer

1. Input plots

1. D_0 input

2. D_1 input

3. S-input

ii. Output plots

1. Y output

c. T Flip Flop.

i. Input plots

1. T- Input

2. Clock - TFF

3. Reset - TFF

ii. Output plots

1. Q_1

2. Q_{10}

THEORY

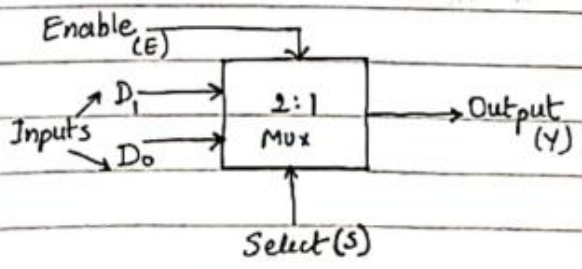
MULTIPLEXER

Multiplexer is a combinational circuit that has maximum of 2^n data inputs. 'n' selection lines and single output line. One of these data inputs will be connected to the output based on the values of of selection lines.
Since there are 'n' selection lines, there will be 2^n possible combinations of zero's and ones. So, each combination will select only one data input. Multiplexer is also called as Mux.

2X1 MULTIPLEXER

A 2-to1 multiplexer consists of two inputs Do and D_1, one select input S and one output Y. Depending on the select signal, the output is connected to either of the inputs. Since there are two input signals, only two ways are possible to connect the inputs to the outputs. so one select is needed to do these operations.

If the select line is low, then the output will be switched to Do input, whereas if select line is high, then the output will be switched to D_1 input. The figure below shows the block diagram of a 2-to1 multiplexer which connects two 1-bit inputs to a common destination.



The truth table of the 2-to-1 multiplexer is shown below. Depending on the value of the select input, the inputs i.e. D_0, D_1 are produced at outputs. The output is D_0 when Select value is $S=0$ and the output is D_1 when Select value is $S=1$.

S	D_0	D_1	Y
0	0	x	0
0	1	x	1
1	x	0	0
1	x	1	1

"X" in the above truth table denotes a don't care condition. So, ignoring the don't care conditions, we can derive the Boolean Expression of a typical 2 to 1 Multiplexer as follows.

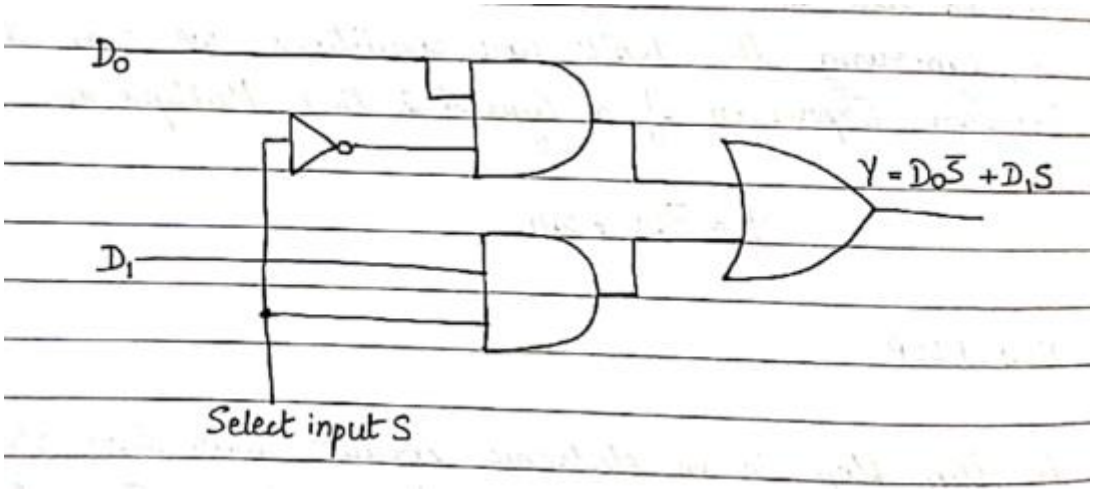
$$Y = \bar{S}D_0 + SD_1$$

FLIP FLOP

A flip-flop is an electronic circuit with two stable states that can be used to store binary data. The stored data can be changed by applying varying inputs. Flip-Flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems. Flip-Flops and latches are used as data storage elements. It is the basic storage element in sequential logic. But first, let's clarify the difference between a latch and flip-flop.

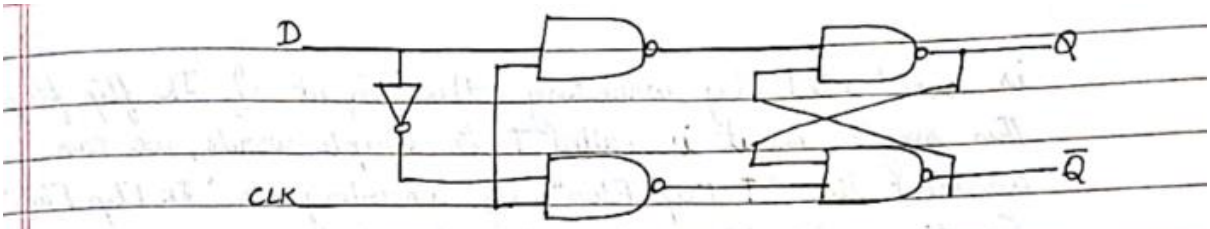
From the above output expression, the logic circuit of 2-to-1 multiplexer can be implemented using logic gates as shown in figure. It consists of two AND gates, one NOT gate and one OR gate. When the select line, S=0, the output of the lower AND gate is zero, but the output of upper AND gate is D_0. Thus, the output generated by the OR gate is equal to D_0.

Similarly, when S=1, the output of the upper AND gate is zero, but the output of lower AND gate is D_1. Therefore, the output of the OR gate is D_1. Thus, the above given Boolean expression is satisfied by this circuit.



D FLIP FLOP

The D Flip Flop is by far the most important of the clocked flip-flops as it ensures that inputs S and R are never equal to one at the same time. The D-type flip-flop are constructed from a gated SR flip-flop with an inverter added between the S and the R inputs to allow for a single D (Data) input.



In a D flip flop, the output can be only changed at the clock edge, and if the input changes at other times, the output will be unaffected.

Clock	D	Q	Q'
↓ »0	0	0	1
↑ » 1	0	0	1
↓ »0	1	0	1
↑ »1	1	1	0

The change of state of the output is dependent on the rising edge of the clock. The output (Q) is same as the input and can only change at the rising edge of the clock.

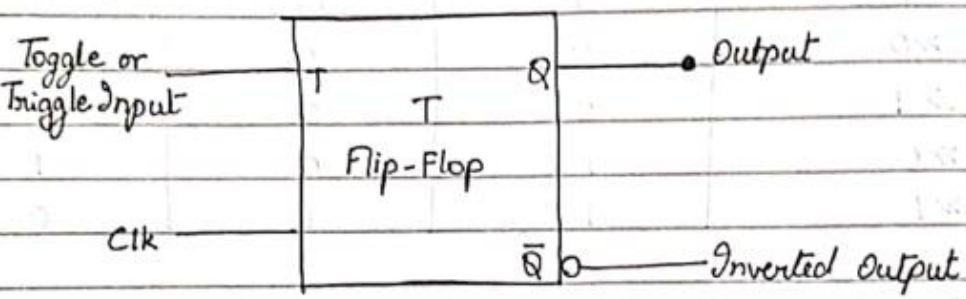
T FLIP FLOP

In T flip flop, "T" defines the term "Toggle". In SR FLIP FLOP, we provide only a single input called "Toggle" or "Trigger" input to avoid an intermediate state occurance. Now, this flip-flop works as a Toggle switch. The next output state is changed with the complement of the present state output. This process is known as "Toggling".

We can construct the "T Flip Flop" by making changes in the "JK Flip Flop". The "T Flip Flop" has only one input which

is constructed by connecting the input of JK flip flop. This single input is called T. In simple words, we can construct the "T Flip Flop" by converting a "JK Flip Flop". Sometimes the "T Flip Flop" is reffered to as single input "JK Flip Flop".

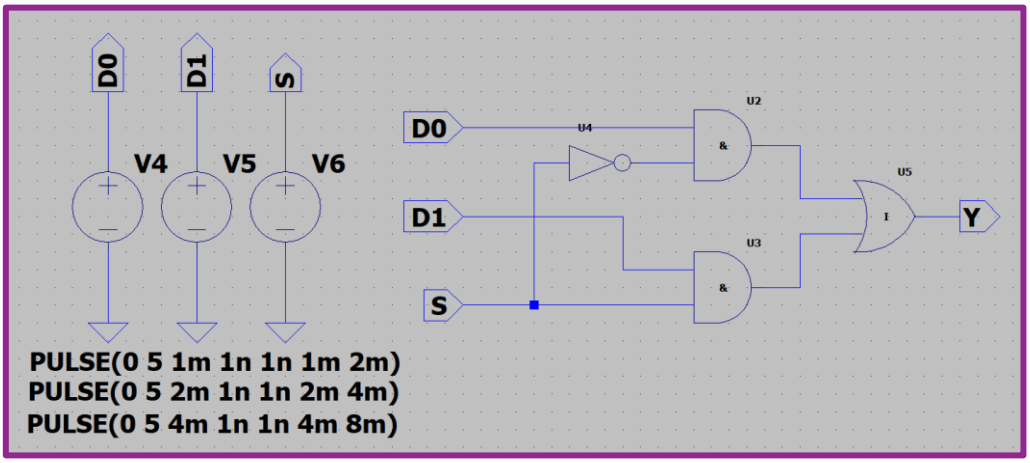
Block diagram of the "T-Flip Flop" is given where T defines the "Toggle input", and CLK defines the clock signal input.



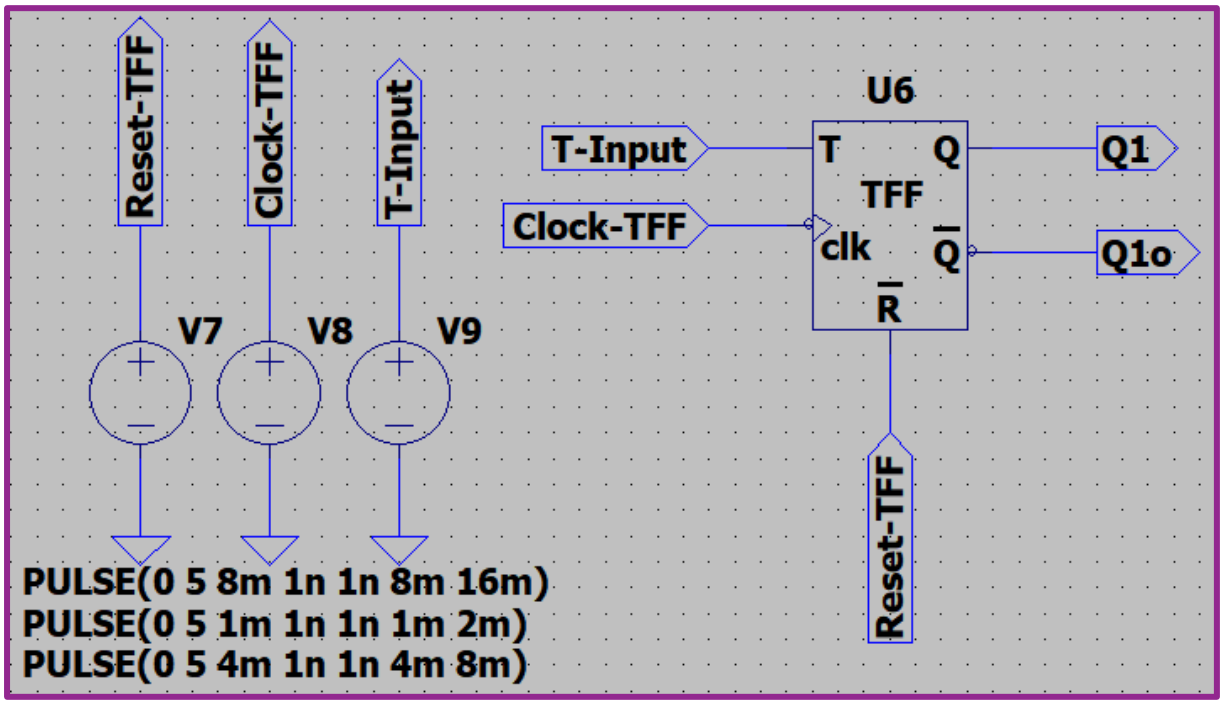
	Previous		Next	
T	Q	Q'	Q	Q'
0	0	1	0	1
0	1	0	1	0
1	0	1	1	0
1	1	0	0	1

SCHEMATIC DIAGRAM

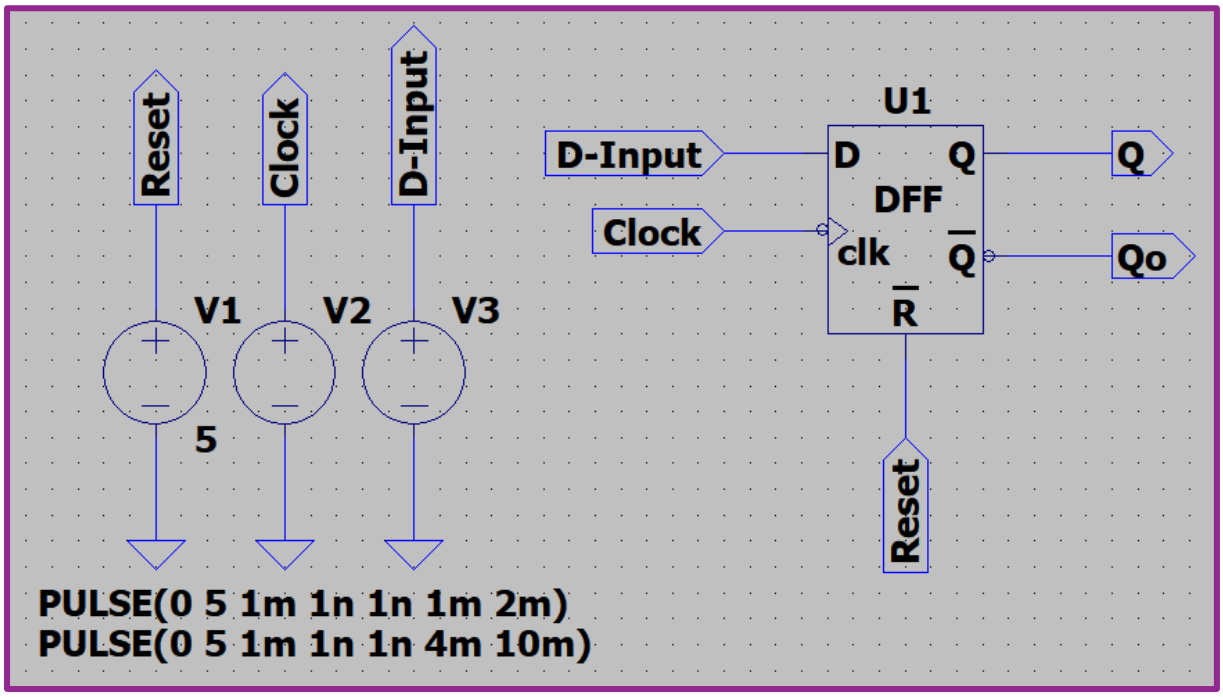
2:1 MULTIPLEXER



T FLIP FLOP

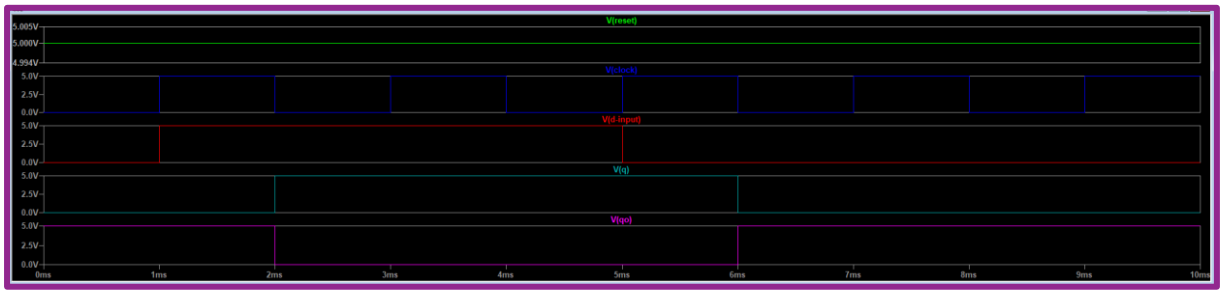


D FLIP FLOP

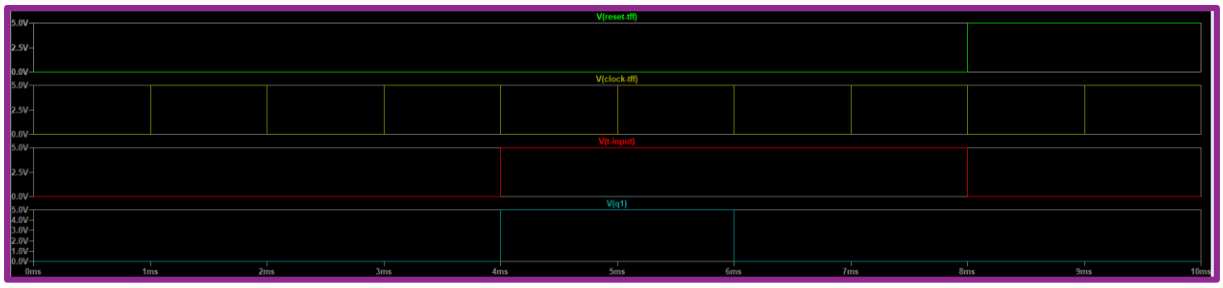


OUTPUT WAVEFORMS

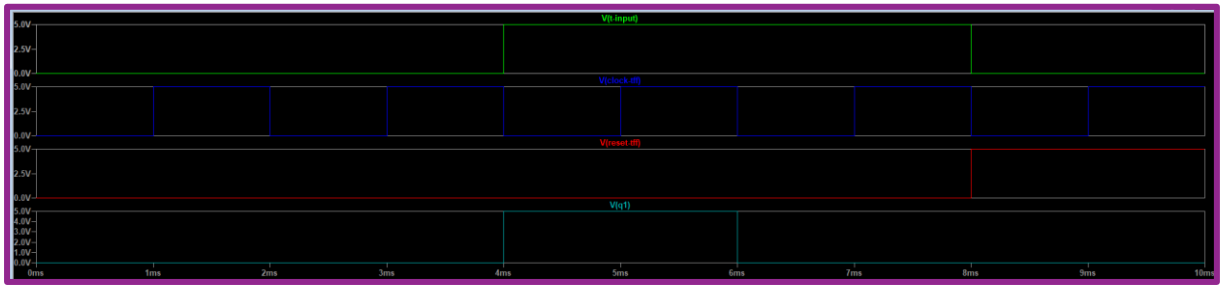
2:1 MULTIPLEXER



D FLIP FLOP



T FLIP FLOP



RESULTS AND INFERENCE:

The results are verified with the help of truth tables and LT SPICE results and hence the 2:1 Multiplexer and D Flip Flop are verified.