EXPERIMENT - VI

ANALYSIS OF LOGIC CIRCUITS OF MEALY SEQUENCE DETECTOR

SLOT: L37 + L38

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AIM

To design a logic circuit for a Mealy Sequence Detector and T flip flop

MATERIALS

Latest version of LT Spice with the [Digital Logic] Library and the necessary input and output data signals for construction and verification

PRE-REQUISITES

Know how logic gates, combination circuits work and how the output varies depending on the input from the voltage source.

How to construct and the mealy sequence detector.

How to use LT spice and install the necessary libraries.

PROCEDURE

1. Download and install LT Spice with the correct libraries
2. Once operational create a new simulation profile and name it.
3. Drag and drop all necessary components to construct the circuit, once completed
4. Go to advance settings and select PULSE under functions for Voltage sources Clock and X
    I. V(initial) = 0
    II. V(on) = 5
    III. T(rise) = 1n
    IV. T(fall) = 1n
    V. And depending on name of inputs
        a. X-Input
            i. V1
                1. V(delay) = 2m
                2. T(on) = 2m
                3. T(period) = 4m
                4. N(cycles) = 1
            ii. V2
                1. V(delay) = 5m
                2. T(on) = 2m
                3. T(period) = 4m
                4. N(cycles) = 1
            iii. V3
                1. V(delay) = 9m
                2. T(on) = 1m
                3. T(period) = 2m
                4. N(cycles) = 1
        b. Clock
            i. V(delay) = 1m
            ii. T(on) = 1m

iii. T(period) = 2m

VI. Connect all of them accordingly using the appropriate labels and make sure to ground all negative ends of the voltage sources.

5. Once done run the simulation under trans for 10m plot the output waveforms in three separate plots.
   a. X – Data Input
   b. Clock
   c. Z data output

THEORY

SEQUENCE DETECTOR

A **sequence detector** is a sequential state machine that takes an input string of bits and generates an output 1 whenever the target sequence has been detected. In a Mealy machine, output depends on the present state and the external input (x). Hence, in the diagram, the output is written outside the states, along with inputs. Sequence detector is of two types:

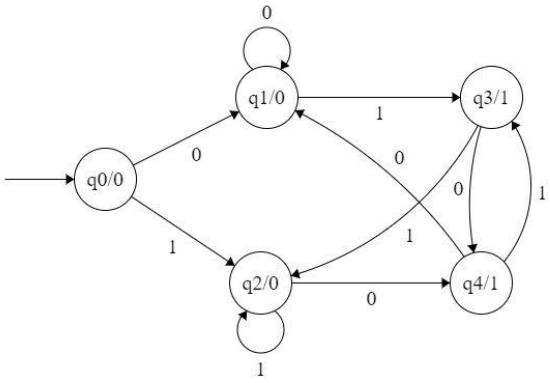
1. Overlapping
2. Non-Overlapping

In an overlapping sequence detector, the last bit of one sequence becomes the first bit of the next sequence. However, in a non-overlapping sequence detector, the last bit of one sequence does not become the first bit of the next sequence. In this post, we'll discuss the design procedure for non-overlapping 101 Mealy sequence detectors.

MEALY AND MOORE MACHINES

Moore machines are finite state machines with output value and its output depends only on present state. It can be defined as (Q, q0, ∑, O, δ, λ) where:

- Q is finite set of states.
- q0 is the initial state.
- ∑ is the input alphabet.
- O is the output alphabet.
- δ is transition function which maps Q×∑ → Q.
- λ is the output function which maps Q → O.

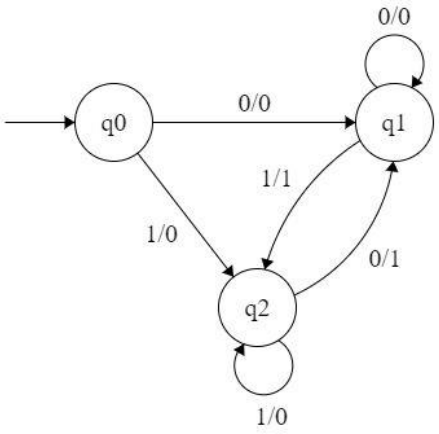


In the moore machine shown in Figure 1, the output is represented with each input state separ ated by /. The length of output for a moore machine is greater than input by 1.

- **Input:** 11
- **Transition:** δ (q0,11)=> δ(q2,1)=>q2
- **Output:** 000 (0 for q0, 0 for q2 and again 0 for q2)

Mealy machines are also finite state machines with output value and its output depends on present state and current input symbol. It can be defined as (Q, q0, ∑, O, δ, λ') where:

- Q is finite set of states.
- q0 is the initial state.
- ∑ is the input alphabet.
- O is the output alphabet.
- δ is transition function which maps Q×∑ → Q.
- 'λ' is the output function which maps Q×∑→ O.



In the mealy machine shown in Figure 1, the output is represented with each input symbol for each state separated by /. The length of output for a mealy machine is equal to the length of input.

- **Input:**11
- **Transition:** δ (q0,11)=> δ(q2,1)=>q2
- **Output:** 00 <q0 to q2 transition has Output 0 and q2 to q2 transition also has Output 0>

Design a sequence detector to detect the input sequence ending in 101. It will produce an output of Y = 1 coincident with the last 1. The circuit does not reset when a 1 output occurs.

A typical input sequence and the corresponding output sequence are:

X= 00110110010 1 0 1 0 0

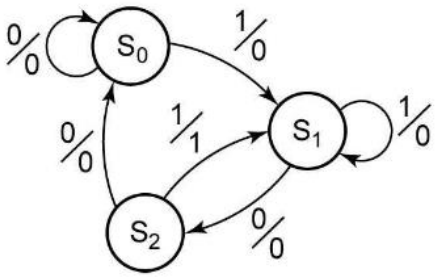
Y: 00000100000 1 0 1 0 0

Initially, we do not know how many flip-flops will be required, so we will designate the circuit states as 50, 51, etc.

We will start with a reset state designated 50.

If a 0 input is received, the circuit can stay in 50 because the input sequence we are looking for does not start with a 0.

Mealy state diagram:

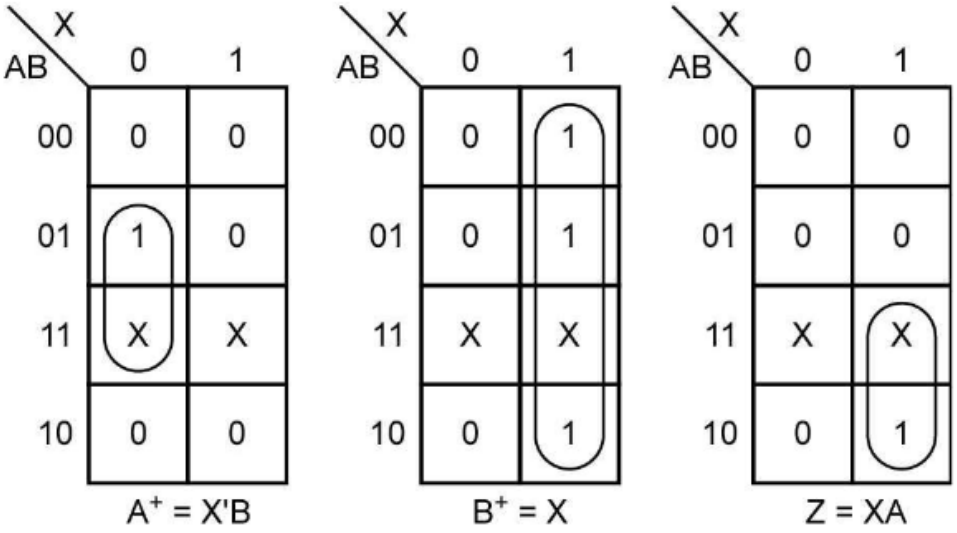


State Assignment:
S0 = 00
S1 = 01
S2 = 10

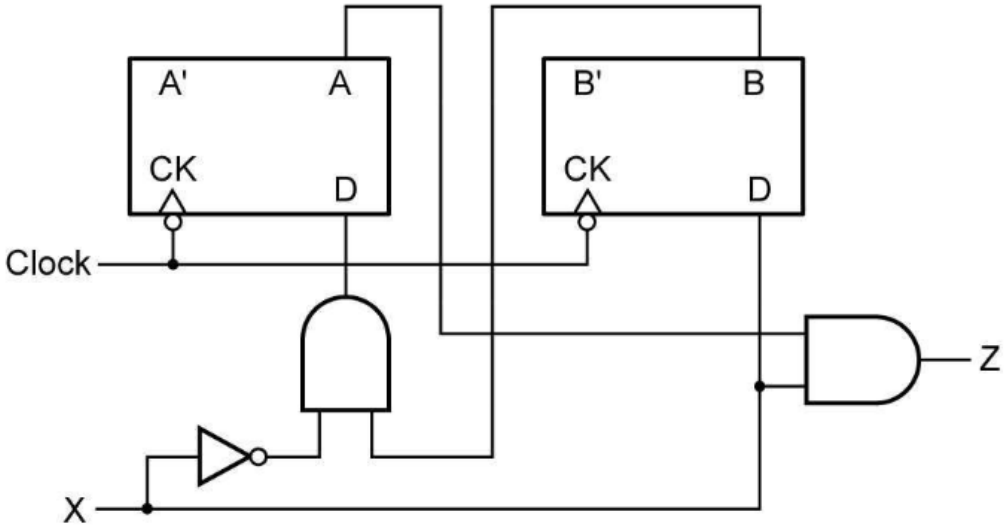
Present State	Next State $X=0$	Next State $X=1$	Present Output $X=0$	Present Output $X=1$
S_0	S_0	S_1	0	0
S_1	S_2	S_1	0	0
S_2	S_0	S_1	0	1

AB	A^+B^+ $X=0$	A^+B^+ $X=1$	Z $X=0$	Z $X=1$
00	00	01	0	0
01	10	01	0	0
10	00	01	0	1

- Derive the FF input and output equation. Choose DFF.

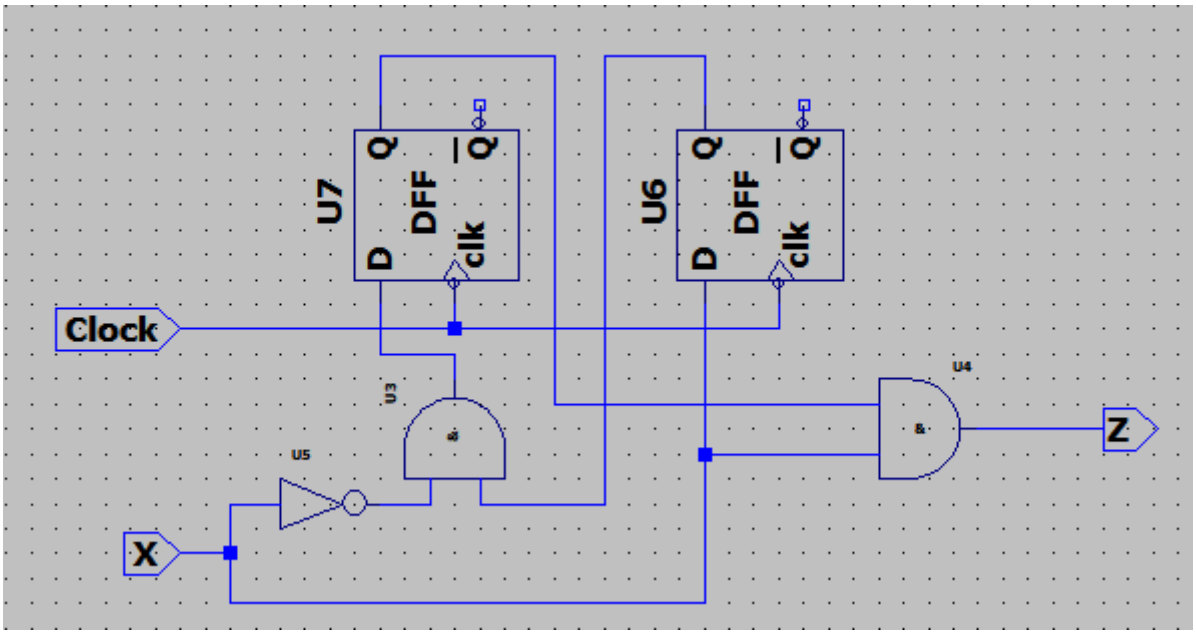


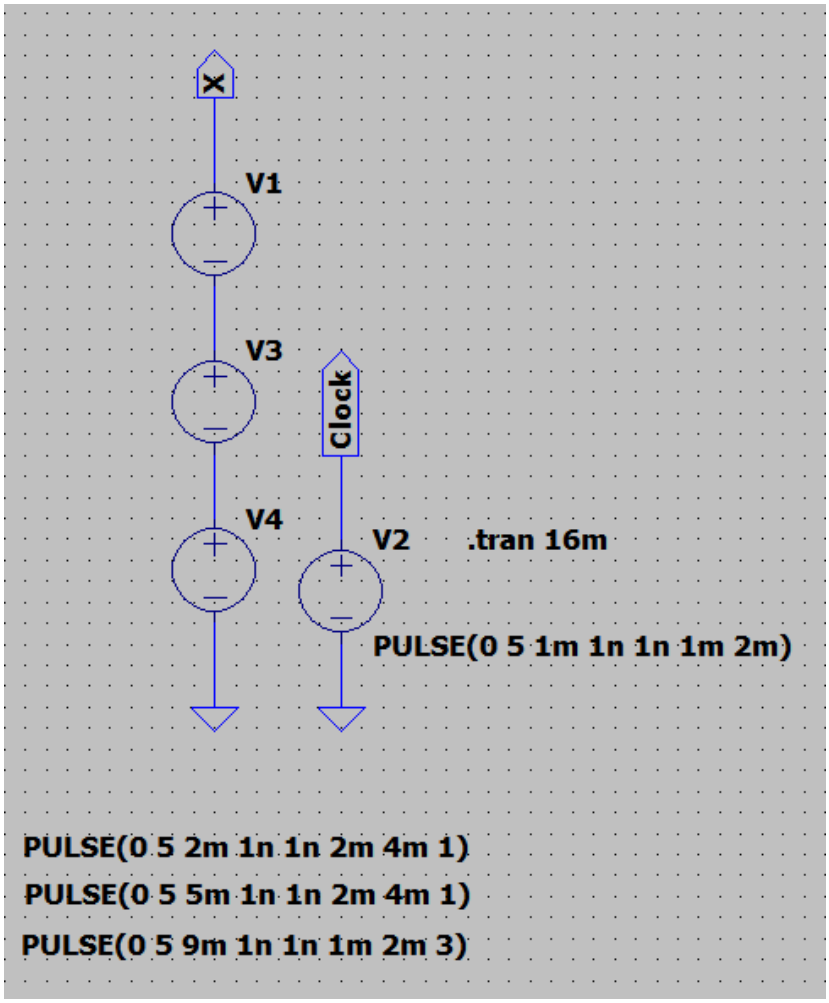
Logic diagram:



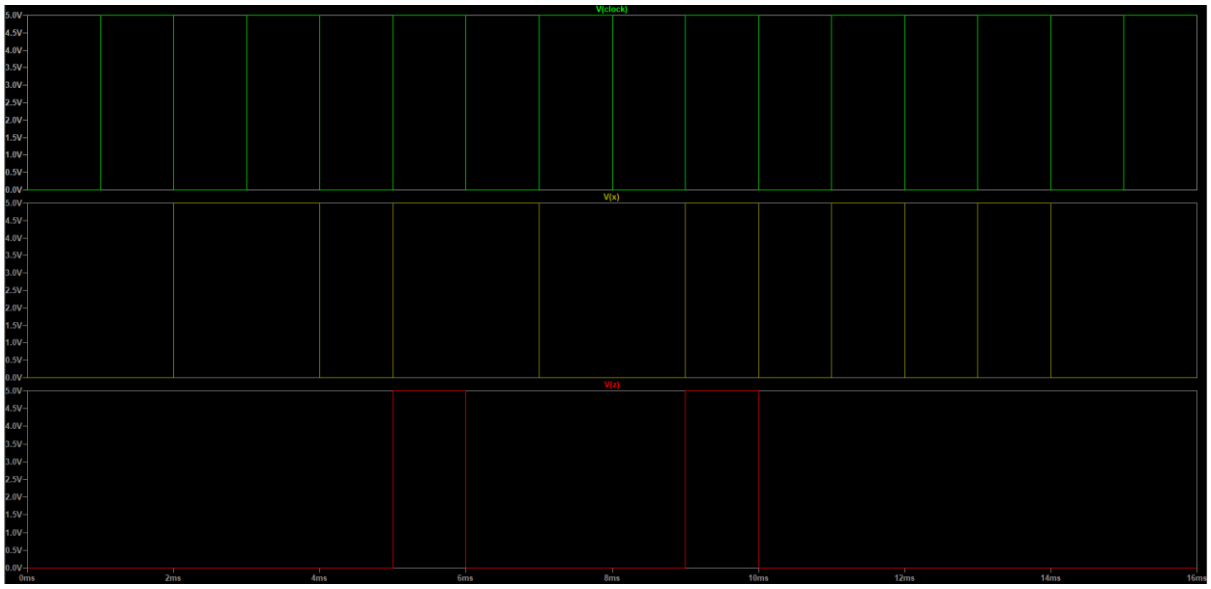
SCHEMATIC DIAGRAM

MEALY SEQUENCE DETECTOR





OUTPUT WAVEFORMS



RESULTS AND INFERENCE

The results are verified with the help of truth tables and LT SPICE results and hence the mealy sequence detector is verified.