EXPERIMENT - I

ANALYSIS OF ALL LOGIC GATES IN LT SPICE, AND VERIFYING THEM

SLOT: L37+L38

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EXPERIMENT - IA

AIM:

To analyse the logic gates in LT spice and verify theoretical outputs with simulated outputs.

MATERIALS REQUIERED

Latest version of LT Spice with the [Digital Logic] Library.

PRE-REQUIST KNOWLEDGE:

Know how logic gates work and how the output varies depending on the input from the voltage source.

How to use LT spice and install the necessary libraries.

THEORY:

Circuit that takes the logical decision and the process are called logic gates. Each gate has one or more input and only one output. OR, AND and NOT are basic gates. NAND, NOR and X-OR are known as universal gates. Basic gates form these gates.

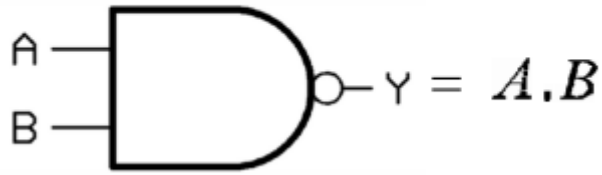
AND GATE:

The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low level when any one of the inputs is low.

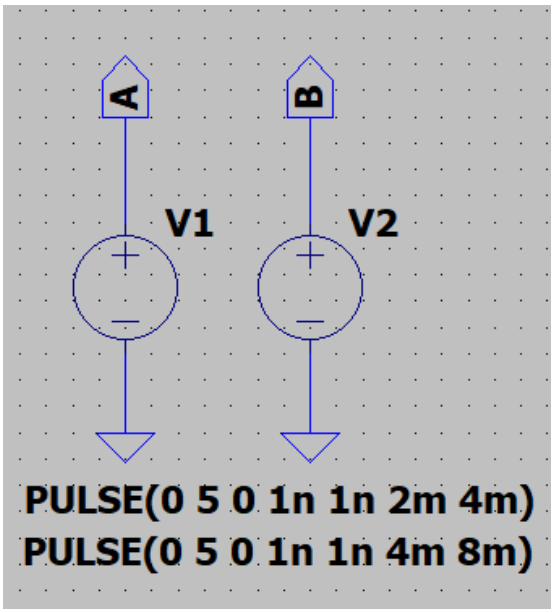
LT SPICE TRUTH TABLE AND BOOLEAN EXPRESSION:

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

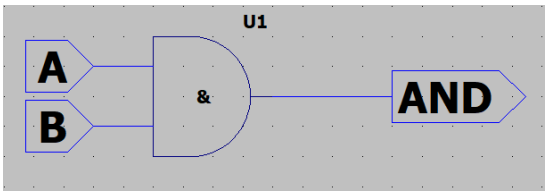
SYMBOL



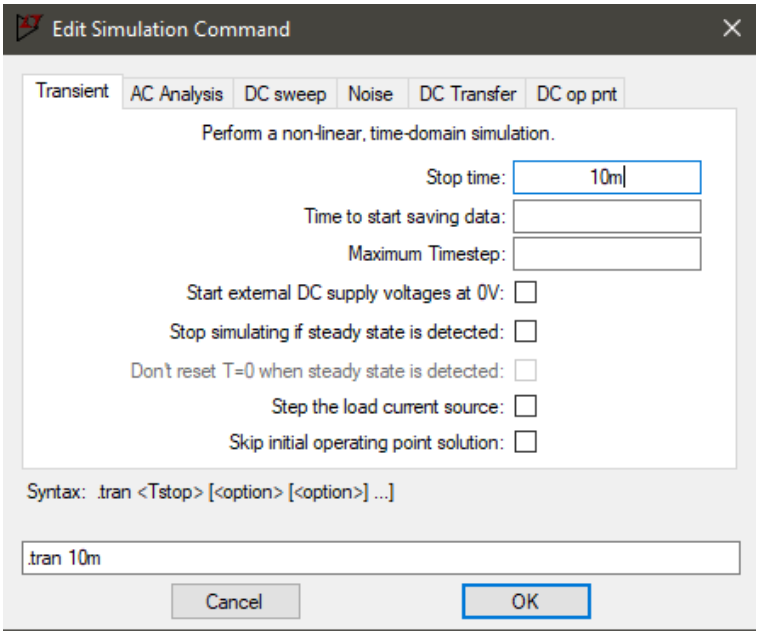
LT SPICE VOLTAGE INPUT:



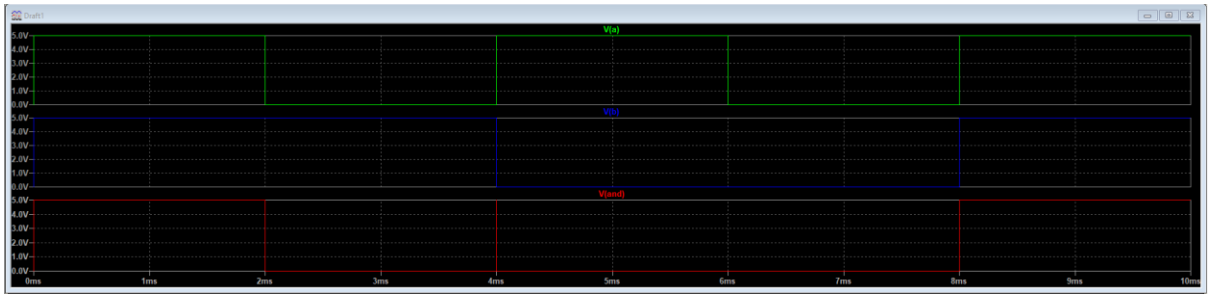
LT SPICE CIRCUIT DIAGRAM:



LT SPICE SIMMULATION SETTINGS:



LT SPICE SIMMULATION OUTPUT:



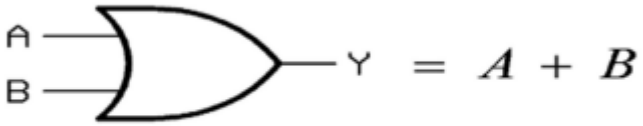
OR GATE:

The OR gate performs a logical addition commonly known as OR function. The output is high when any one of the inputs is high. The output is low level when both the inputs are low.

LT SPICE TRUTH TABLE AND BOOLEAN EXPRESSION:

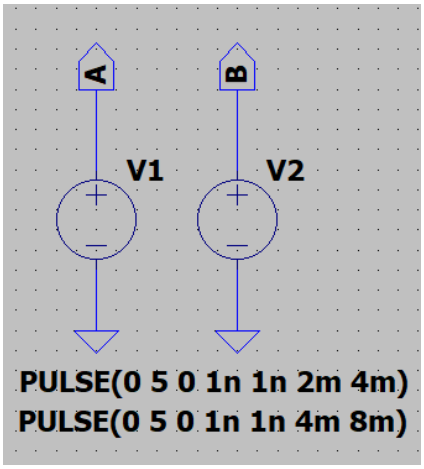
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

SYM BOL

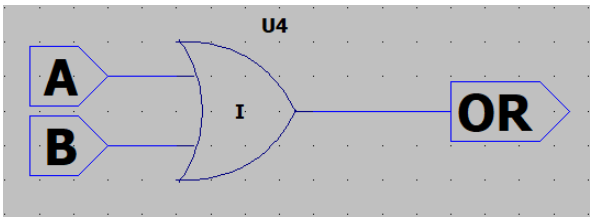


OR gate

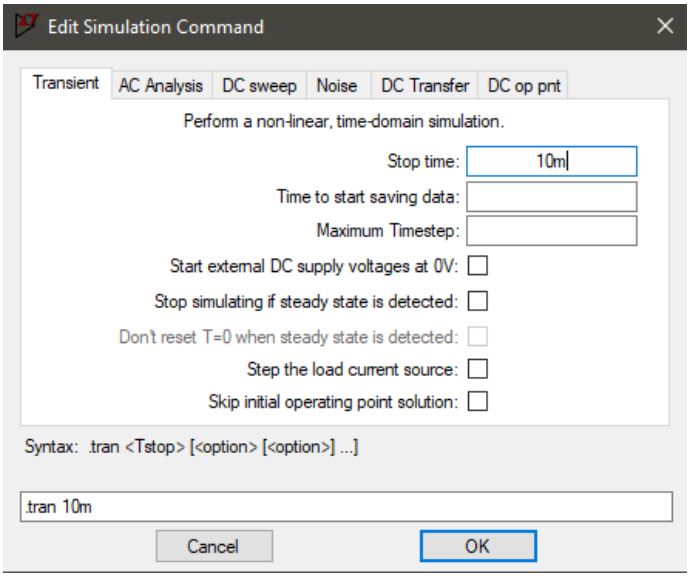
LT SPICE VOLTAGE INPUT:



LT SPICE CIRCUIT DIAGRAM:



LT SPICE SIMMULATION SETTINGS:



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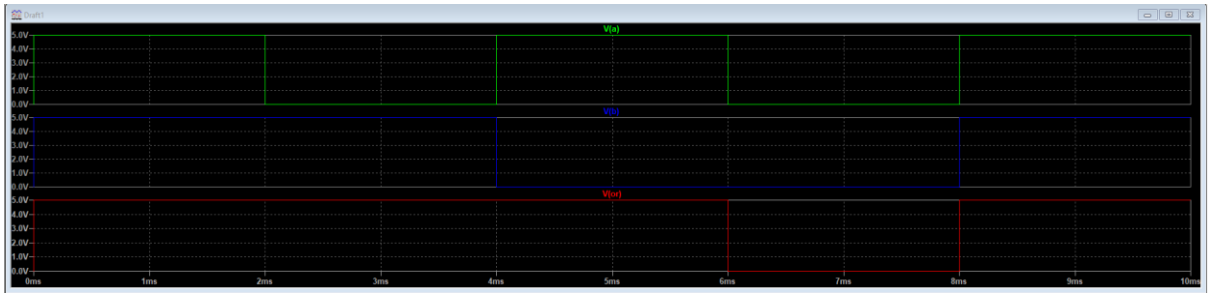


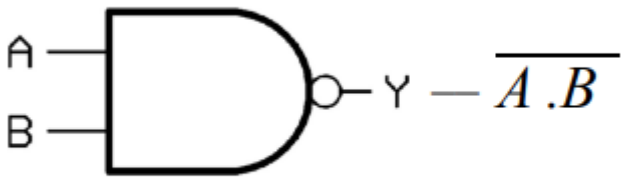
NAND GATE:

The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any one of the inputs is low. The output is low level when both inputs are high.

LT SPICE TRUTH TABLE AND BOOLEAN EXPRESSION:

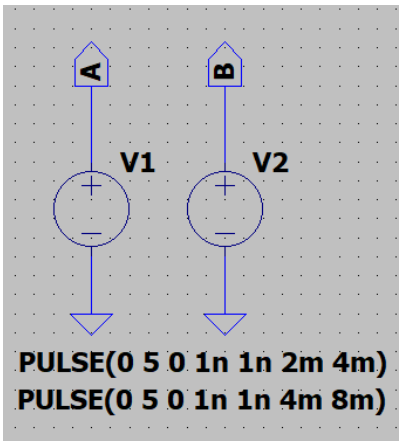
A	B	Y=(A.B)'
0	0	1
0	1	1
1	0	1
1	1	0

SYMBOL

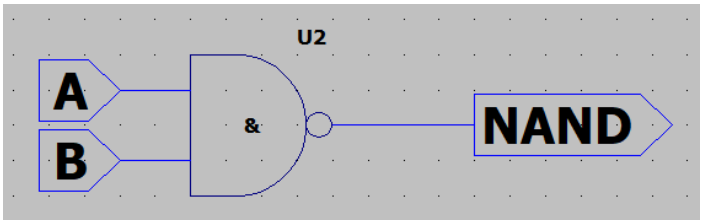


NAND gate

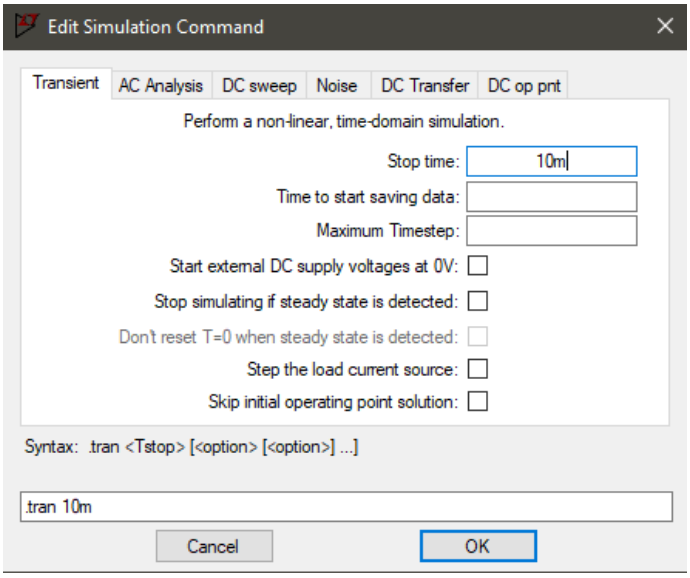
LT SPICE VOLTAGE INPUT:



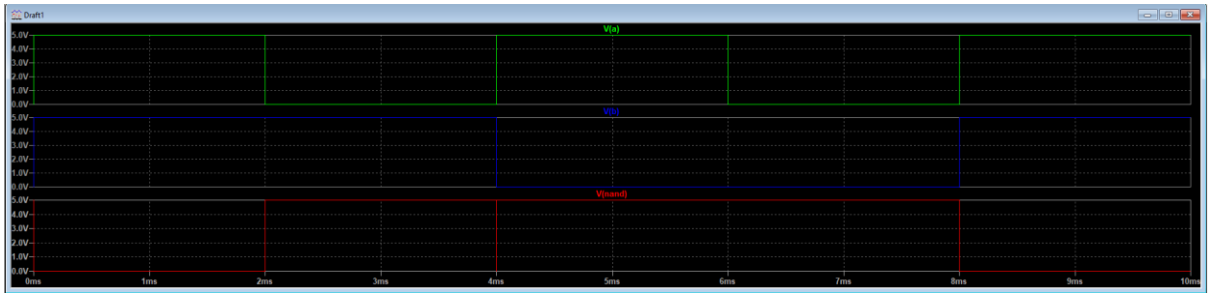
LT SPICE CIRCUIT DIAGRAM:



LT SPICE SIMMULATION SETTINGS:



LT SPICE SIMMULATION OUTPUT:

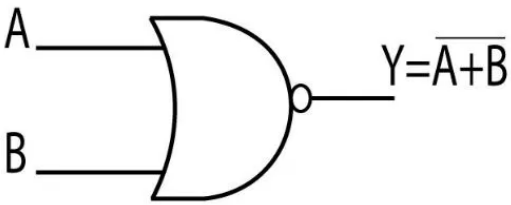


NOR GATE:

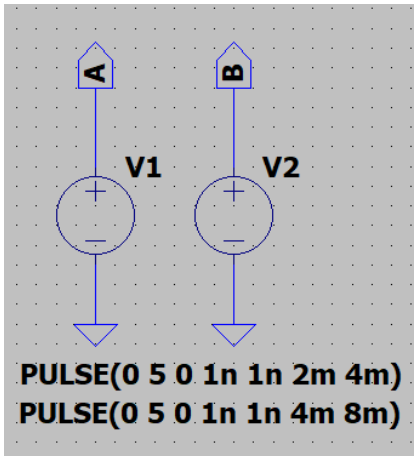
The NOR gate is a contraction of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are high.

LT SPICE TRUTH TABLE AND BOOLEAN EXPRESSION:

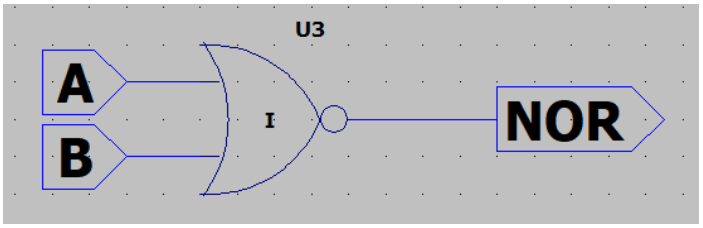
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



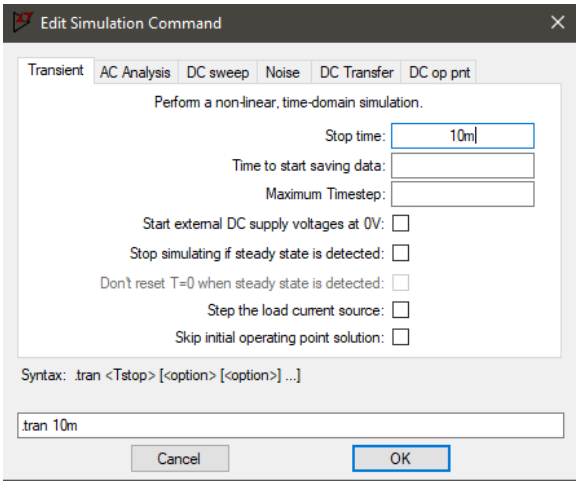
LT SPICE VOLTAGE INPUT:



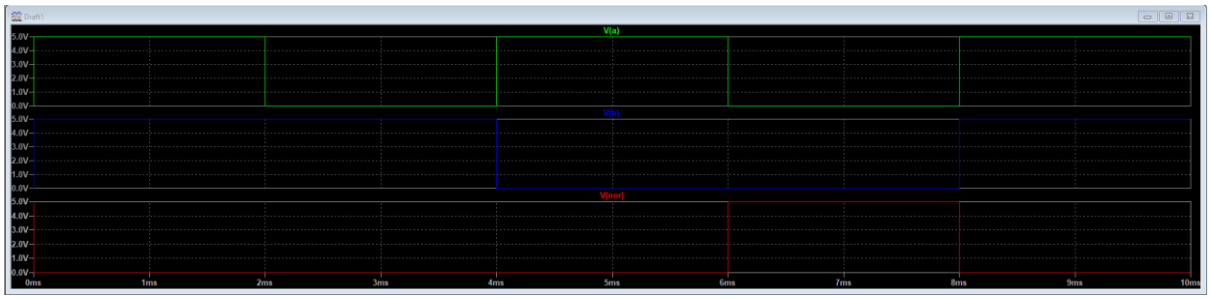
LT SPICE CIRCUIT DIAGRAM:



LT SPICE SIMMULATION SETTINGS:



LT SPICE SIMMULATION OUTPUT:

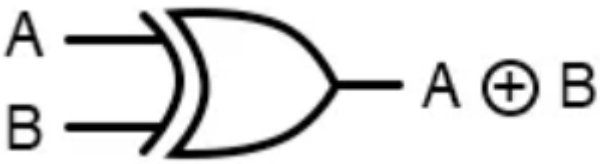


X-OR GATE:

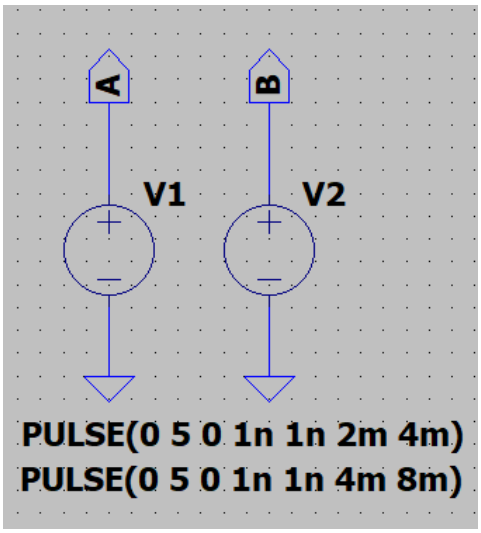
The output is high when any one of the inputs is high. The output is low when both the inputs are low and both the inputs are high.

LT SPICE TRUTH TABLE AND BOOLEAN EXPRESSION:

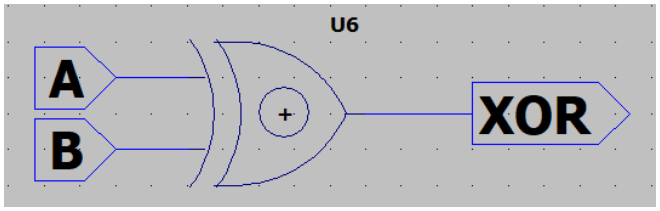
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



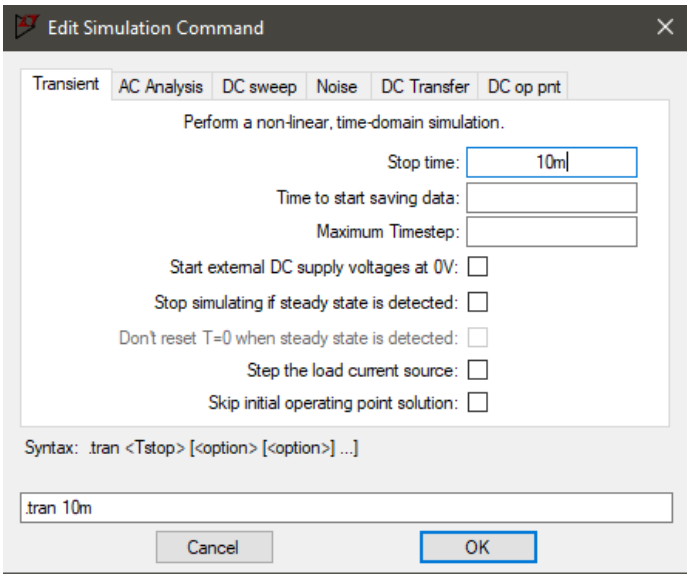
LT SPICE VOLTAGE INPUT:



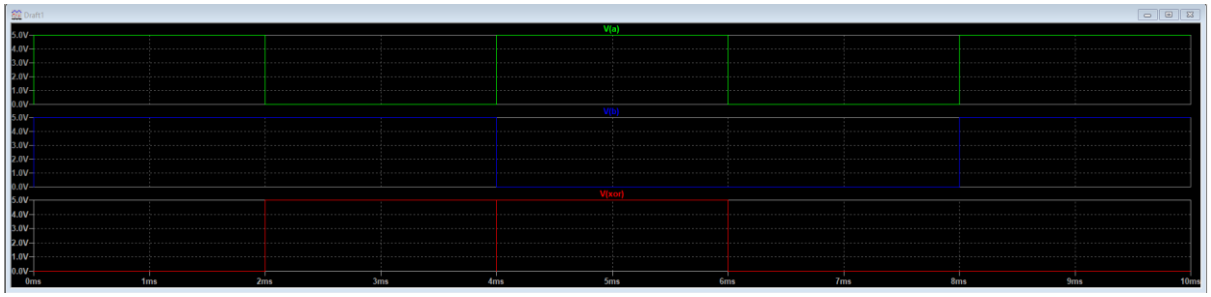
LT SPICE CIRCUIT DIAGRAM:



LT SPICE SIMMULATION SETTINGS:



LT SPICE SIMMULATION OUTPUT:



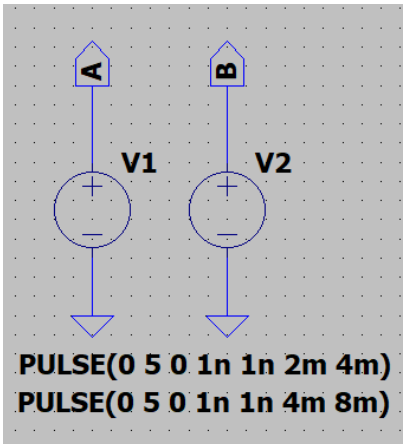
NX-OR GATE:

High when both the inputs are low the output is high, it is also high if both the inputs are high. The NXOR gives low input only if only one of the inputs are low then the net output is high.

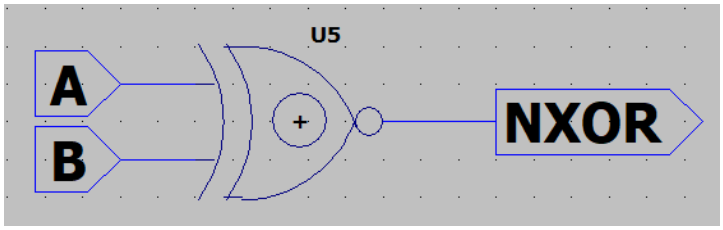
LT SPICE TRUTH TABLE AND BOOLEAN EXPRESSION:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

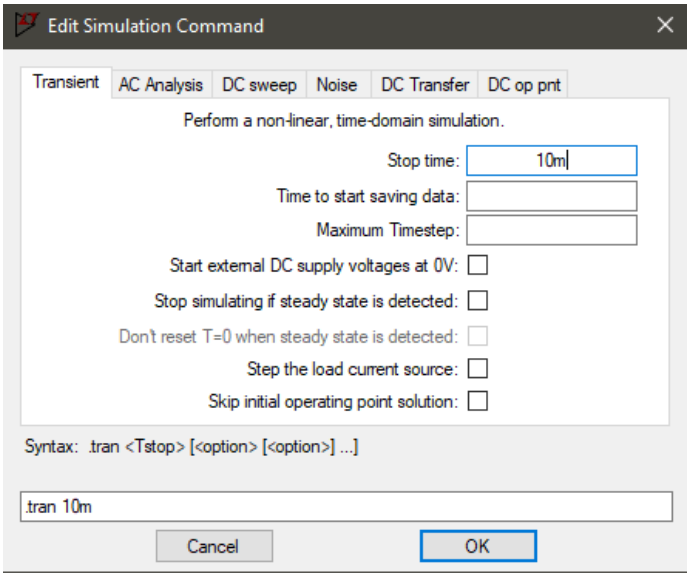
LT SPICE VOLTAGE INPUT:



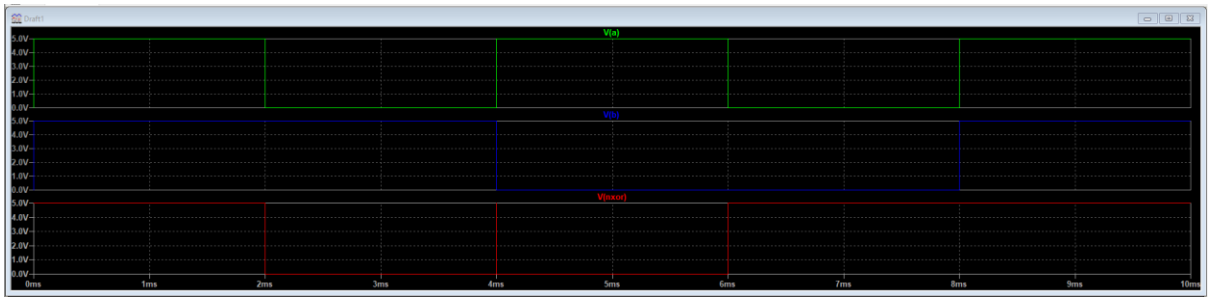
LT SPICE CIRCUIT DIAGRAM:



LT SPICE SIMMULATION SETTINGS:



LT SPICE SIMMULATION OUTPUT:



RESULTS AND INFERENCE:

The results are verified with the help of truth tables and LT SPICE results and hence the logic gates are verified.

EXPERIMENT – 1B

AIM

To realize the basic gates using universal gates.

THEORY

Universal gates are the ones which can be used for implementing any gate like AND, OR and NOT or any combination of these basic gates NAND and NOR gates are universal gates. Any logic function can be implemented using NAND gates. To achieve this, first the logic function is converted using has to be written in Sum of Product (SOP) form. Once the logic circuit is converted to SOP, then it is east to implement using NAND gate. In other words, any logic circuit with AND gates in first level and OR gates in second level can be converted into a NAND-NAND gate circuit. Any logic function can be implemented using NOR gates. To achieve this, first the logic function is converted using has to be written in Product of Sum (POS) form. Once the logic circuit is converted to POS, then it is east to implement using NOR gate. In their words any logic circuit with OR gates in first level and AND gates in second level can be converted into a NOR-NOR gate circuit.

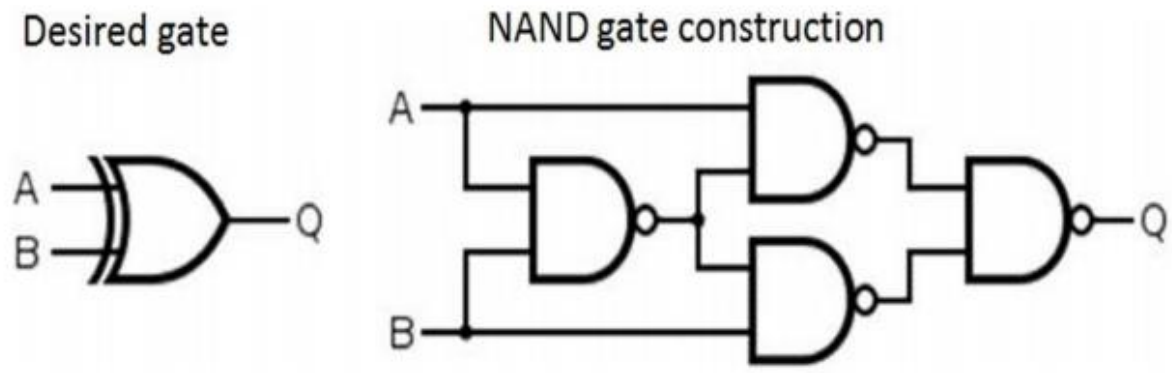
XOR GATE using NAND GATE:

XOR

An XOR gate is constructed similarly to an OR gate, except with an additional NAND gate inserted such that if both inputs are high, the inputs to the final NAND gate will also be high, and the output will be low.

This effectively represents the formula: "NAND (A NAND (A NAND B)) NAND (B NAND (A NAND B))"

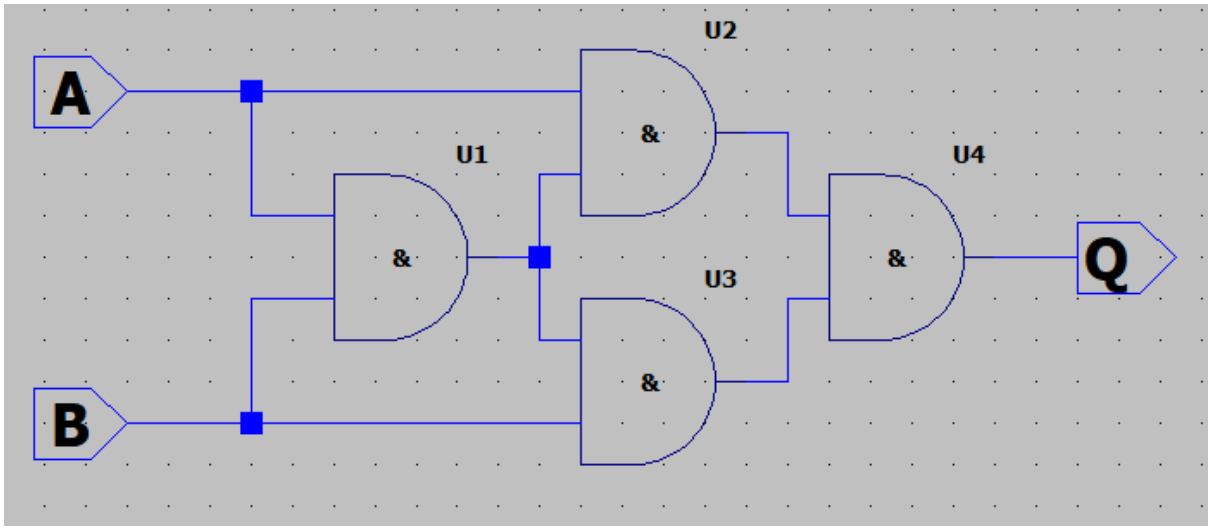
CIRCUIT DIAGRAM AND CONSTRUCTIONS:



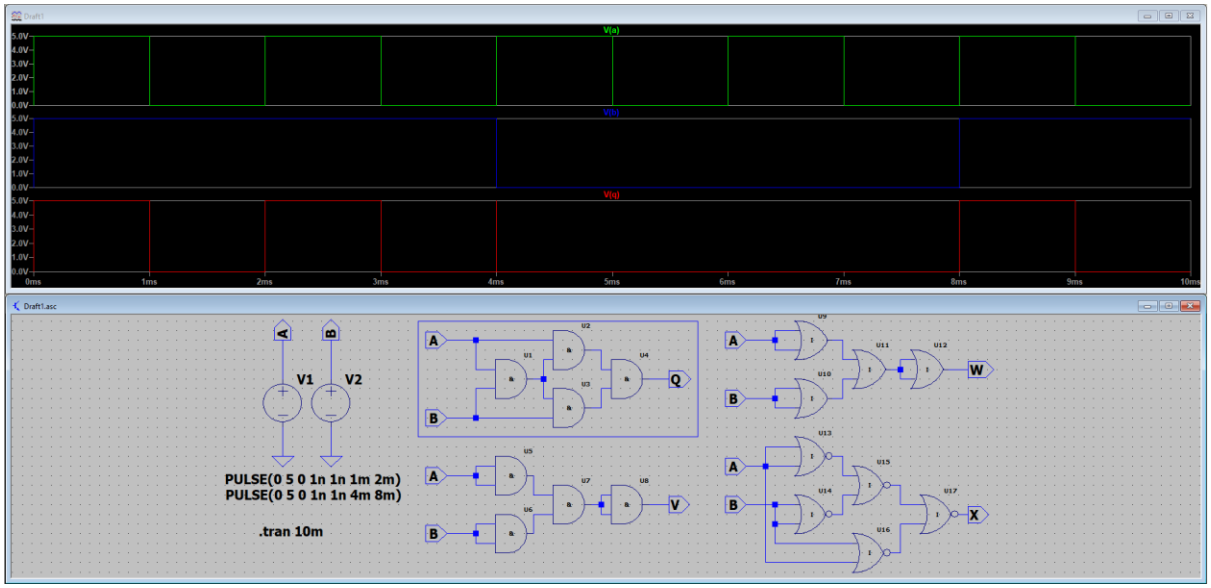
TRUTH TABLE AND OBSERVATIONS:

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

LT SPICE CIRCUIT DIAGRAM:



SIMMULATION:

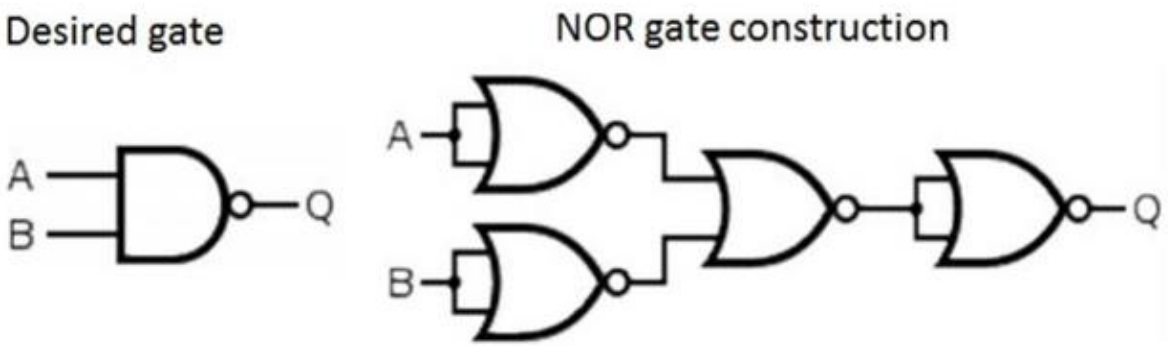


NAND GATE using NOR GATE:

NAND

A NAND gate is made using an AND gate in series with a NOT gate

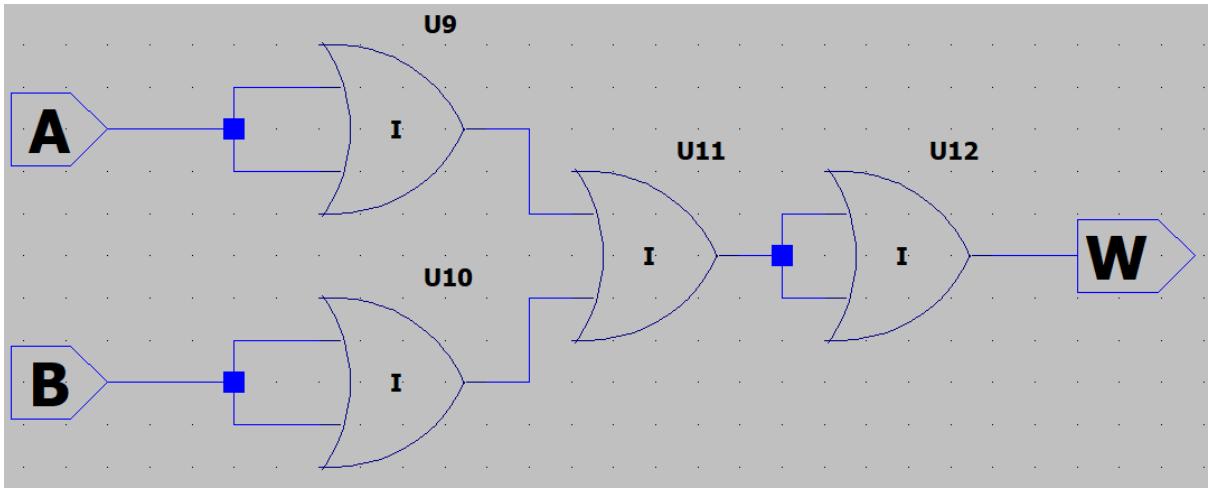
CIRCUIT DIAGRAM AND CONSTRUCTIONS:



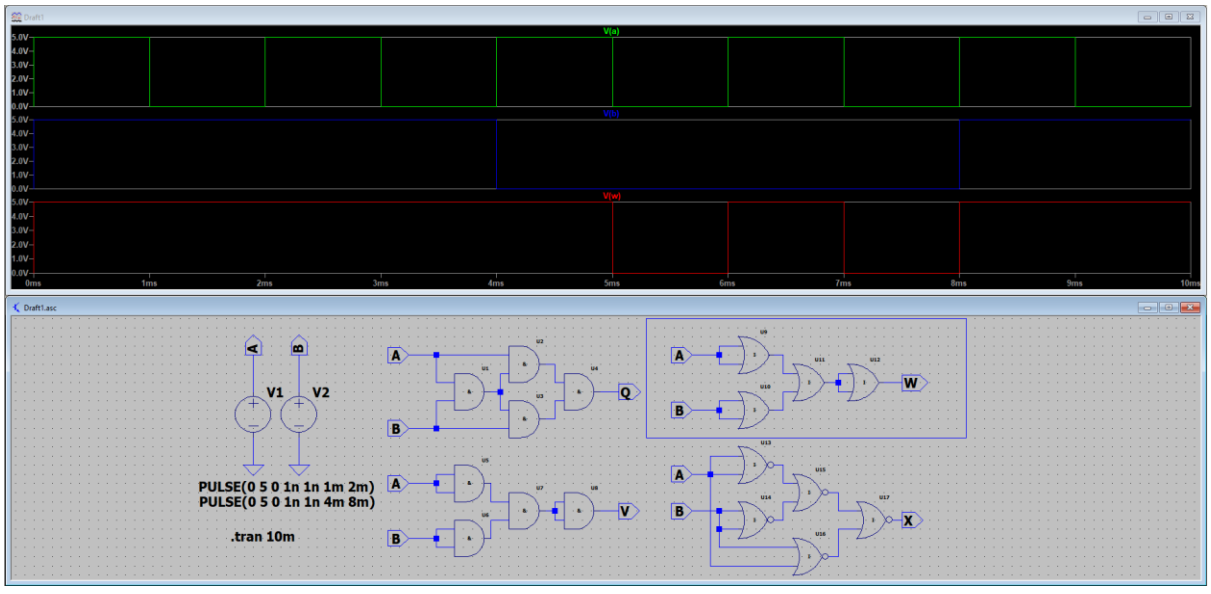
TRUTH TABLE AND OBSERVATIONS:

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

LT SPICE CIRCUIT DIAGRAM:



SIMMULATION:

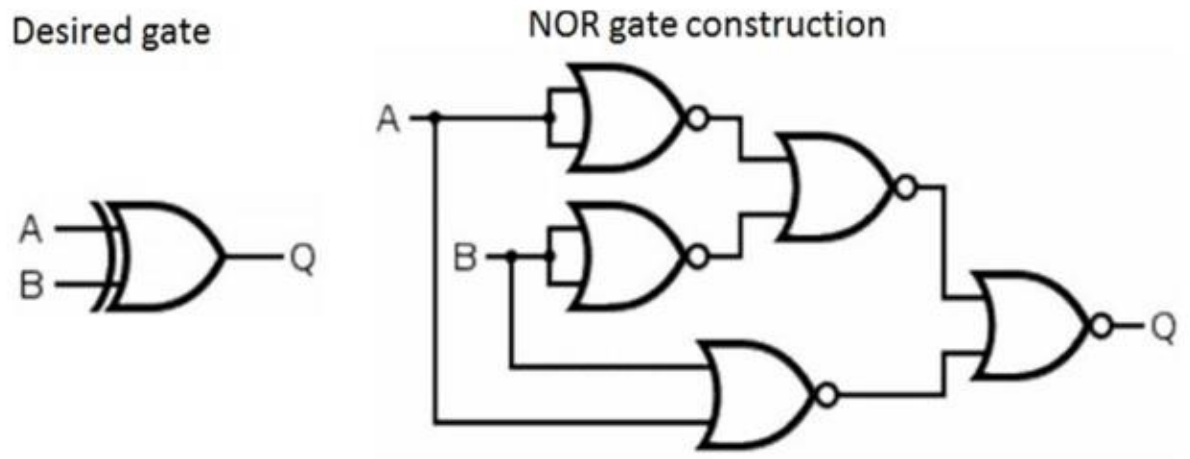


XOR GATE using NOR GATE:

XOR

An XOR gate is made by connecting the output of 3 NOR gates (connected as an AND gate) and the output of a NOR gate to the respective inputs of a NOR gate. This expresses the logical formula (A AND B) NOR (A NOR B). This construction entails a propagation delay three times that of a single NOR gate.

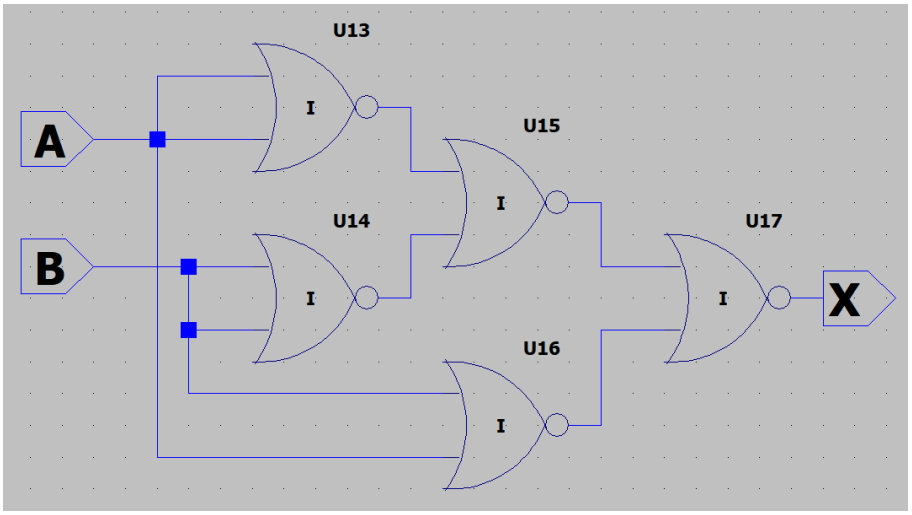
CIRCUIT DIAGRAM AND CONSTRUCTIONS:



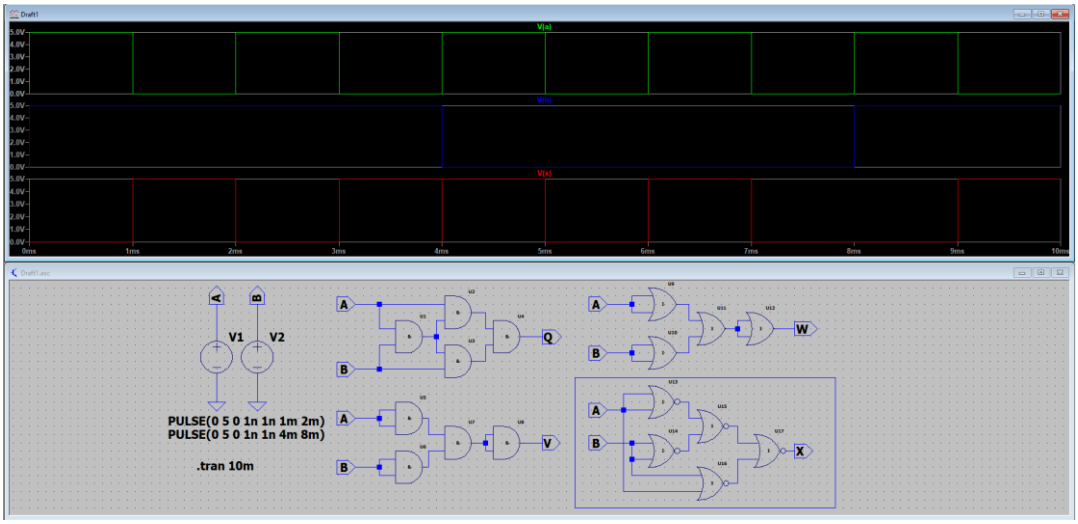
TRUTH TABLE AND OBSERVATIONS:

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

LT SPICE CIRCUIT DIAGRAM:



SIMMULATION:



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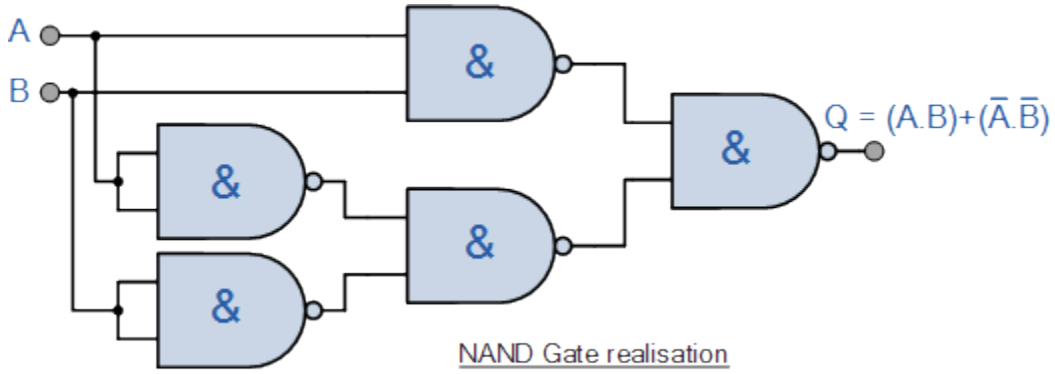
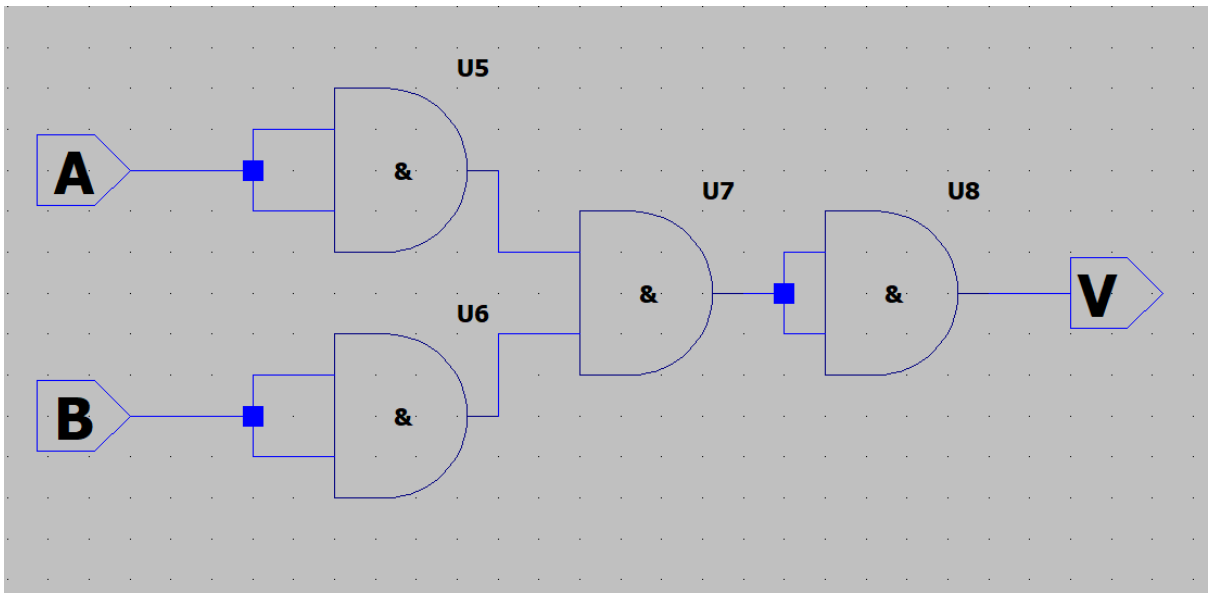


NAND Gate realisation

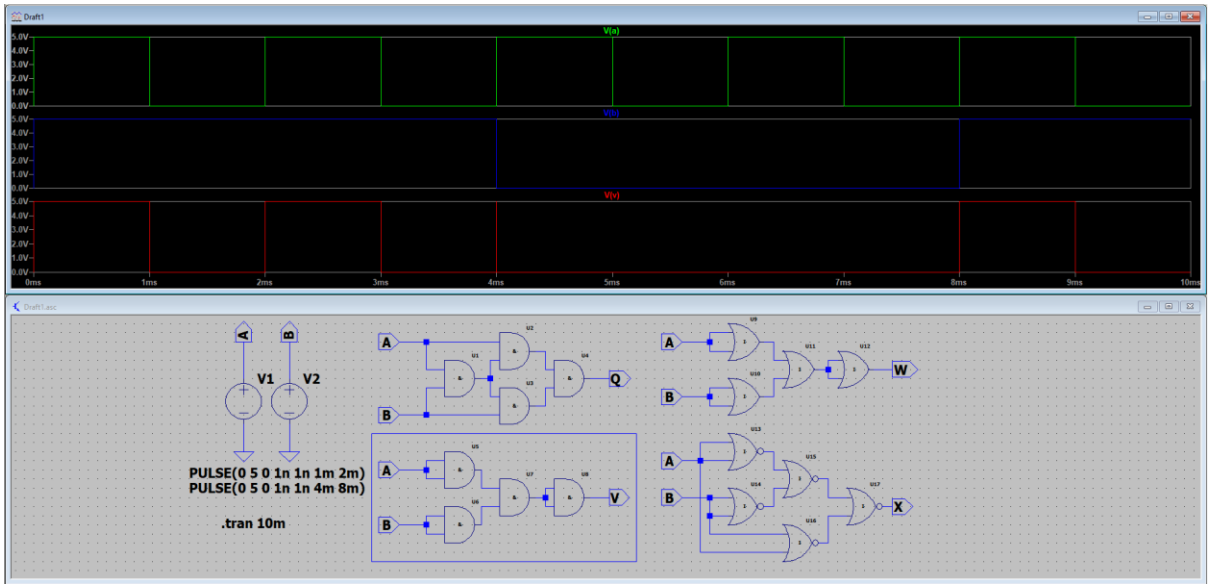
TRUTH TABLE AND OBSERVATIONS:

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

LT SPICE CIRCUIT DIAGRAM:



SIMMULATION:



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