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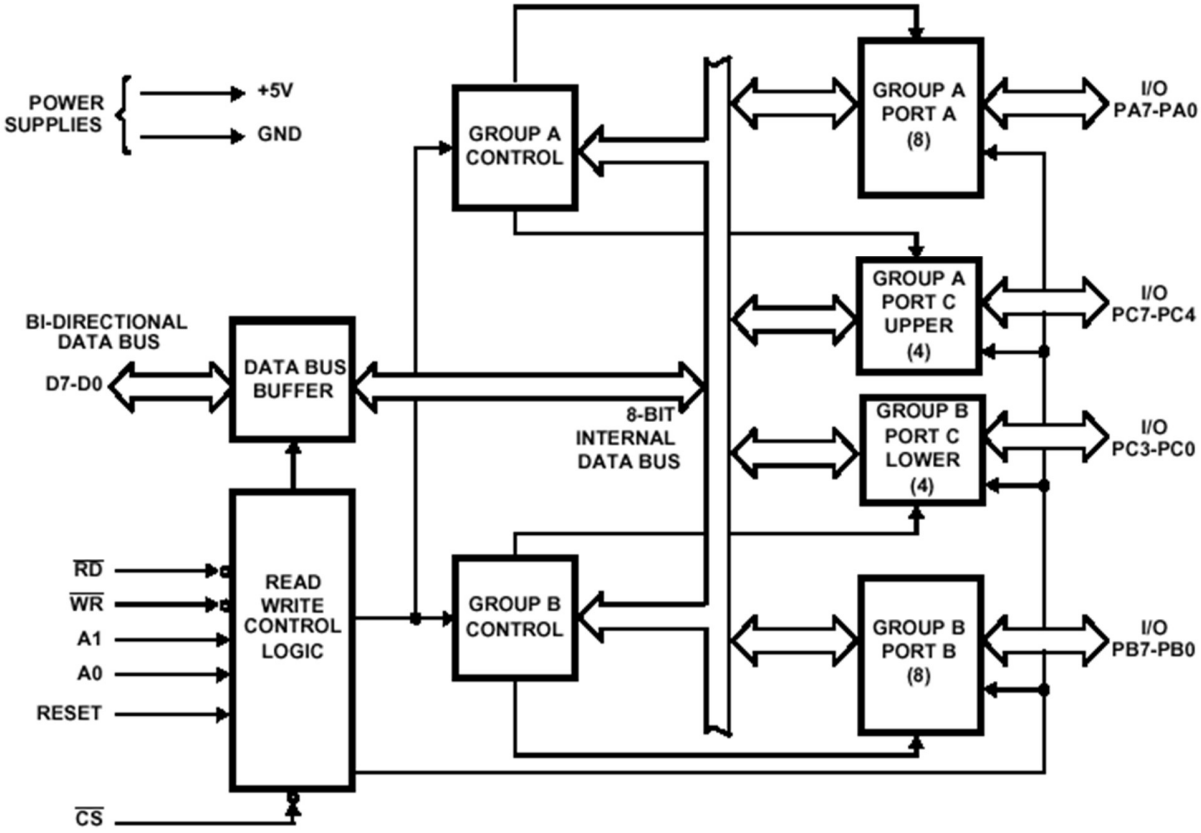
EXPERIMENT NO-8

Aim: Interfacing of IC 8255 with Intel 8086 processor**.**

Theory:

IC8255 (Programmable Peripheral Interface)

Functional Block Diagram:



Block Diagram of the 8255 Programmable Peripheral Interface (PPI)

Data Bus Buffer

This three-state bi-directional 8-bit buffer is used to interface the 8255 to the system data bus. Data is transmitted or received by the buffer upon execution of

input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

(CS) :- Chip Select. A "low" on this input pin enables the communication between the 8255 and the CPU.

(RD) :- Read. A "low" on this input pin enables 8255 to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255.

(WR):- Write. A "low" on this input pin enables the CPU to write data or control words into the 8255.

(A0 and A1):-Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word register. They are normally connected to the least significant bits of the address bus (A0 and A1).

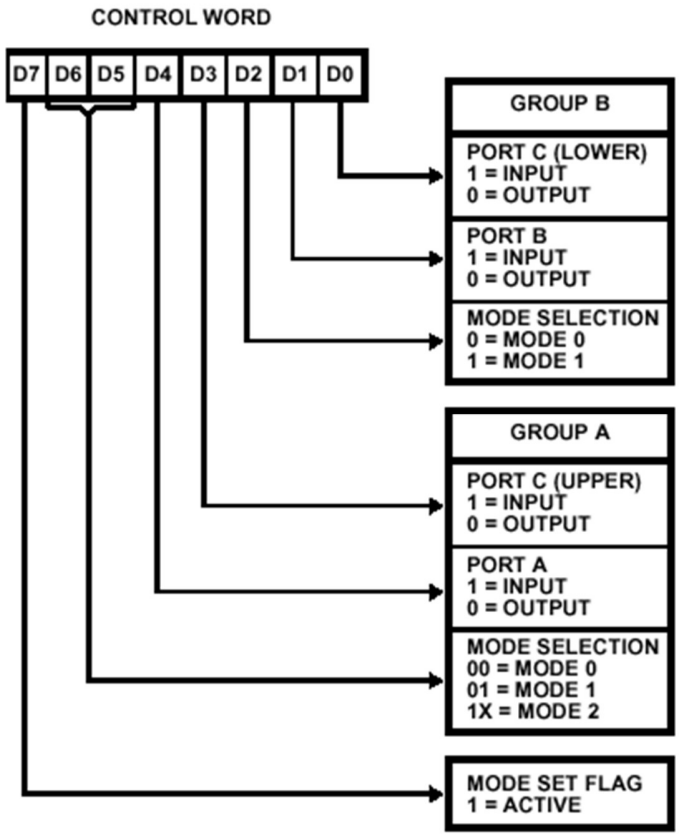
(RESET) :-Reset. A "high" on this input initializes the control register to 9Bh and all ports (A, B, C) are set to the input mode.

A1	A0	SELECTION
0	0	PORT A
0	1	PORT B
1	0	PORT C
1	1	CONTROL

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255. Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports

CONTROL WORD OF 8255



Ports A, B, and C

The 8255 contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255.

Port A -One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A.

Port B -One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C -One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal output and status signal inputs in conjunction with ports A and B

Program

```
Dyna-86> A 1000:1000
1000:1000 MOV AL,80
1000:1002 OUT 33,AL
1000:1004 MOV AL,55
1000:1006 OUT 30,AL
1000:1008 MOV AL, AA
1000:100A OUT 31,AL
1000:100C MOV AL,0F
1000:100E OUT 32,AL
1000:1010
Dyna-86> A 1000:1000,1000:1010
Break at 0FFF:1011
Dyna-86>
```

Output for 8255 interface card is based on mode selection and output will be on LED or in memory location. After execution of this program LED will glow according to the input given in AL register.

Conclusion:- Output is observed on LED's for the4 inputs given on the specified register. With the output different I/O modes and control word format has been studied in this experiment**.**