

Assignment:-2

Q-1 EXPLAIN by Hyperthreading mechanism and its use in Pentium-4

- * Hyperthreading was Intel's first effort to bring parallel computation to end users PC. It was first use on desktop CPU with the Pentium 4.
- * The Pentium 4 at that time only featured just a single CPU core. therefore it only performs a single task and fails to perform any type of multiplex operation.
- * A single CPU with hyperthreading appears as two logical CPU for an operating system. In this case, the CPU is single but the OS considers two CPUs for each core and hardware has single set of execution.
- * Therefore, CPU assume as it has multiple cores than it does and the operating system assume two CPUs for each core.
- * Hyperthreading allows each core to do two things simultaneously. It increases CPU performance by improving the processor's efficiency, thereby allowing the user to run multiple demanding apps at a same time or use heavily threading apps without the PC lagging.
- * Today hyperthreading is available on Intel core, core i3, i5, i7 etc.

- * TO use hyperthreading in Pentium 4 or in general on OS and BIOS that support hyperthreading technology.
For Pentium 4 BIOS supports this hyperthreading technology.
- * Use of Hyperthreading in Pentium 4
 - (i) with hyperthreading Pentium 4 can process more info in less time and can run more background task.
 - (ii) computer experience is boosted in Pentium 4 and users are more likely to multitask and run heavily threaded program.
 - (iii) hyperthreading the cores in Pentium 4 improves performance and speed, but on a case by case basis depending on which task are compatible with hyperthreading core.

Q-2 Analyze the use of 80386 Protection mode w.r.t privilege level for different users.

- Ans * 80386 CPU Provides a very advanced mode of operations called the Protected mode.
- * In Protected mode, 80386 CPU Provides dedicated hardware to prevent user programs from affecting other user programs and also safeguards the operating system from being affected by user programs.
 - * There are four privilege levels, assigned to programs and data to define their privileges.

1) Level 0 :- This level is assign to operating system Kernel.

- (i) It is most privilege level.
- (ii) Any program at this level can access all the data at any privilege level whereas data at this level can only be accessed by a program at privilege level 0

2) Level 1 :- This level is assigned to the system services such as file handling device drivers.

- (i) It is 2nd most privilege level.
- (ii) Any program at this level can access the data from any other level having lower privilege level. whereas data at this level can only access by program at level 0 and level 1

3) Level 2 :- This level is assigned to the custom extension of the operating system.

- (i) This is 3rd most privilege level.
- (ii) Any program at this level can access the data at any privilege level which is lower than this level (numerically levels), whereas data at this privilege level can only be accessed by a program at privilege level 0, 1 or 2.

4) Level 3 :- This level is assigned to all the user application and programs.

- (i) This is the least privileged level.
- (ii) Any program at this level can more likely access data at privilege levels 0, whereas data at this level can be accessed by any level 0, 1, 2, 3.

Q-3

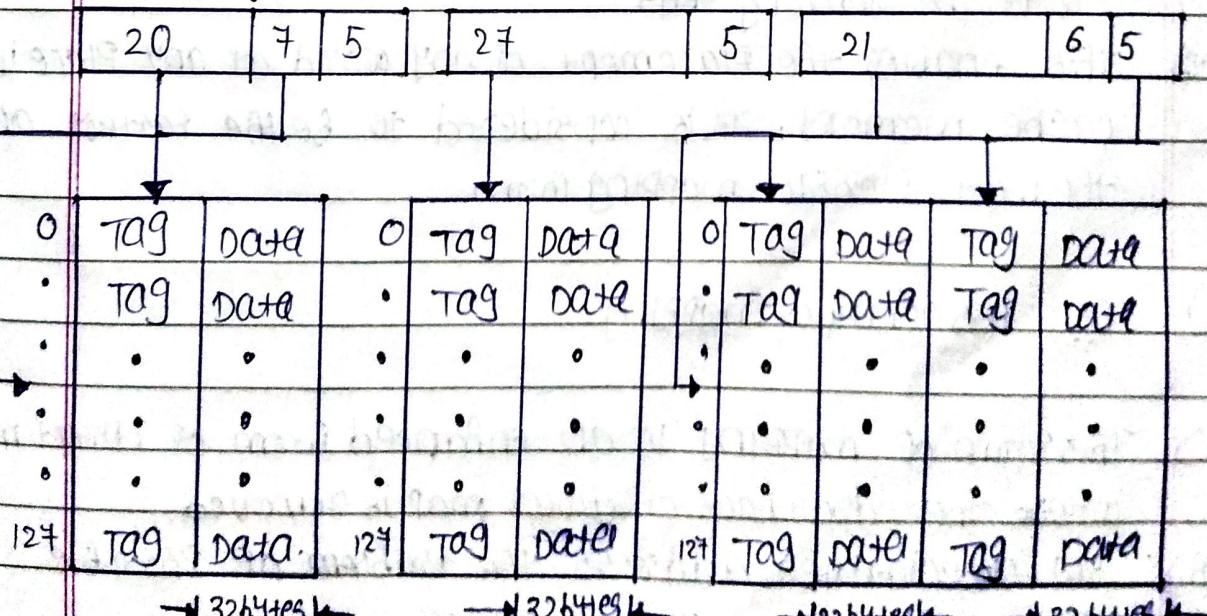
Sketch and explain Cache organisation of Pentium Processor.

Ans

When processor needs to read or write a location in main memory, it checks the a corresponding entry in the cache.

- 1) If the processor finds that the memory location is in the cache, a cache hit has occurred and data is read from cache.
 - 2) If the processor does not find the memory location in the cache, a cache miss has occurred for a cache miss, the cache allotted new entry and copies in data from main memory, then the request is fulfilled from the contents of cache.
- * There are 3 different type of mapping used.
- (i) direct mapping
 - (ii) associative mapping
 - (iii) set-associative mapping.

82-bit Physical add 32-bit Phy-add. 32-bit Phy-add.



direct
mapped cache

associativ
mapped

set-associativ
mapped

① Direct Mapping :-

- (i) The simplest technique, known as direct mapping, map each block of main memory into one possible cache line.
- (ii) In direct mapping, assign each block to a specific line in the cache.
- (iii) If a line is previously taken by a memory block then a new block needs to loaded.
- (iv) An address space is split into two parts index field and tag field.
- (v) The cache is used to store the tag field whereas the rest is stored in the main memory.

② Fully Associative mapping :-

- (i) In this type of mapping, the associative memory is used to store content and address of memory word.
- (ii) Any block can go into any line of the cache.
- (iii) This means that the word id bits are used to identify which word in the block is needed, but the tag becomes all of the remaining bits.
- (iv) This enables the placement of any word at any place in the cache memory. It is considered to be the fastest and the most flexible mapping form.

③ Set-Associative mapping

- (i) This form of mapping is an enhanced form of direct mapping where the drawback of direct map is removed.
- (ii) Set associative address the problem of possible thrashing in the direct mapping.

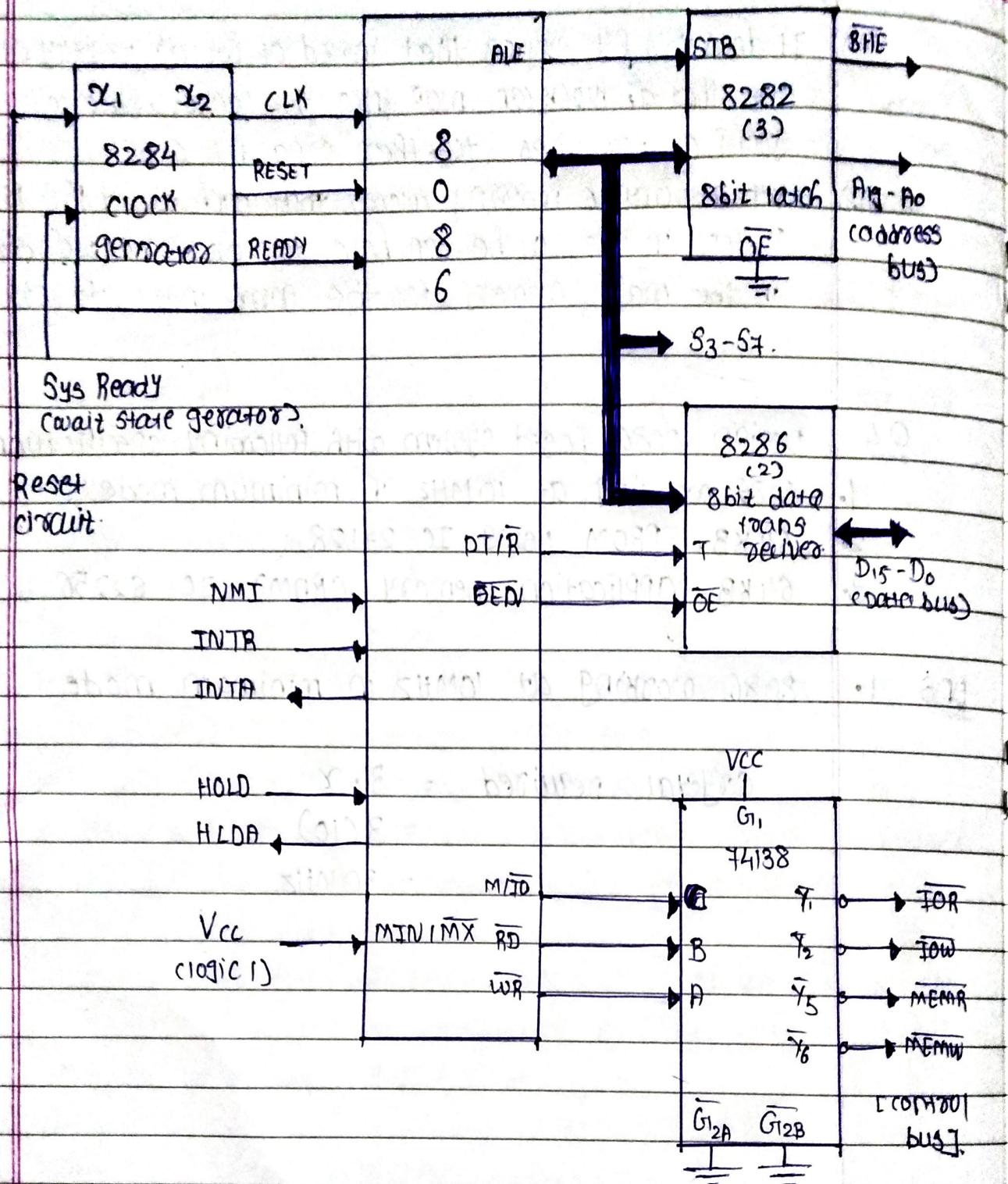
- , (iii) It does this by saying that instead of having exactly one line that a block can map into the cache, we will group a few lines together creating a set.
- (iv) Set-associative mapping allows that each word that is present in the cache can have two or more words in the main memory for the same index address.

Q4 Design 8086 based system with following specification

1. 8086 working at 10 MHz in minimum mode
2. 64 KB, EPROM using IC 27128
3. 64 KB, Application memory (RAM) IC 62256

Ans 1. 8086 working at 10 MHz in minimum mode.

$$\begin{aligned}\text{crystal required} &= 3 : 2 \\ &= 3(10) \\ &= 30 \text{ MHz}\end{aligned}$$



②) 64 KB EEPROM using 27128

\Rightarrow Required memory = 128 KB

available memory = 64 KB

"number" of chip required = 2

Number of address line = 3 lines [$A_1 - A_3$]

$$\text{Size of single EPROM chip} = 64 \text{ KB} = 2^{16}$$

31 64KB application memory from using IC 62256

$$\Rightarrow \text{RAM required} = 256\text{KB} \quad \text{size of single RAM} = 64\text{KB}$$

$$\text{RAM Available} = 64 \text{ KB} = 2^{16}$$

NO. OF CHIPS = 4 CHIPS