```
`timescale 1ns / 1ps

module lab_1(
input  [15:0]  pc,
output wire  [15:0] instruction
    );
    wire [3:0] rom_addr = pc[4:1];
    reg [15:0] rom[15:0];
    initial
    begin
            rom[0]=16'b1110000100001001;
            rom[1]=16'b1010000100000111;
            rom[2]=16'b1110000100000101;
            rom[3]=16'b1000000100000111;
            rom[4]=16'b0100000100001111;
            rom[5]=16'b1100000101111010;
            rom[6]=16'b0000000000000000;
            rom[7]=16'b0000000000000000;
            rom[8]=16'b0000000000000000;
            rom[9]=16'b0000000000000000;
            rom[10]=16'b0000000000000000;
            rom[11]=16'b0000000000000000;
            rom[12]=16'b0000000000000000;
            rom[13]=16'b0000000000000000;
            rom[14]=16'b0000000000000000;
            rom[15]=16'b1100000001110000;
       end
       assign instruction ={pc[15:0]   <32}? rom[rom_addr[3:0]]:16'b0  ;




endmodule


 Test bench


module lab_1_tb();

      reg         [15:0]          pc;
      wire          [15:0]     instruction;
    lab_1 m1(pc,instruction);
```

```
  initial begin
  #5 pc = 16'b0000000000000000;
  #10 pc = 16'b0000000000000001;
   #10 pc = 16'b0000000000000010;
   #10 pc = 16'b0000000000000011;
   #10 pc = 16'b0000000000000100;

  end



endmodule
```