Shri Ramdeobaba College of Engineering and Management,

Nagpur-13.

Department of Electronics Engineering

ENP352 –CMOS Digital Circuit Design Lab

Lab 3

Effect of trans-conductance ratios on VTC of CMOS inverter and simulation of the Intrinsic Propagation delay of inverter.

Odd Semester – 2023-24

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Date of Performance:	21/10/23
Date of Submission:	28/10/23
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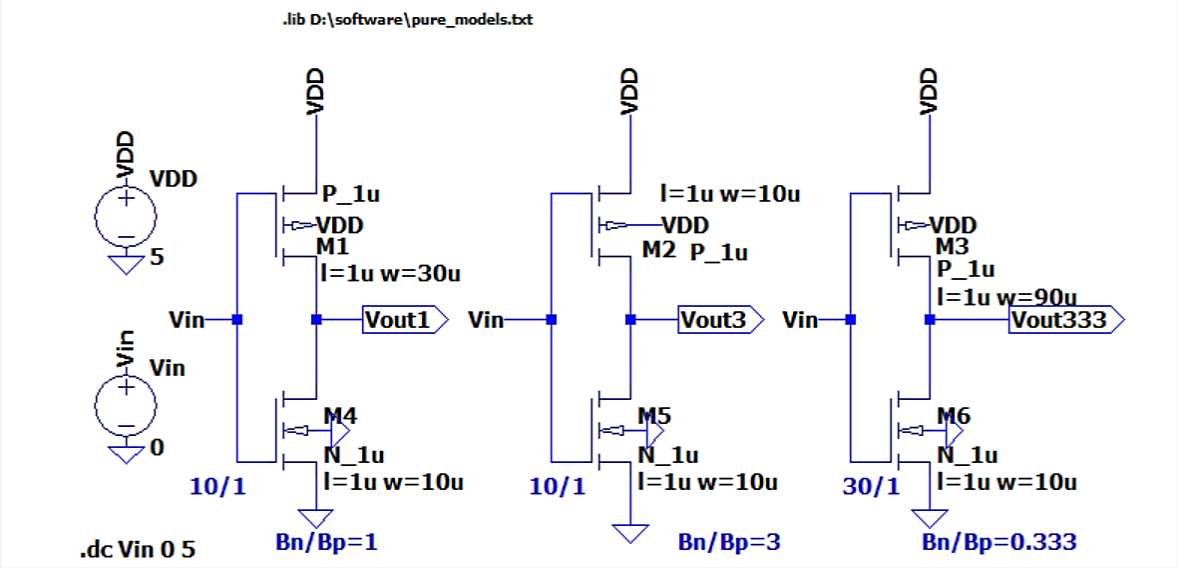
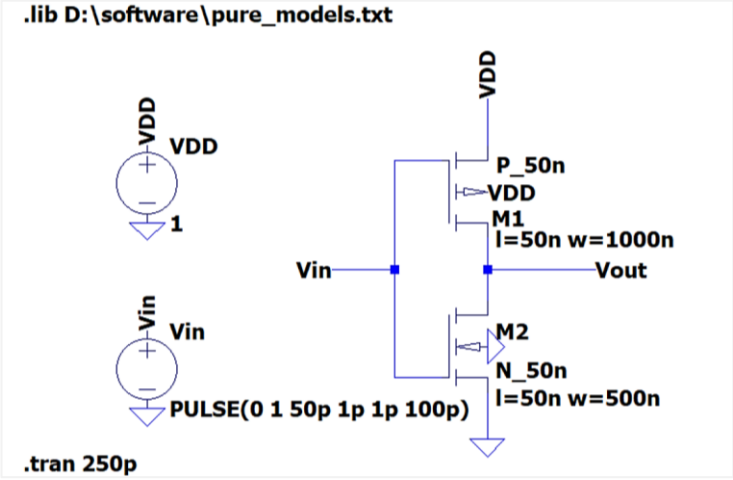
Lab-03

1) **Aim:** Investigate using SPICE and the long-channel CMOS process parameters supplied to you, the transfer curves for the CMOS inverter with trans-conductance ratios βn/βp 3, 1, and 1/3. Explain what changing the ratio does to the transfer characteristics. Estimate and simulate the intrinsic propagation delays of inverter if short channel devices are used (PMOS: NMOS=2:1).

- ✓ **Software Used: LTspice**
- ✓ **Circuit Diagram:**





✓ **Observation Table**

Table No. 1: For Inverter (Long Channel) (Wn=10u Ln=1u) (Wp=30u Lp=1u)

Value of β_n/β_p	**Switching Threshold of the inverter (Vm)**
β_n/β_p= 1	2.558V
Value of β_n/β_p	**Switching Threshold of the inverter (Vm)**
β_n/β_p= 1/3	3.122V
Value of β_n/β_p	**Switching Threshold of the inverter (Vm)**
β_n/β_p= 3	1.905V

Table No. 2: For Inverter (Short Channel) (Wn=50n Ln=500n) (Wp=50n Lp=1000n)

Variables	Values
t_{PHL}	**59.66ps – 50.5ps = 9.16ps**
t_{PLH}	**160.99ps – 151.49ps = 9.50ps**

✓ **Calculations:**

Theoretical Vm = VDD/2 = 5/2 = 2.5V

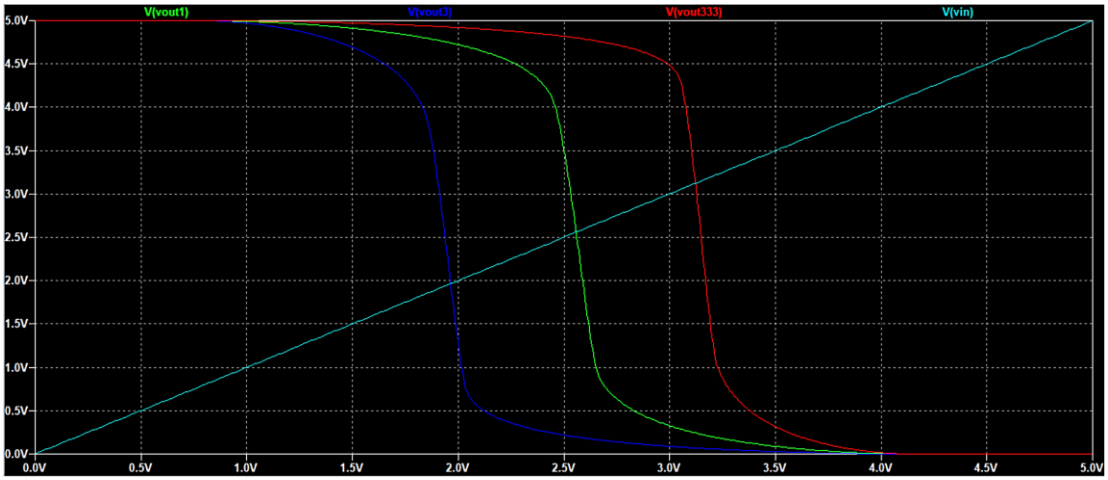
For T_{PHL}:
Vin = 50.5ps
Vout = 59.66ps

Propagation Delay
T_{PLH} = Vout - Vin
= 59.66ps – 50.5ps
= 9.16ps

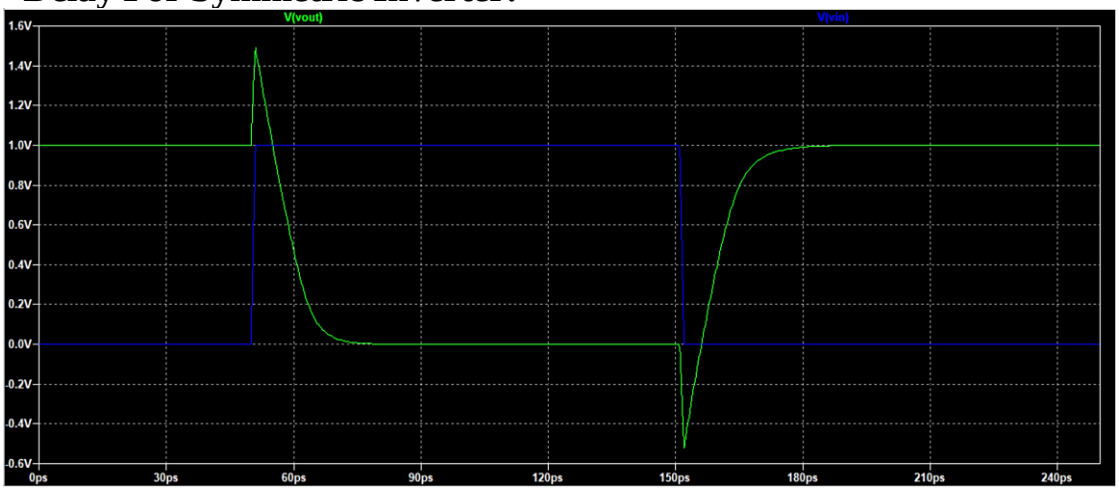
For T_{PLH}:
Vin = 151.49ps
Vout = 160.99ps

Propagation Delay
T_{PLH} = Vout – Vin
= 160.99ps – 151.49ps
= 9.50ps

✓ **Obtained Waveforms/Simulation Results:**



Delay For Symmetric Inverter:



✓ Discussion and Conclusion:

For a long-channel inverter with a Bn/Bp ratio of 1, the switching threshold is 2.55 V. This threshold is where Vin equals Vout on the transfer curve, and with a ratio of 1, both nmos and pmos transistors have equal strength. If we change the ratio to 0.33, the pmos becomes stronger, shifting its VTC to the left. This occurs because the input voltage that triggers an output change moves to lower levels. Conversely, if we make the nmos stronger (ratio Bn/Bp=3), the VTC shifts to the right, making the inverter less sensitive to lower input voltages, and the transition from low to high occurs at a higher input voltage. The propagation delay of a logic gate is approximately 9.1 ps for both tPHL (low to high transition) and tPLH (high to low transition), calculated at the 50% point of the input-output transition.

Batch-A2 -22_Lab-03