Shri Ramdeobaba College of Engineering and Management, Nagpur-13.

Department of Electronics Engineering

ENP352 –CMOS Digital Circuit Design Lab

Odd Semester – 2023-24

Lab 05

Driving Big Capacitive Loads.

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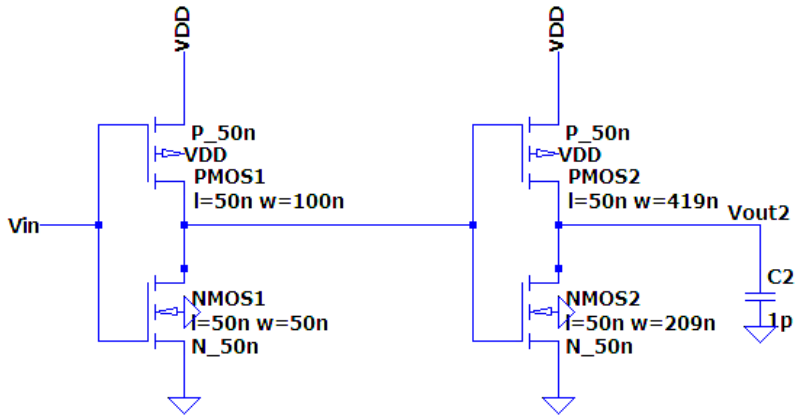
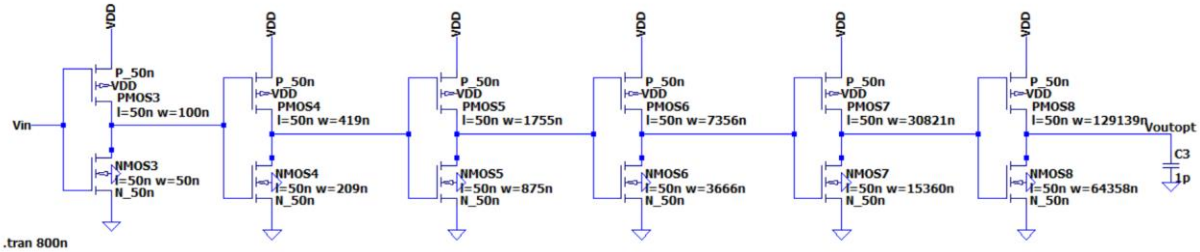
Lab-05

1) **Aim:** Design a buffer (chain of inverters) to drive the load capacitance with a minimum delay. You need to start the design from the minimum sized inverter (L=Ln=Lp=50n, Wp= 450n, Wn= 150n). Load that needs to be driven is of 1 pF. (Use short channel models).

✔ **Software Used: LTspice**

✔ **Circuit Diagram:**





✔ **Observation Table**

Table No. 1: For chain of inverters (Short Channel)

Optimal no. of stages: 06

Observed delay from input to output:

Stage	W/L (NMOS)	W/L (PMOS)
#1	(W=50n; L=50n)	(W=100n ;L=50n)
#2	(W=209n; L=50n)	(W=419n ;L=50n)
#3	(W=875n; L=50n)	(W=1755n ;L=50n)
#4	(W=3666n; L=50n)	(W=7356n ;L=50n)
#5	(W=15360n; L=50n)	(W=30821n ;L=50n)
#6	(W=64358n; L=50n)	(W=129139n ;L=50n)
#7	(W=269660n; L=50n)	(W=541092n; L=50n)
#8	(W=1128527n; L=50n)	(W=2264470n; L=50n)

Table No. 2: For chain of inverters (Short Channel)

No. of stages: 01

Observed delay from input to output: 20.42n

Table No. 3: For chain of inverters (Short Channel)

No. of stages: 02

Observed delay from input to output: 4.12n

Table No.4: For chain of inverters (Short Channel)

No. of stages: 03

Observed delay from input to output: 1.14n

Table No.5 For chain of inverters (Short Channel)

No. of stages: 04

Observed delay from input to output: 0.427n

Table No.6: For chain of inverters (Short Channel)

No. of stages: 05

Observed delay from input to output: 0.414n

Table No.7: For chain of inverters (Short Channel)

No. of stages: 06

Observed delay from input to output: 0.34n

Table No.8: For chain of inverters (Short Channel)

No. of stages: 07

Observed delay from input to output: 0.74n

- ✔ **Calculations:**

Case 1 (single stage):

t1=400n
t2=420.42n
tphl = 420.42n – 420n
= 20.42n

t1=500n
t2=520.42n
tplh = 520.42n – 500n
= 20.42n
Tpd = (tplh+tphl)/2

= 20.42n

Case 2 (stages=2):

t1=500n
t2=504.12n
tphl = 500n – 504.12n
= 4.12n

t1=400n
t2=404.12n
tplh = 404.12n – 400n
= 4.12n
Tpd = (tplh+tphl)/2
= 4.12n

Case 3 (stages=3):

t1=400n
t2=401.14n
tphl = 401.14n – 400n
= 1.14n

t1=500n
t2=501.14n
tplh = 501.14n – 500n
= 1.14n
Tpd = (tplh+tphl)/2
= 1.14n

Case 4 (stages=4):

t1=500n
t2=500.427n
tphl = 500.427n – 500n

= 0.427n

t1=400n
t2=400.427n
tplh = 400.427n – 400n
= 0.427n
Tpd = (tplh+tphl)/2
= 0.427n

Case 5 (stages=5):

t1=400n
t2=400.414n
tphl = 400.414n – 400n
= 0.414n

t1=500n
t2=500.41n
tplh = 500.41n – 500n
= 0.41n
Tpd = (tplh+tphl)/2
= 0.41n

Case 6 (stages=6):

t1=500n
t2=500.35n
tphl = 500.35n – 500n
= 0.35n

t1=400n
t2=400.33n
tplh = 400.33n – 400n
= 0.33n
Tpd = (tplh+tphl)/2
= 0.34n

Case 7 (stages=7):

t1=500n
t2=500.76n
tphl = 500.76n – 500n
= 0.76n

t1=400n
t2=400.73n
tplh = 400.73n – 400n
= 0.73n
Tpd = (tplh+tphl)/2
= 0.74n

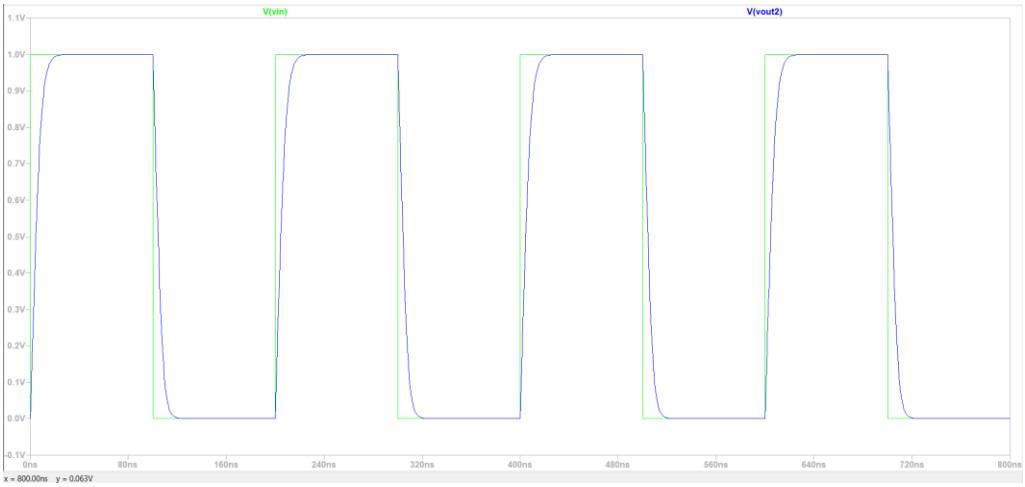
Case 8 (stages=8):

t1=300n
t2=300.35n
tphl = 300.34n – 300n
= 0.34n

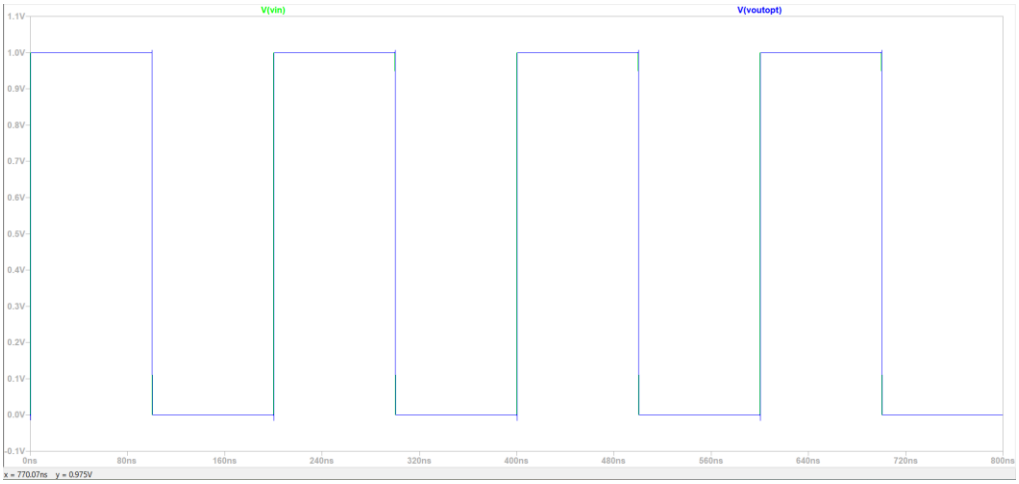
t1=200n
t2=200.32n
tplh = 200.32n – 200n
= 0.32n
Tpd = (tplh+tphl)/2
= 0.33n

Obtained Waveforms/Simulation Results:

Case2: (stages = 2)



Case6:(Stages=6)



✔ Discussion and Conclusion:

As the number of stages of inverters is increased the propagation delay is reduced drastically due to the increase in fanout at each stage. We take one stage less than the optimal value of n since after a certain point the reduction in delay is not that significant but the size increases very significantly, therefore avoid to go for the optimal value.

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