Shri Ramdeobaba College of Engineering and Management, Nagpur-13.
Department of Electronics Engineering

ENP352 –CMOS Digital Circuit Design Lab

Odd Semester – 2023-24

Lab 06

Sequential Logic Element

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Semester/Section:	Sem V· A
Date of Performance:	18/11/23
Date of Submission:	25/11/23
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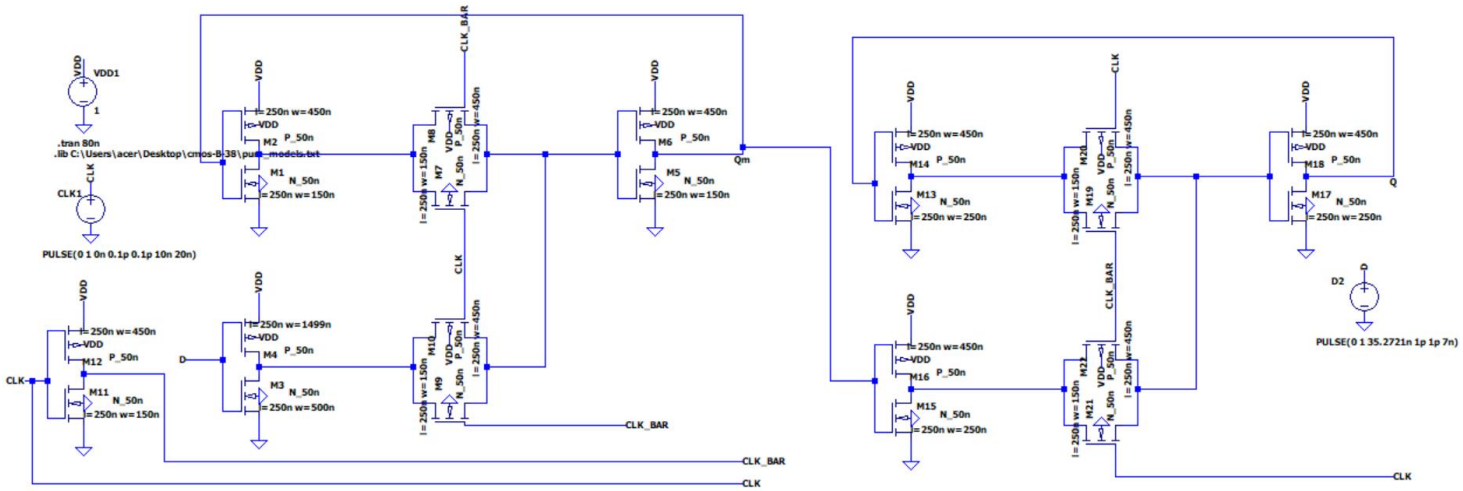
Lab-06

1) **Aim:** Implement D F/F. Define and estimate setup time for your design through SPICE simulation.

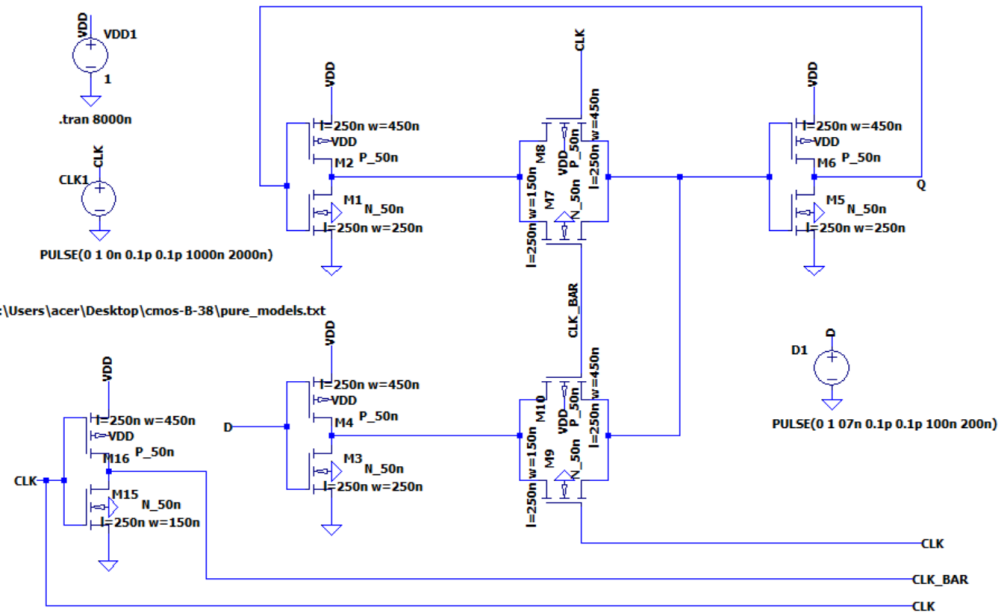
✓ **Software Used: LT Spice**

✓ **Circuit Diagram:**

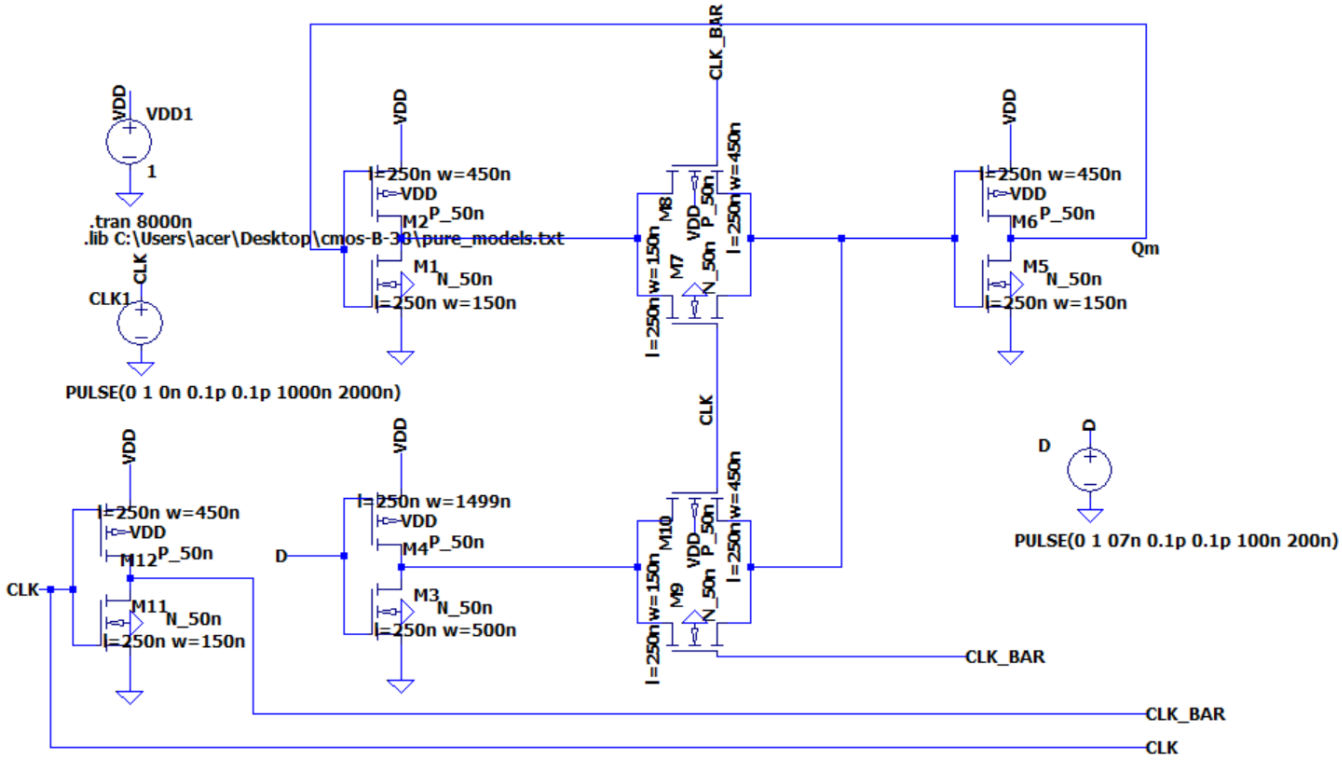
D Flip-Flop



Positive Latch



Negative Latch:



✓ Observation

Table No. 1: DFF (Short Channel)

Observed delay from input to output:

	Relative position (separation) of CLK and D (ns)	$T_{c\text{-}t\text{-}q}$ (ns)	Set-up time of the design (T_{SU}) (ns)
Case 1	2.9883	0.8994(LH)+1.0881(HL)=0.99375	Setup Time =4.1712
Case 2	3.4864	0.8864(LH)+1.086(HL)=0.9862	
Case 3	3.857	0.891(LH)+1.0878(HL)=0.9894	
Case 4	3.8599	0.895(LH)+1.0921(HL)=0.9935	
Case 5	3.9844	0.8901(LH)+1.0869(HL)=0.9885	
Case 6	4.1712	0.8902(LH)+1.0929(HL)=0.9915	

✓ Calculations:

Case 1

T_{PHL} = 61.0907 - 60.0026 = 1.0881ns

T_{PLH} = 40.8892 - 39.9898 = 0.8994ns

T_{PD} = 0.99375ns

Case 2

T_{PHL} = 61.0885 - 60.0025 = 1.086ns

T_{PLH} = 40.8882 - 40.0018 = 0.8864ns

T_{PD} = 0ns

Case 3

T_{PHL} = 61.091 - 60.0032 = 1.0878ns

T_{PLH} = 40.891- 40 = 0.891ns

T_{PD} = 0.9894ns

Case 4

T_{PHL} = 61.092-60.0016 = 1.0920ns

T_{PLH} = 40.87-39.98=0.892ns

T_{PD} = 0.985ns

Case 5

T_{PHL} = 61.0938-60.00164 = 1.0921ns

T_{PLH} = 40.891-39.9960 = 0.895ns

T_{PD} = 0.9935ns

Case 6:

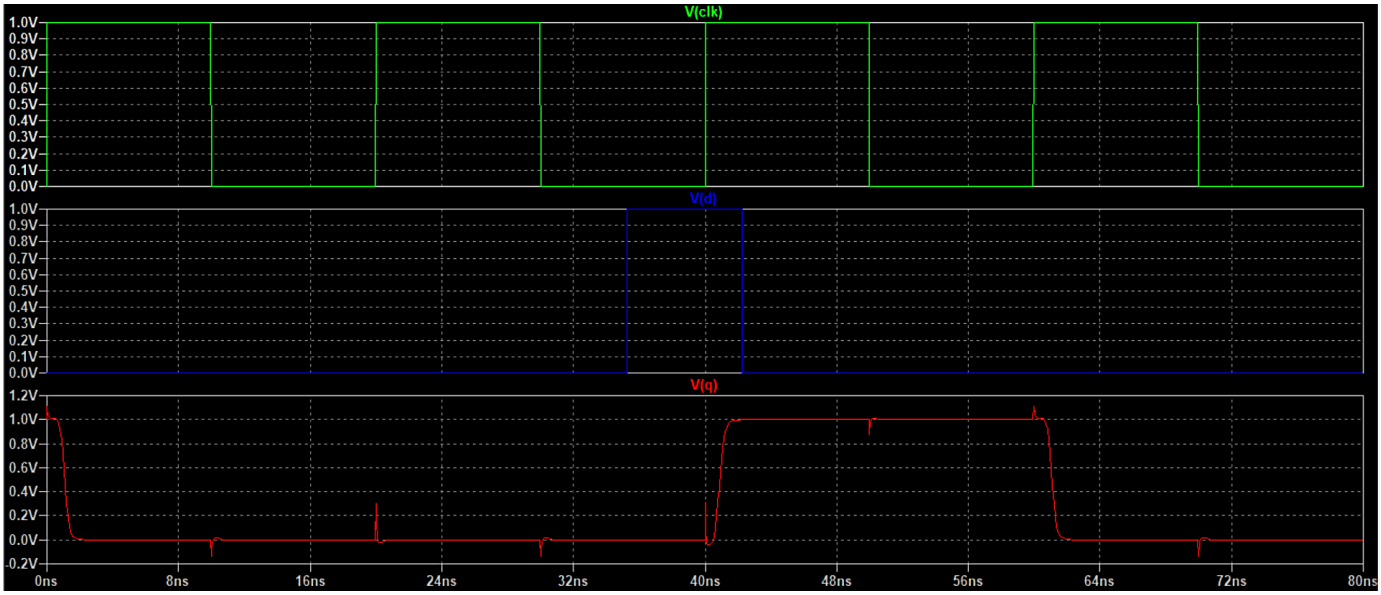
T_{PHL} = 61.0943-60.0014 = 1.0929ns

T_{PLH} = 40.8873-39.9971 = 0.8902ns

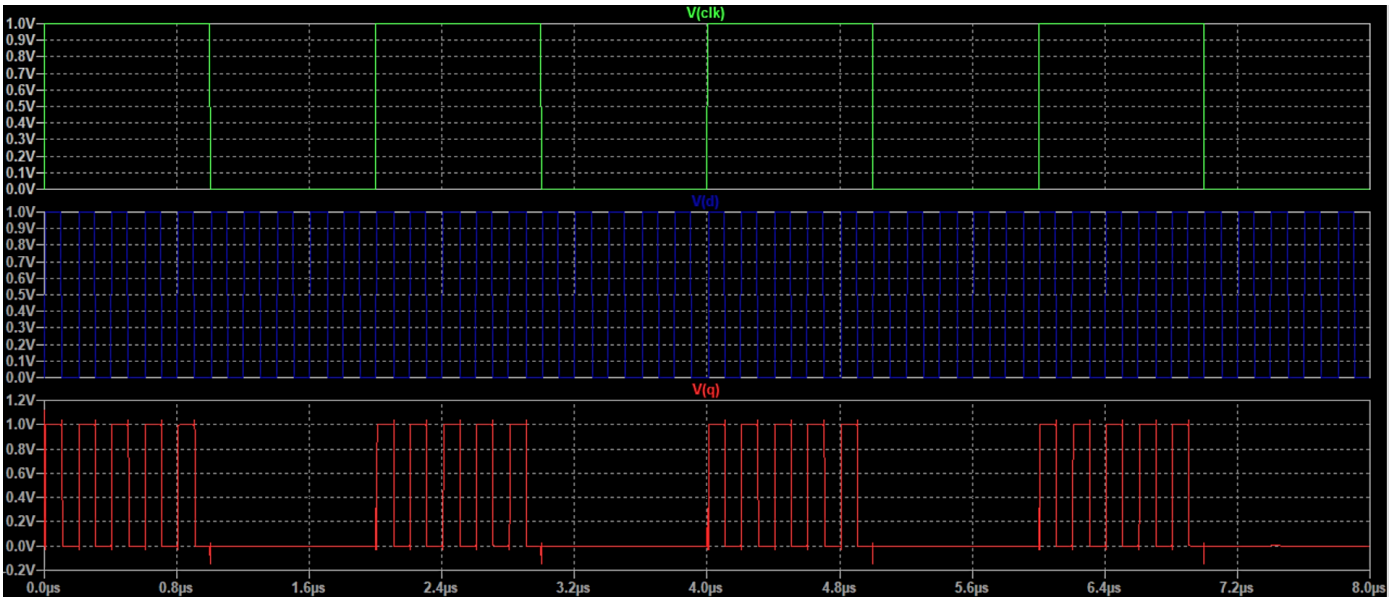
T_{PD} = 0.9862ns

✓ Obtained Waveforms/Simulation Results:

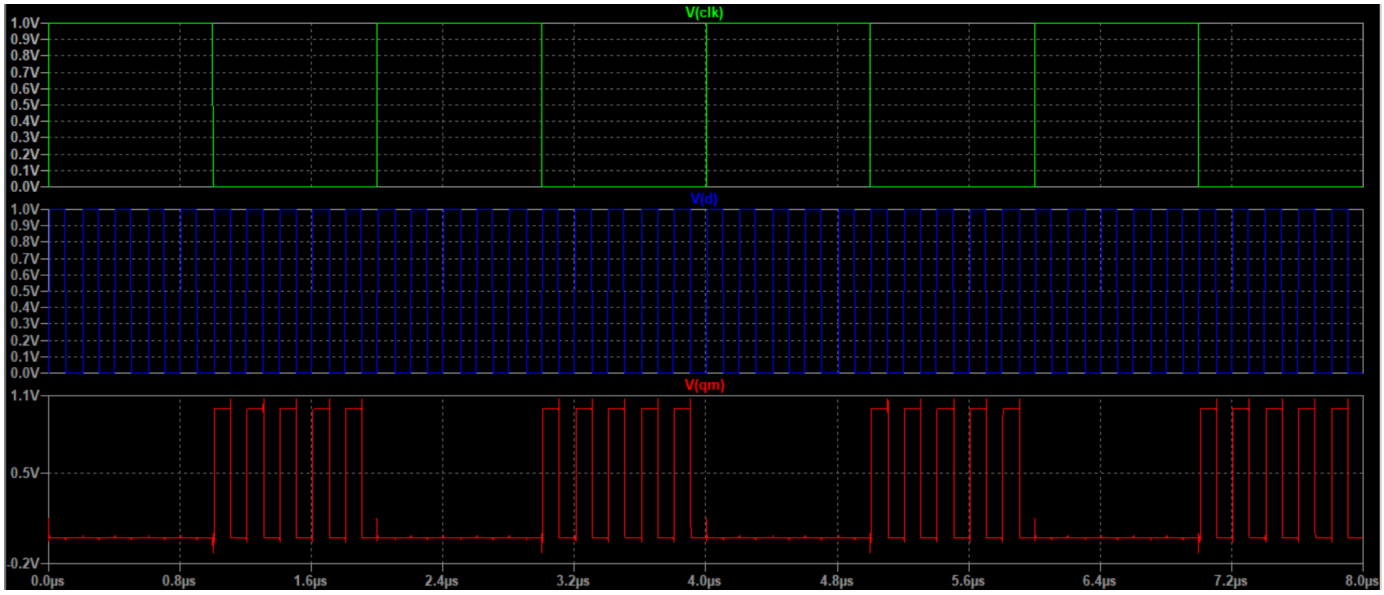
D Flip-Flop:



Positive Latch:



Negative Latch:



✓ Discussion and Conclusion:

From this experiment, we successfully analyze and understand the behavior of the D flip-flop in digital sequential circuit and determine the time required for the input signal to settle before the clock edge arrivals which is known as setup time. In D flip-flop as the distance between clock and D input increases by some parameters than it gives better output.

Batch_A2-22_Lab-No- 06