Shri Ramdeobaba College of Engineering and Management, Nagpur-13.

Department of Electronics Engineering

ENP402 –CMOS VLSI Design Lab

Odd Semester – 2023-24

Lab 02

Calculation of noise margin and dynamic power consumption.

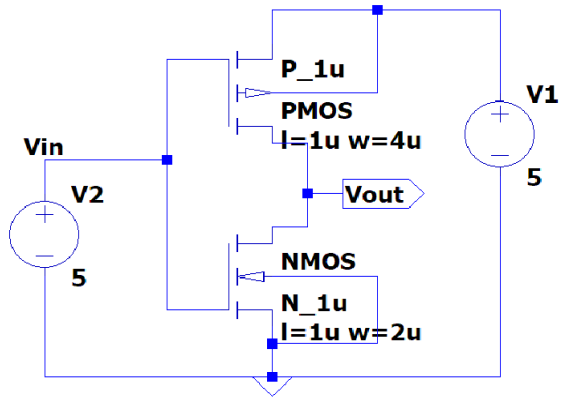
Name:	Harsh Mishra
Batch / Roll No.	A2_22
Semester/Section:	Sem V-A
Date of Performance:	07/10/23
Date of Submission:	10/10/23
Name & Signature of Faculty	Prof. Prachi Rane

Lab-02

Aim: Using SPICE, plot the transfer characteristics for the inverter seen in Fig.2 in both the long- and short-channel CMOS technology. From the plot, determine V_M, V_{IL}, V_{0H}, and V_{0L}. Calculate noise margin in both the cases. Use VDD=5V for long channel devices and VDD=1V for short channel devices. Comment on dynamic power consumption.

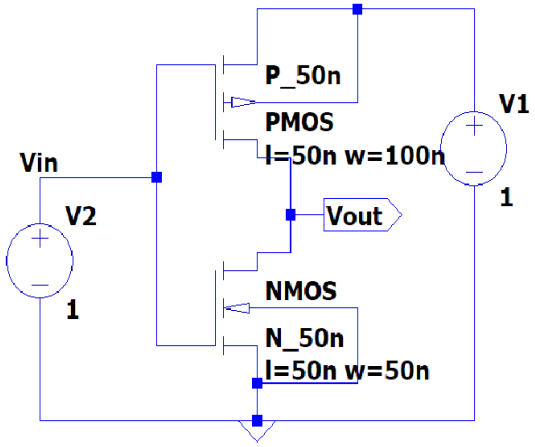
- **Software Used: LTspice ● Circuit Diagram:**

(A) For Inverter (Long Channel):



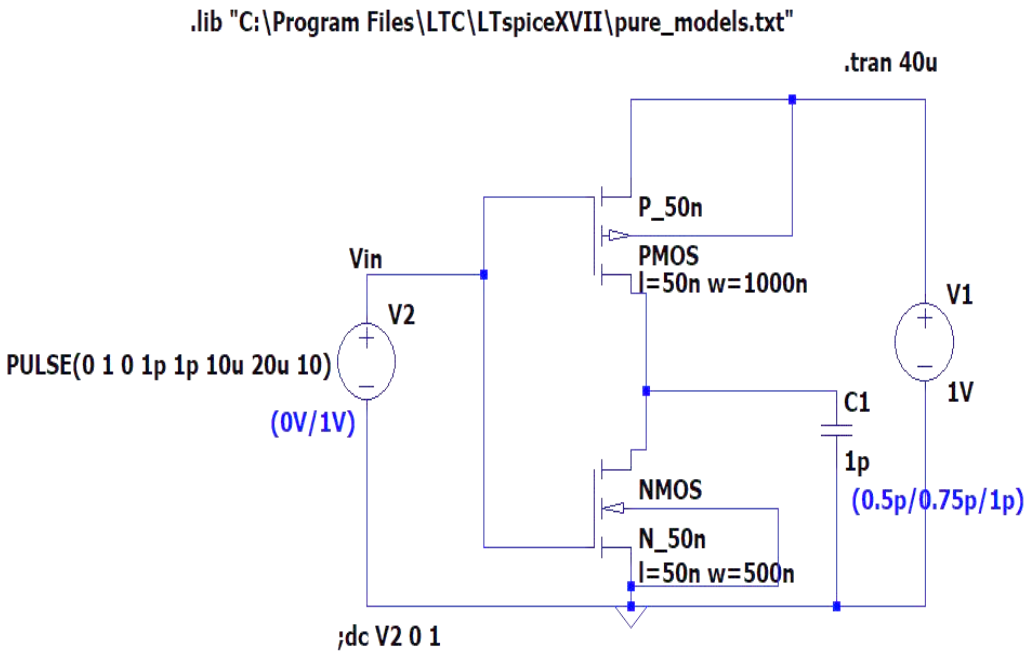
.lib D:\software\pure_models.txt
.dc V2 0 5

(B)For Inverter (Short Channel):



.lib D:\software\pure_models.txt
.dc V2 0 1

(C)For Dynamic Power Consumption (Short Channel):



- **Observation Table**

(A)For Inverter (Long Channel) (Wn= 1u Ln= 2u) (Wp= 1u Lp= 4u)

Critical Voltages	Values	Switching Threshold of the inverter(Vm)	Noise Margin
V_M	2.4v	2.4v	Nml= Vil - Vol =1.99-0v =1.99v Nmh=Voh -Vih =5-2.72v =2.28v
V_{IL}	1.99v		
V_{IH}	2.72v		
V_{OL}	0v		
V_{OH}	5v		

(B)For Inverter (Short Channel) (Wn=50n Ln=50n) (W=100n L=50n)

Critical Voltages	Values	Switching Threshold of the inverter (Vm)	Noise Margin
V_M	0.49v		
V_{IL}	0.4v		
V_{IH}	0.56v		Nml= Vil - Vol =0.40-0v =0.40v Nmh=Voh -Vih =1-0.56v =0.43v
V_{OL}	0v		
V_{OH}	1v	0.49v	

(C)For Dynamic Power Consumption (Short Channel) (Wn= 50n Ln= 1000n) (Wp= 50n Lp= 500n)

Values of C_L	Power Consumption (Th)	Power Consumption (Pr)
0.5pf	25nW	26.34nW
1pf	50nW	56.75nW

- **Calculations:**

(A) For Inverter (Long Channel):

Vm= Vdd/2= 5/2 = 2.5v

1.Nml = Vil - Vol = 2v - 0v = 2v

2.Nmh= Voh - Vih= 5v - 2.6= 2.4v

(B)For Inverter (Short Channel):

Vm= Vdd/2= 1/2 = 0.5v

1.Nml = Vil - Vol = 0.40v - 0v = 0.40v

2.Nmh= Voh - Vih= 1v -0.57v = 0.43v

(C) For Dynamic Power Consumption (Short Channel):

1.For 0.5pF-

PRACTICAL:

Total avg power = 54.26nW
Static power = -21.21nW(0v)
-6.761nW(1v)
Total static power = 21.21nW + 6.761nW= 27.93nW

Dynamic power = 54.26nW - 27.93nW = 26.33nW

THEORETICAL:

Dynamic power = Cl* Vdd^2 *f
=0.5*10^-12*(1/20 *10^-6)
=25nW

2.For 1pF-

PRACTICAL:

Total avg power =84.67nW
Static power = -21.21nW(0v)
-6.761nW(1v)
Total static power = 21.21nW + 6.761nW= 27.93nW

Dynamic power = 84.67nW - 27.93nW = 56.75nW

THEORETICAL:

Dynamic power = Cl* Vdd^2 *f
=1*10^-12*(1/20 *10^-6)

=50Nw

3.For 5pF-

PRACTICAL:

Total avg power =295.17nW

Static power = -21.21nW(0v)

-6.761nW(1v)

Total static power = 21.21nW + 6.761nW= 27.93nW

Dynamic power = 295.17nW - 27.93nW = 267.25nW

THEORETICAL:

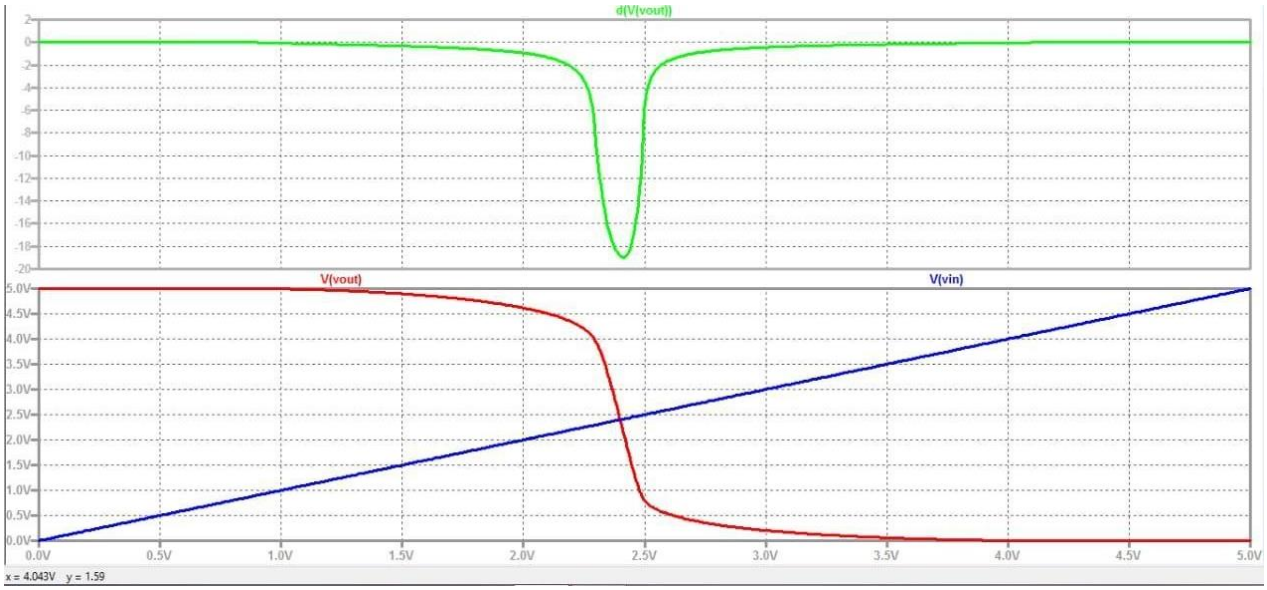
Dynamic power = Cl* Vdd^2 *f

=5*10^-12*(1/20 *10^-6)

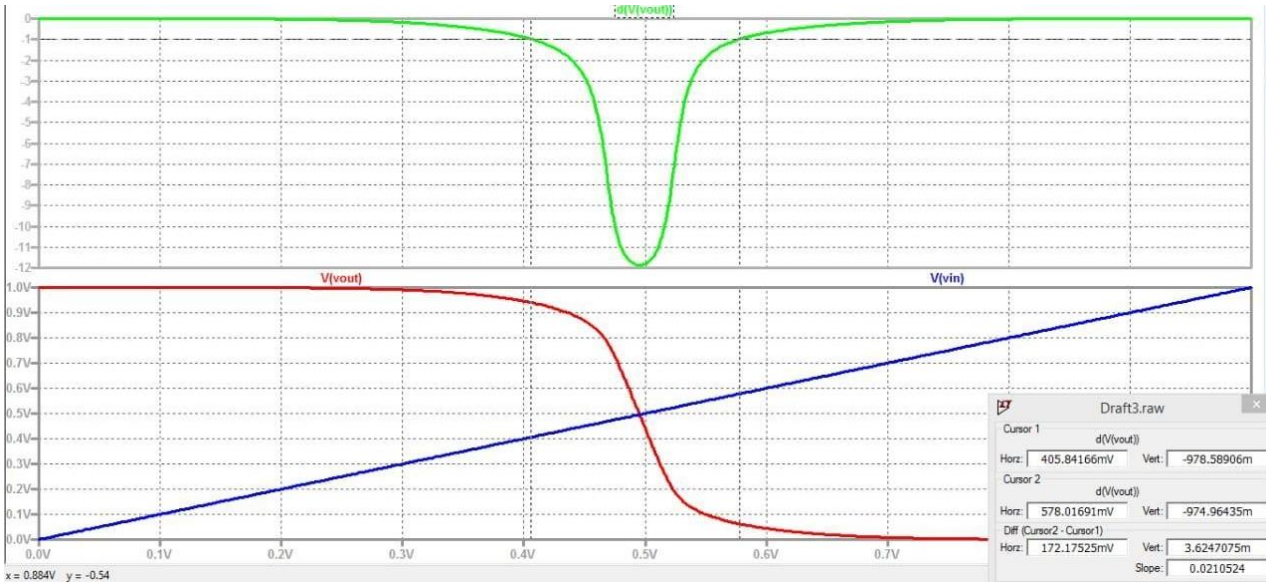
=250nW

- **Obtained Waveforms/Simulation Results:**

(A) For Inverter (Long Channel):

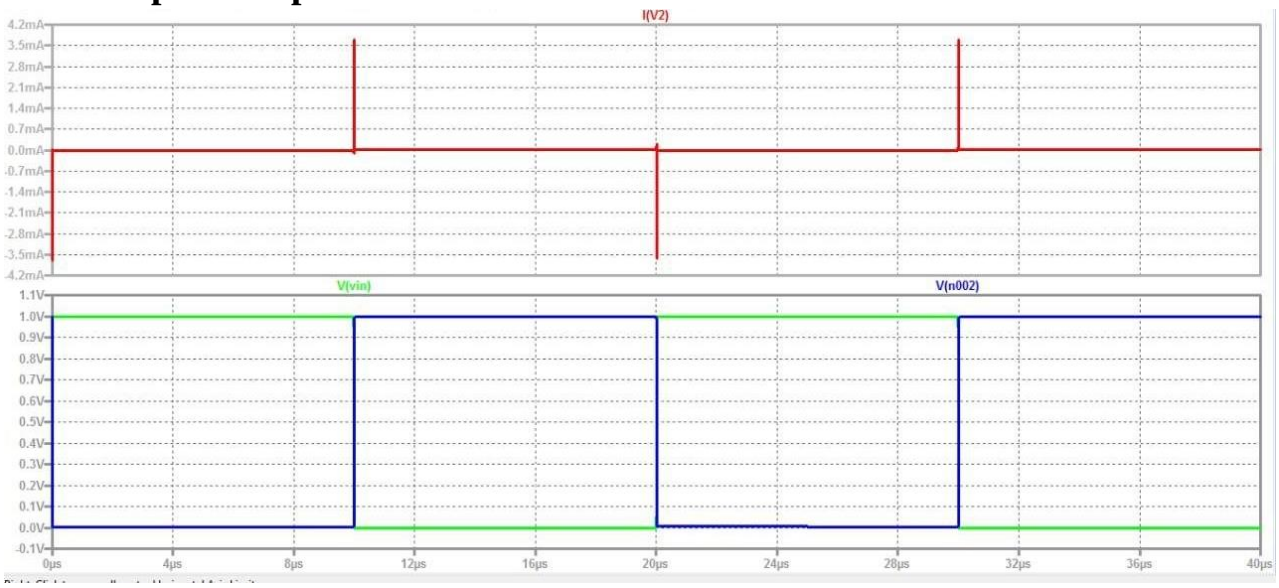


(B)For Inverter (Short Channel):

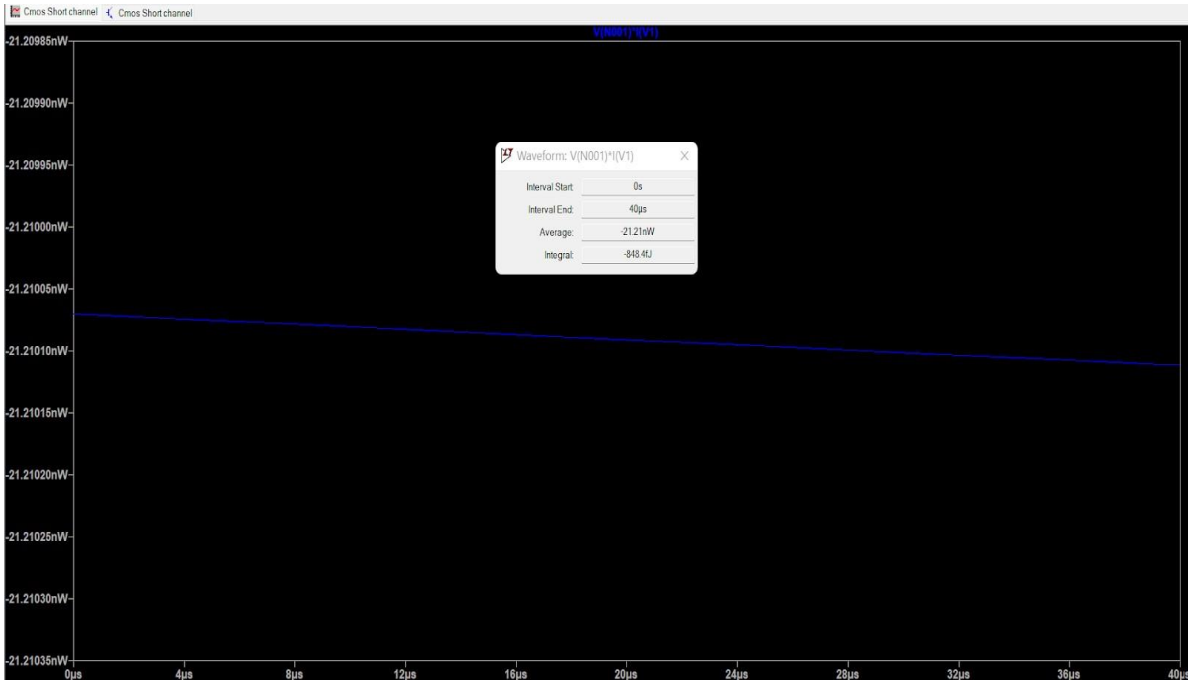


(C)For Dynamic Power Consumption (Short Channel):

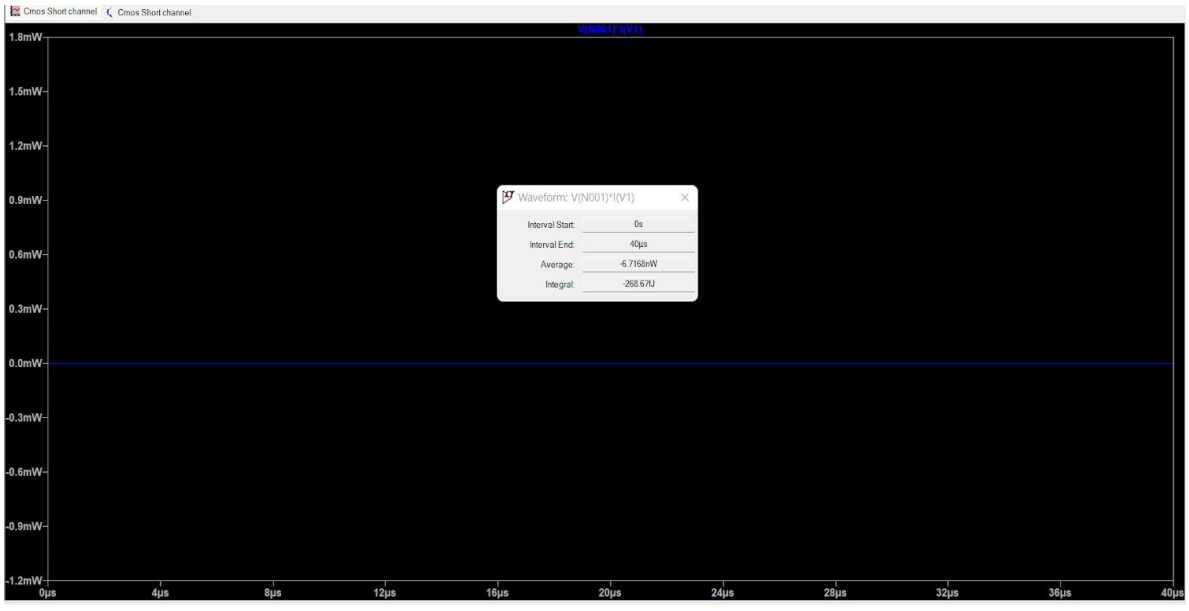
1. For pulse response-



2.For static power(0v)-



3.For static power(1v)-



- **Discussion and Conclusion:** 1) The Noise margin and threshold voltage of long channel is greater than that of short channel. This applies that the short channel CMOS circuit is more sensitive to noise

  2)As we increase the value of the capacitor, power consumption increases. The power consumption of CMOS is proportional to the square of the power supply voltage (V2) and the capacitive load. Therefore, by reducing the power supply voltage, we can significantly reduce power consumption.

Batch_A2-22_Lab-No- 02