Shri Ramdeobaba College of Engineering and Management,

Nagpur-13.

Department of Electronics Engineering

ENP352 –CMOS Digital Circuit Design Lab

Lab 04

Layout Design

Odd Semester – 2023-24

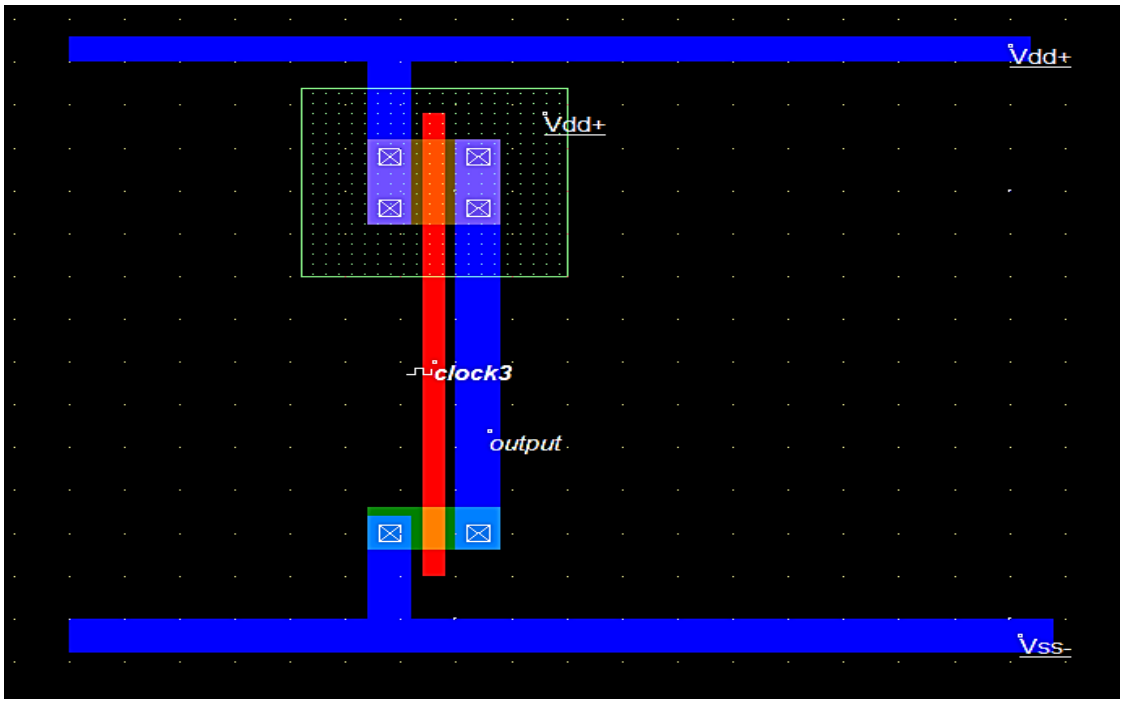
Name:	Harsh Mishra
Batch / Roll No.	A2-22
Semester/Section:	Vth/A
Date of Performance:	02/12/23
Date of Submission:	02/12/23
Name & Signature of Faculty	Prof. Prachi Rane

Lab-04

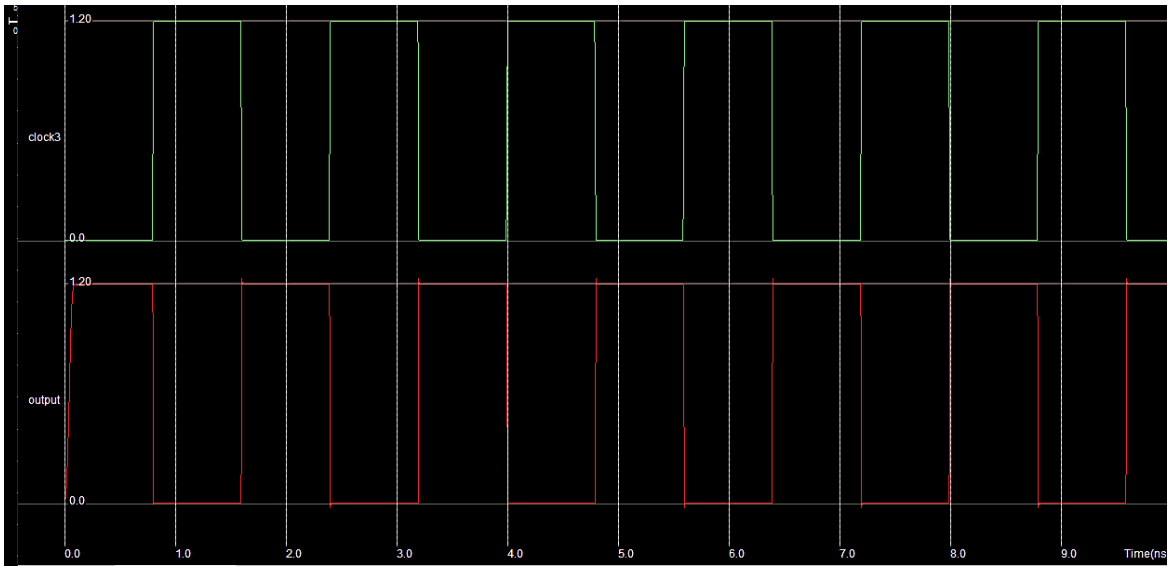
1) **Aim:** Draw the layout of inverter designed for equal rise and fall time and extract the layout and simulate the netlist in SPICE (250nm CMOS process).

Software Used: Microwind3.1

✓ Layout Diagram:



✓ Obtained Waveforms/Simulation Results:



CIRCUIT example

```
*
* IC Technology: CMOS 90nm, 6 Metal Copper - strained SiGe - LowK
*
VDD 1 0 DC 1.20
Vclock3 6 0 DC 0 PULSE(0.00 1.20 0.79N 0.01N 0.01N 0.79N 1.60N)
*
* List of nodes
* "output" corresponds to n°3
* "clock3" corresponds to n°6
*
* MOS devices
MN1 0 6 3 0 N1 W= 0.25U L= 0.10U
MP1 1 6 3 1 P1 W= 0.50U L= 0.10U
*
C2 1 0 0.330fF
C3 3 0 0.416fF
C4 1 0 0.611fF
C6 6 0 0.022fF
*
*
* n-MOS BSIM4 :
* low leakage
.MODEL N1 NMOS LEVEL=14 VTHO=0.28 U0=0.060 TOXE= 1.2E-9 LINT=0.015U
+K1 =0.450 K2=0.100 DVT0=2.300
+DVT1=0.570 LPE0=23.000e-9 ETA0=0.080
+NFACTOR= 0.9 U0=0.060 UA=3.400e-15
+WINT=0.005U LPE0=23.000e-9
+KT1=-0.060 UTE=-1.800 VOFF=0.010
+XJ=0.150U NDEP=170.000e15 PCLM=1.100
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p
*
* p-MOS BSIM4:
* low leakage
.MODEL P1 PMOS LEVEL=14 VTHO=-0.32 U0=0.027 TOXE= 1.2E-9 LINT=0.015U
+K1 =0.450 K2=0.100 DVT0=2.300
+DVT1=0.570 LPE0=23.000e-9 ETA0=0.080
+NFACTOR= 1.9 U0=0.027 UA=2.200e-15
+WINT=0.005U LPE0=23.000e-9
+KT1=-0.060 UTE=-1.800 VOFF=0.010
```

```
+XJ=0.150U NDEP=170.000e15 PCLM=0.700
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p
*
* Transient analysis
*
* (Winspice)
.options temp=27.0
.control
tran 0.1N 5.00N
print V(3) V(6) > out.txt
plot V(3) V(6)
.endc
```

✓ Discussion and Conclusion:

Hence, we successfully designed and plot the layout of n-mos and p-mos also for inverter in microwind software

Batch-A2-22_Lab-04