Shri Ramdeobaba College of Engineering and Management,

Nagpur-13.

Department of Electronics Engineering

ENP352 –CMOS Digital Circuit Design Lab

Lab 07

Memory Elements

Odd Semester – 2023-24

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Batch / Roll No.	A-22
Semester/Section:	Vth/A
Date of Performance:	25/11/23
Date of Submission:	02/12/23
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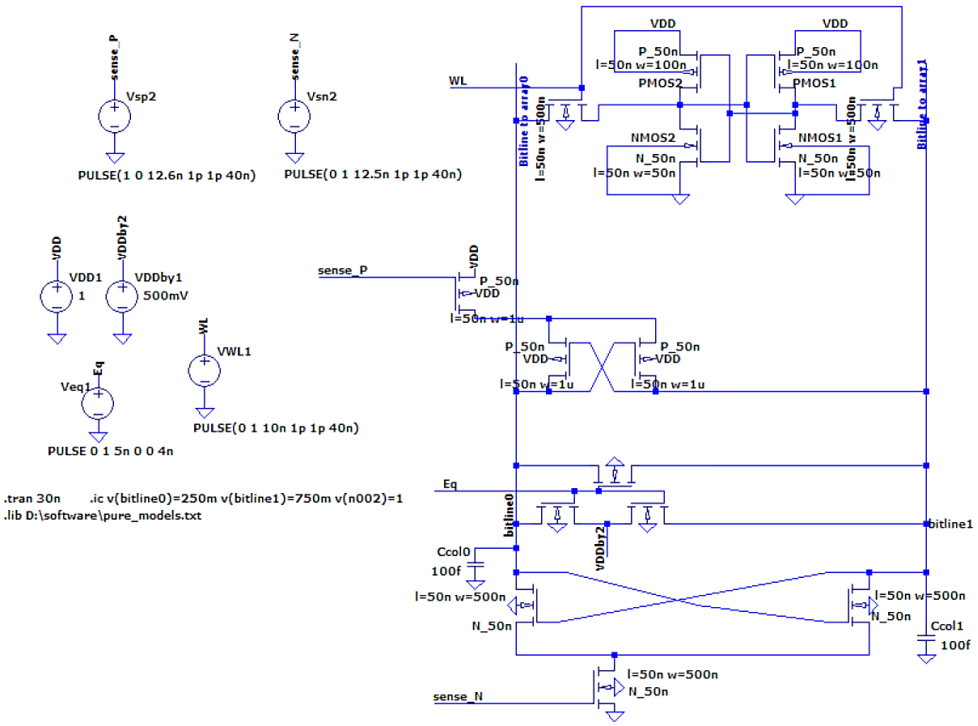
1) **Aim:** To design and simulate SRAM cell with sense amplifier circuit.

✓ **Software Used: LTspice**

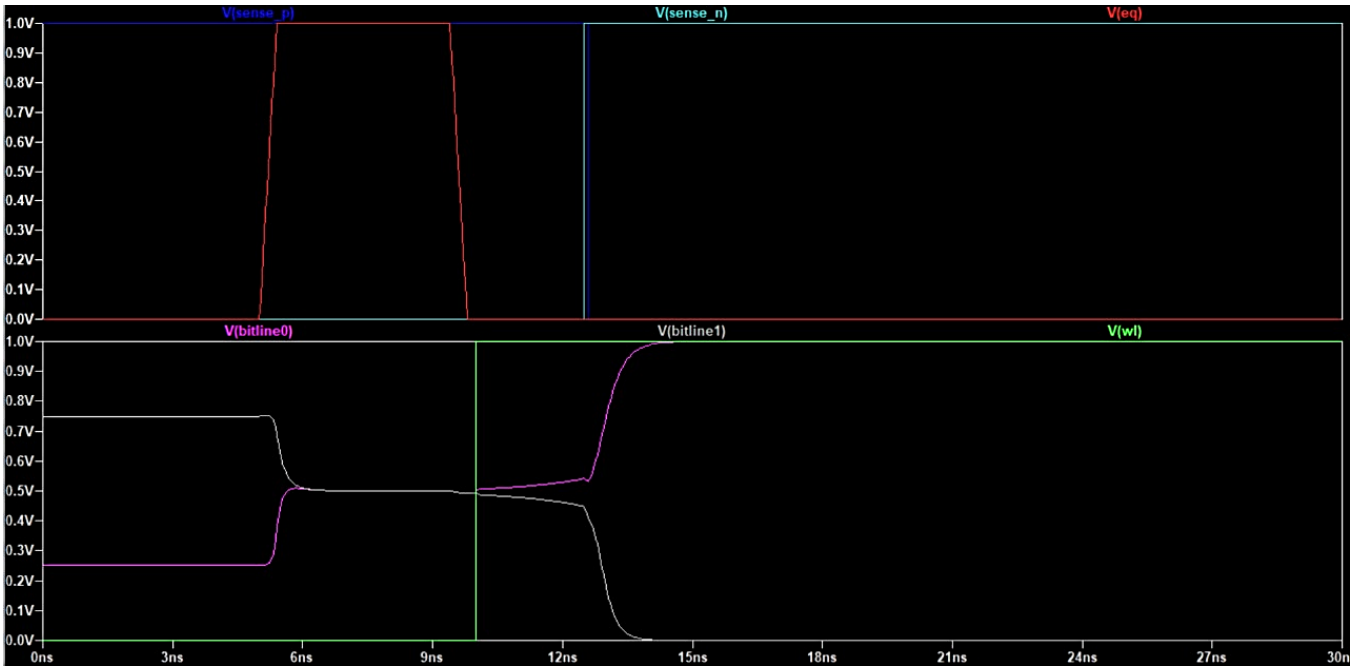
Schematic Simulation:

The memory circuit is said to be static if the stored data can be retained indefinitely (as long as a sufficient power supply voltage is provided), without any need for a periodic refresh operation. The circuit structure of simple SRAM cell, as well as the PSA and NSA (PMOS Sense amplifier/ NMOS sense Amplifier) circuits is shown in Fig.1. When a memory cell is accessed (WL, the word [row] line goes high), the data from the cell (a charge) is placed on the bit line. The bit line voltage changes. At this point we know the bit line looks like a capacitor and that only one word line can go high at a time in a memory array. The voltage movement on the bit line, ΔVbit, may be very small so determining if the voltage is moving upwards or downwards is done with help of sense amplifier (PMOS Sense amplifier/ NMOS sense Amplifier).
We start any sense operation by equilibrating the bit lines (the inputs to the sense amplifier).

✓ **Circuit Diagram:**



✓ Obtained Waveforms/Simulation Results:



✓ Discussion and Conclusion:

From this experiment we have successfully created a memory using six transistor SRAM cell to stored 1bit of data. To make it fully functional memory we can write on it and whatever we write it could be readable by the user. A cross coupled inverter used with two extra transistors they help to write on memory bit line and word line are required.

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