3 BIT SYNCHRONOUS UP COUNTER

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Declaration

We, the students of B. Tech. of Computer Science & Engineering Department hereby declare that we own the full responsibility for the information, results etc. provided in this PROJECT titled "**3 BIT SYNCHRONOUS UP COUNTER**" submitted to Siksha 'O' Anusandhan University, Bhubaneswar for the partial fulfillment of the subject Digital Logic (CSE 1011). We have taken care in all respect to honor the intellectual property right and have acknowledged the contribution of others for using them in academic purpose and further declare that in case of any violation of intellectual property right or copyright we, as the candidate(s), will be fully responsible for the same.

Abstract

Electronic counters are of two types: Asynchronous and Synchronous. Here we will work on Synchronous counter. Synchronous counters use a common clock and logic between the flip-flops to encode the count sequence. Asynchronous counters are simpler because they do not require logic gates, but any latency will scale linearly with respect to the number of bits. Synchronous architecture is preferable. If the application is not sensitive to false errors produced by latency, however, an asynchronous counter alone or with overclocking (in the event that cumulative latency is greater than the cycle time) may be feasible. Alternatively, filters, such as a strobing circuit, can be used to remove erroneous outputs caused by latency from the output.

Contents

Introduction

A synchronous counter is one whose output bits change state simultaneously, with no ripple. In these types of counters, the flip flops are clocked at the same time by a common clock pulse. Thus, all the flip flops change state simultaneously (in parallel). It advances upward in sequence (0, 1, 2, 3, 4, 5, 6, 7). The counter advances to the next output state on the positive edge of the input clock. The outputs of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input disables the counting action and causes the data at the data inputs to be loaded into the counter on the positive-going edge of the clock. A LOW level at the master reset input sets all the four outputs of the flip-flops to LOW level after the next positive-going transition on the clock input. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

Problem Statement

Synchronous counters are used in digital clocks and in multiplexing. The most common Synchronous counters is machine motion control, the process in which the rotary shaft encoders convert the mechanical pulses into electric pulses. These pulses will act as clock input of the counter and will initiate the circuit motion.

Here we will design a 3-bit up counter using T Flip Flop.

Methodology

For designing a 3-bit synchronous up counter we need 3 T Flip Flops, and one AND gate. So, the ICs needed are -

1. Quad 2 Input AND Gate (IC 7408)
2. Master Slave Dual J-K Flip Flop (IC 7473)

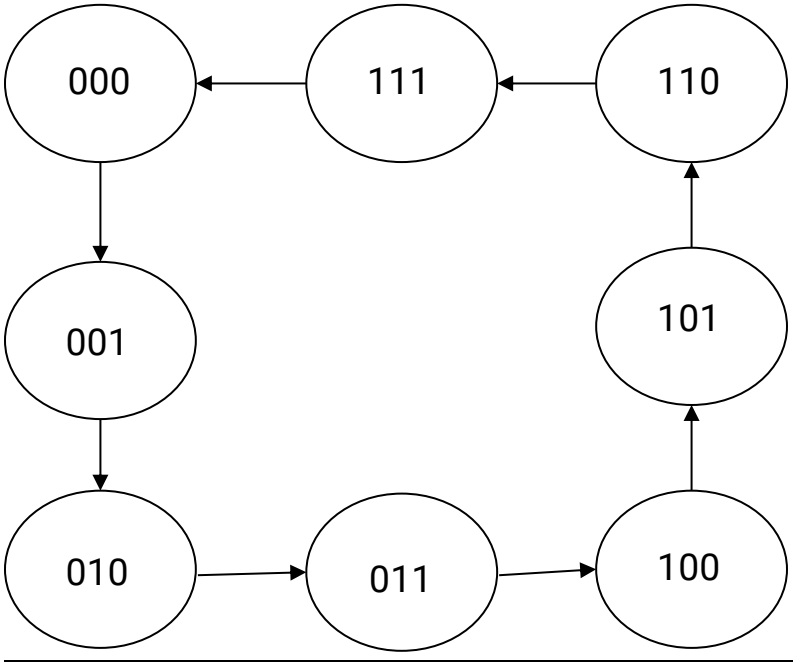
EXCITATION TABLE FOR T FLIP FLOP

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

TRUTH TABLE FOR AND GATE

A	B	F = A.B
0	0	0
0	1	0
1	0	0
1	1	1

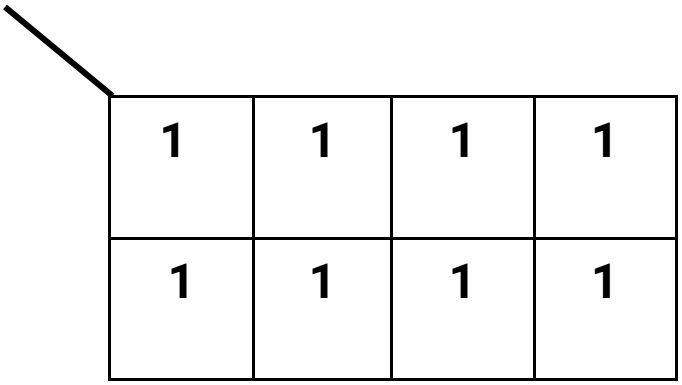
STATE DIAGRAM



CIRCUIT EXCITATION TABLE

Q_C	Q_B	Q_A	Q^*_C	Q^*_B	Q^*_A	T_C	T_B	T_A
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

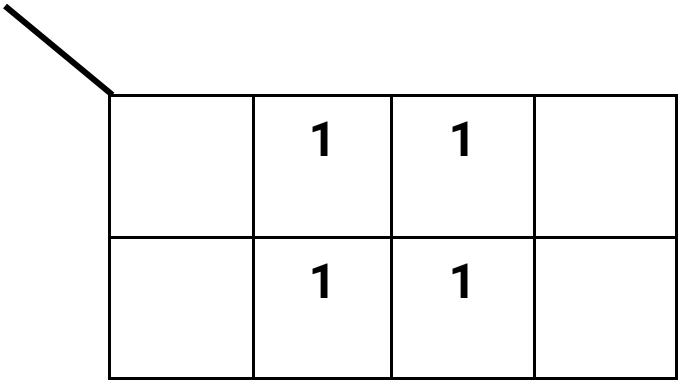
K-MAP FOR T_A -



1	1	1	1
1	1	1	1

$$T_A = 1$$

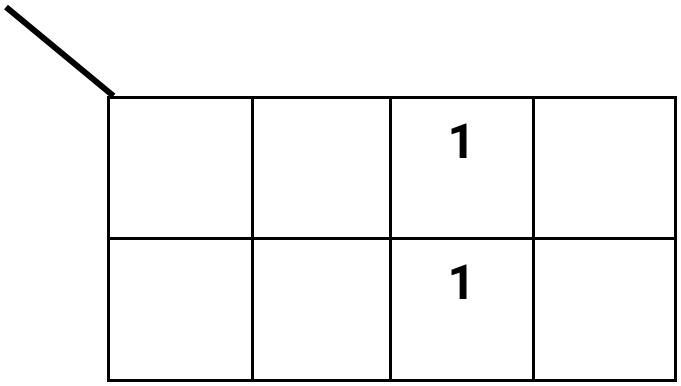
K-MAP FOR T_B -



	1	1	
	1	1	

$$T_B = Q_A$$

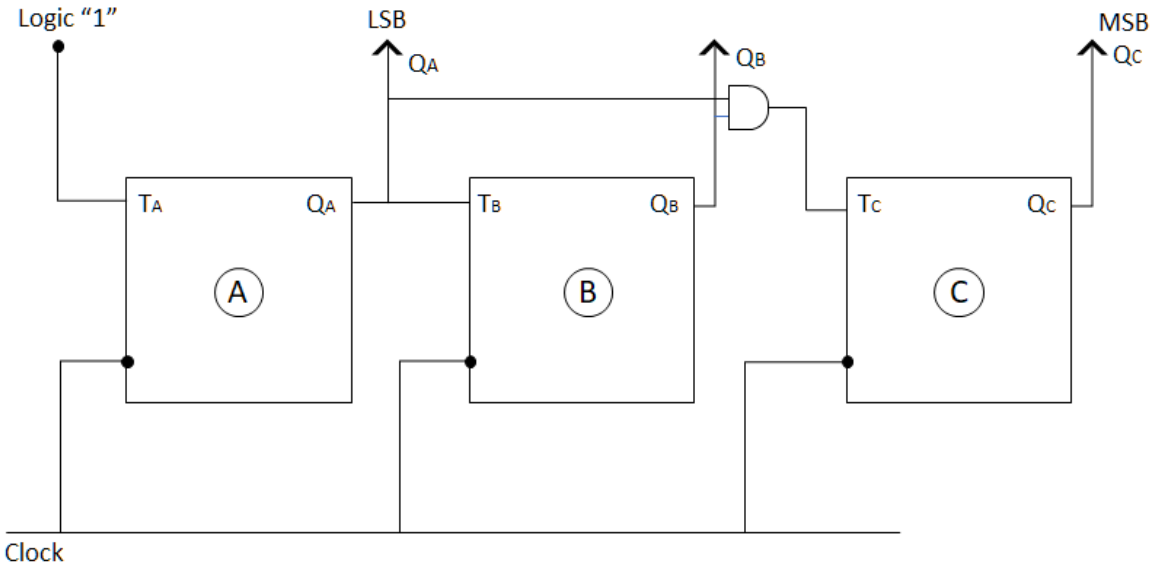
K-MAP FOR T_C -



$$T_C = Q_B Q_A$$

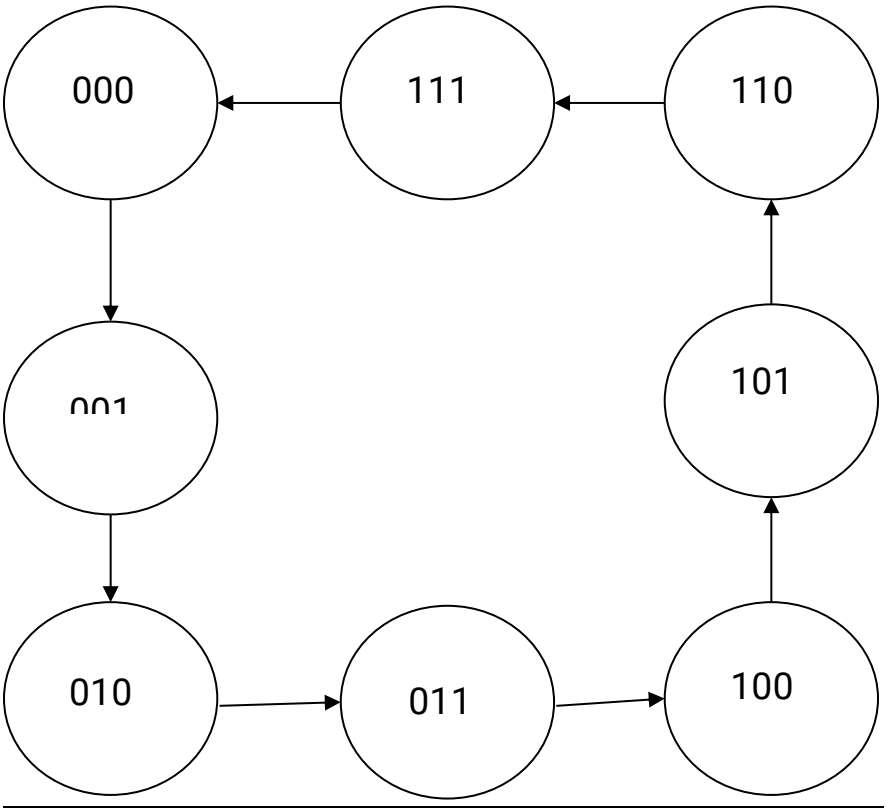
Implementation

CIRCUIT DIAGRAM



Results & Interpretation

OUTPUT STATE DIAGRAM



Conclusion

All we did was design a 3 Bit Binary Up-Counter using Two Master Slave J-K Flip flops and One And Gate. This project can surely be applied into places like People Counter in malls, Parking Counters in big parking areas, and small components like Real Time clocks.

All of the gates were triggered by one common clock pulse. In short, counter itself is the widest application of Flip Flops. This project is one instance of it.

References

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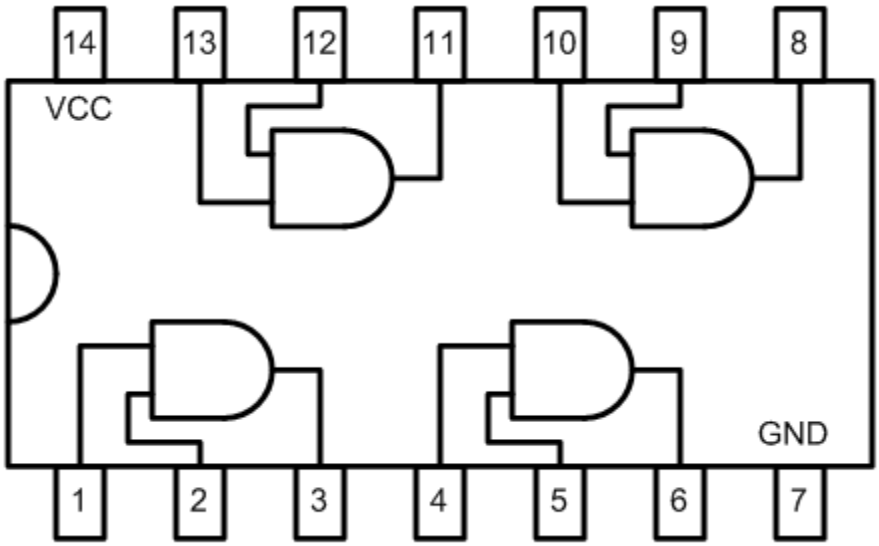
Appendices

IC 7408 (Quad 2 Input AND Gate)



IC 7473 (Master Slave JK Flip Flop)