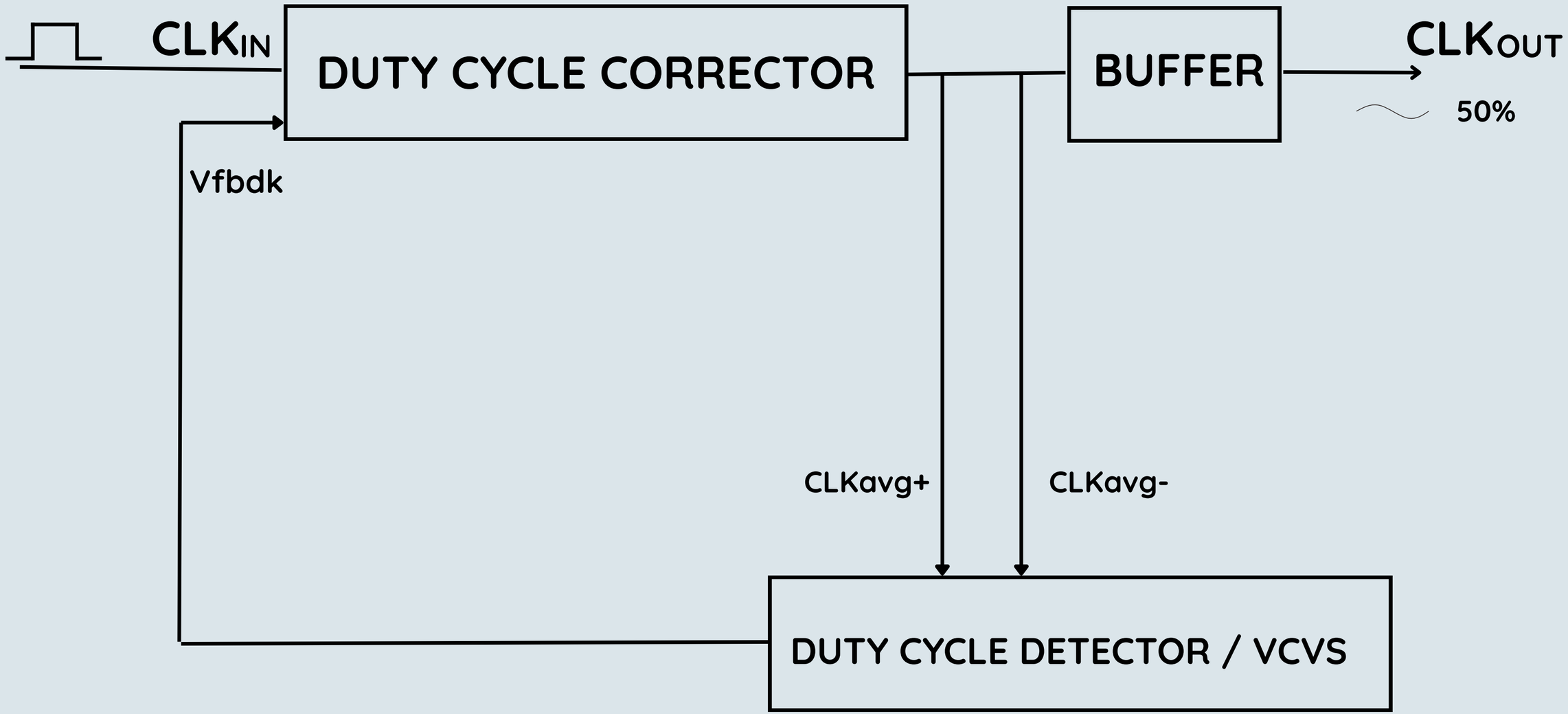
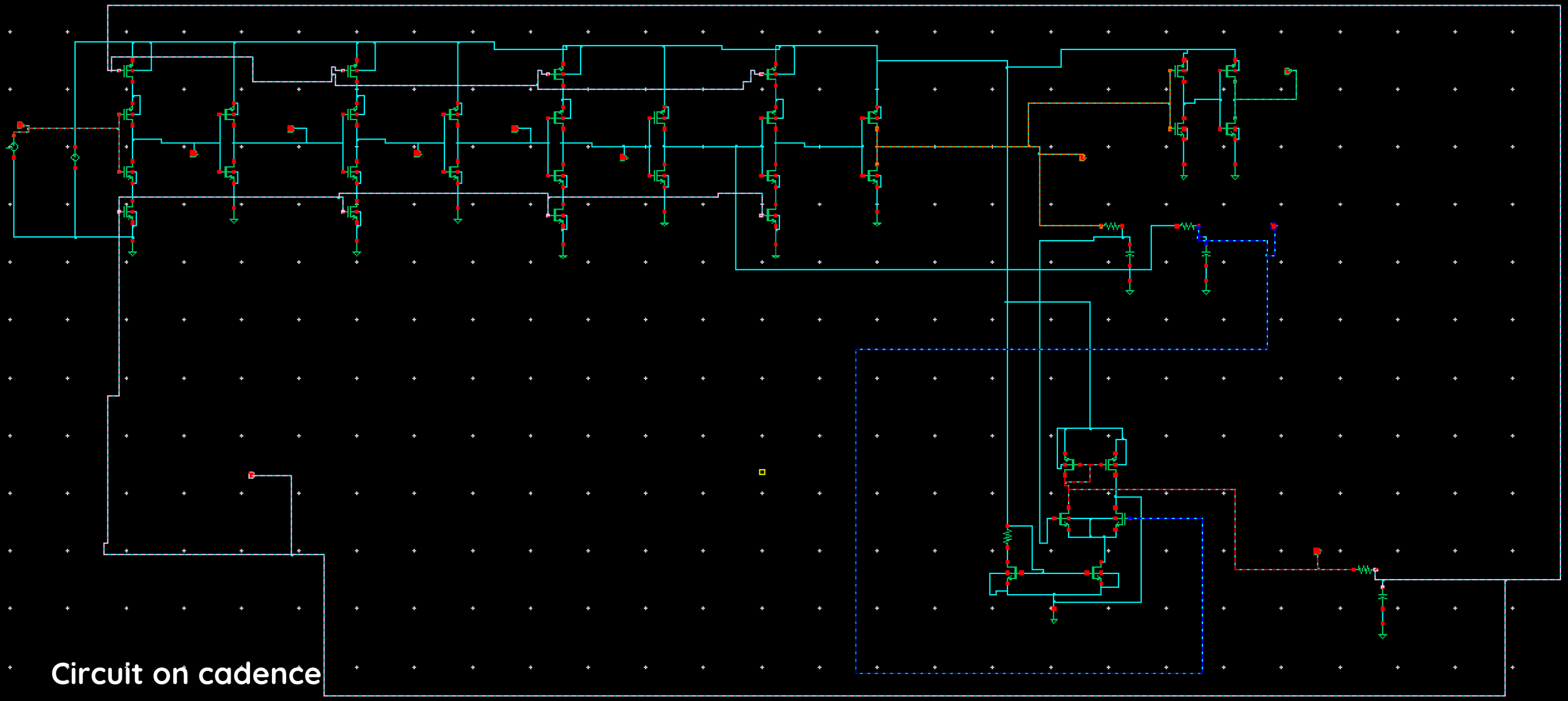
Duty Cycle Correction Circuit

<Analog>

Proposed Circuit Diagram

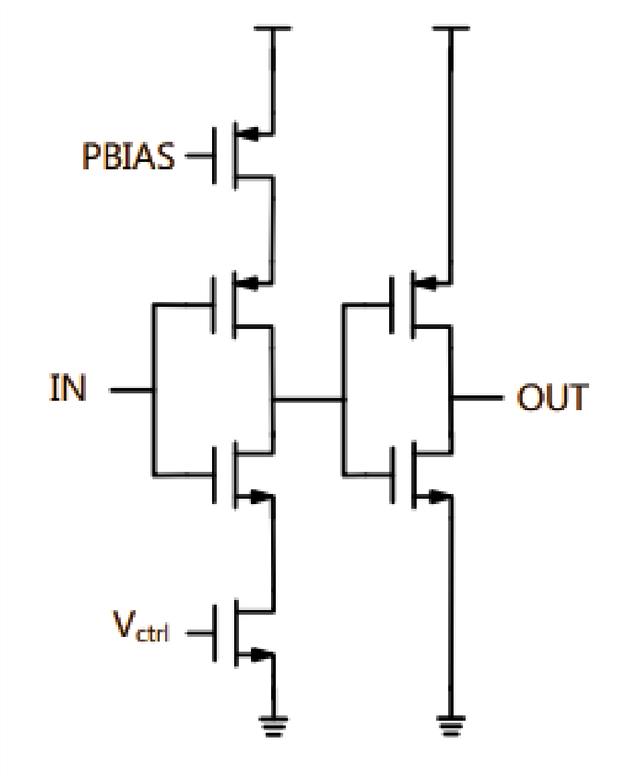




Circuit on cadence

Logic flow step by step

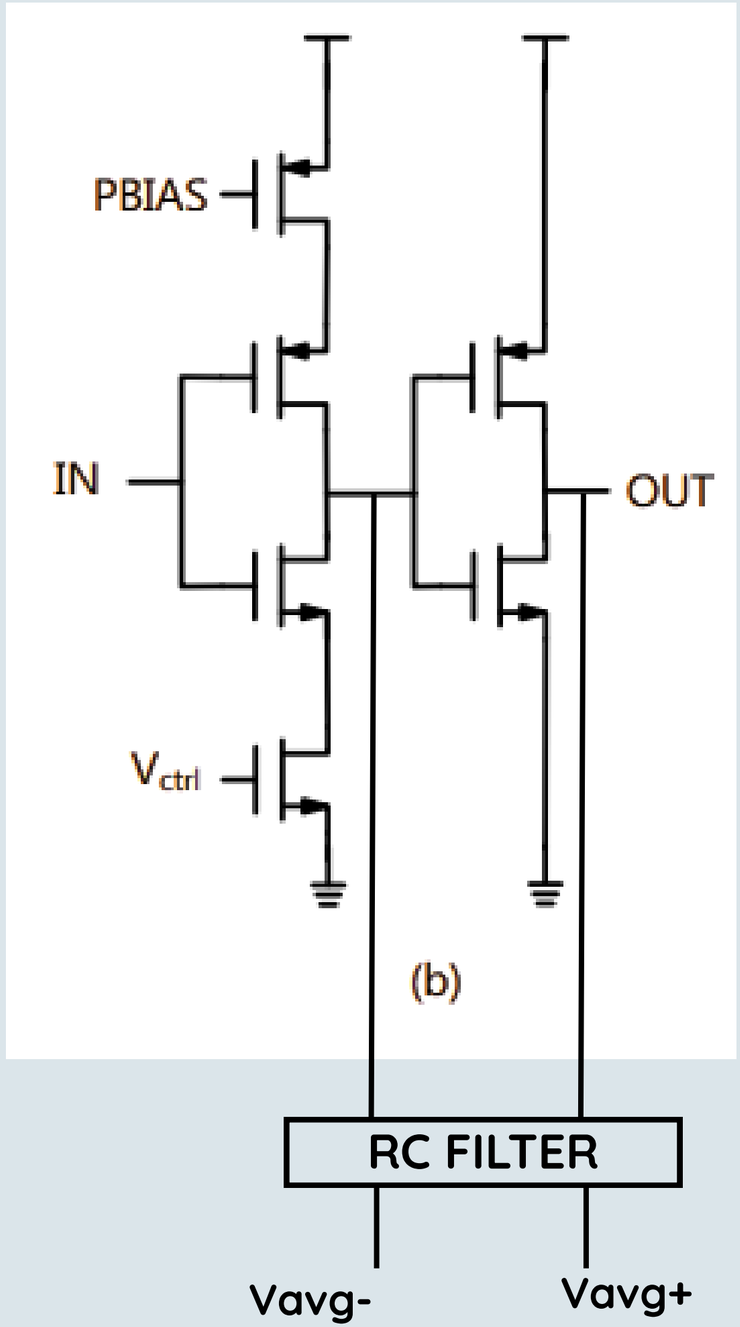
Duty cycle corrector :- The circuit has been taken from the paper. With the help of this circuit we can control the delay of both rising and falling edge of a clock. This triggering of delay of both the edges helps to correct the clock.



WORKING:

The circuit operates by controlling the current available to the inverter during switching transitions1. The additional transistors act as variable resistors that can limit the current flow, thereby affecting the switching speed and pulse width of the output signal.

Logic flow step by step



Duty Cycle Adjustment Process

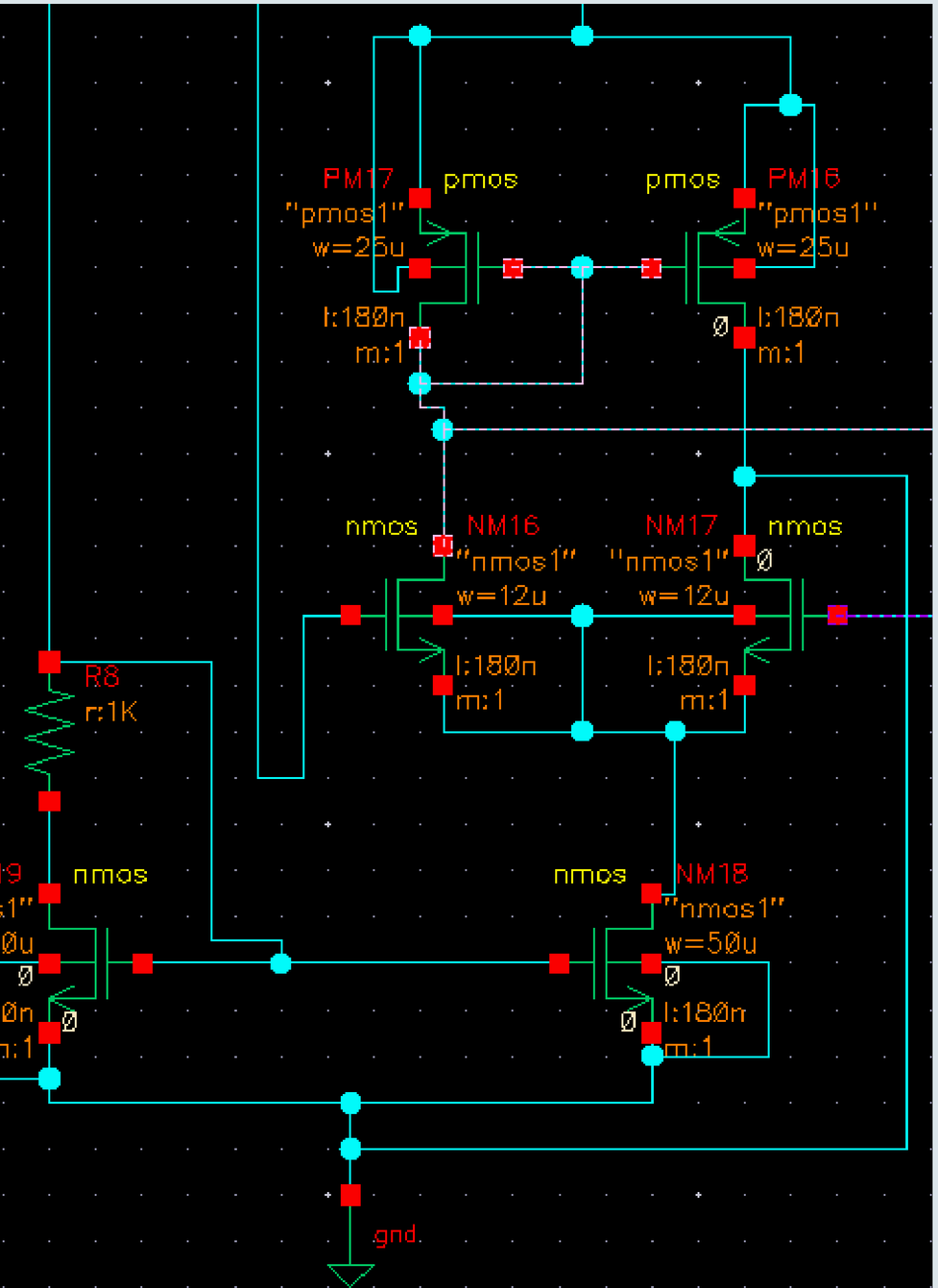
1. **Rising Edge Control**: The PMOS transistor affects how quickly the output can pull up to VDD, controlling the rise time
2. **Falling Edge Control**: The NMOS transistor affects how quickly the output can pull down to ground, controlling the fall time

- **CMOS inverter** is used to invert the corrected clock back to original.

- Our circuit works in a feedback loop which controls the value of both the Vctrl and PBIAS used in corrector circuit.

We have take two feedback inputs which are **Vavg-** and **Vavg+**. These are the averages of the output of the DCC **before CMOS** and **after CMOS** respectively. We have averaged out the clock by using **RC filter circuit**. As our frequency ranges from **10^8 HZ to 10^9 Hz** thus we have taken time constant **10^{-6}** which is very big thus with respect to given time periods i.e. 10^{-9} s to 10^{-8} s thus can be used for aveage out the signal. Thus we have taken the values of **R = 100K** & **C=10ps.**

Logic flow step by step



We have to provide voltage feedback to corrector and incoming inputs are also voltage so we have used vcvs with some gain. We have applied this idea using differential amplifier. Vavg+ & Vavg- are connected to gates of differential amplifier which will take difference of both signal and will output the amplified difference which after filtering is given back to corrector as feedback.

We have used PMOS current mirror as active load and NMOS current source for tail current. By tuning the width of the transistors we have achieved the required gain.

PMOS transistors : $W=25*10^{-6}$ m

NMOS differentials: $W=12*10^{-6}$ m

NMOS tail current: $W=50*10^{-6}$ m

Logic flow step by step

Closed-Loop Operation

1. **Detection: Detector continuously monitors the difference between clock output and its inverse**
2. **Amplification: Any duty cycle error is amplified by the gain**
3. **Correction: The amplified error signal adjusts both VCTRL and PBIAS simultaneously**
4. **Convergence: The loop drives the duty cycle toward 50% where the differential error becomes zero**

Results

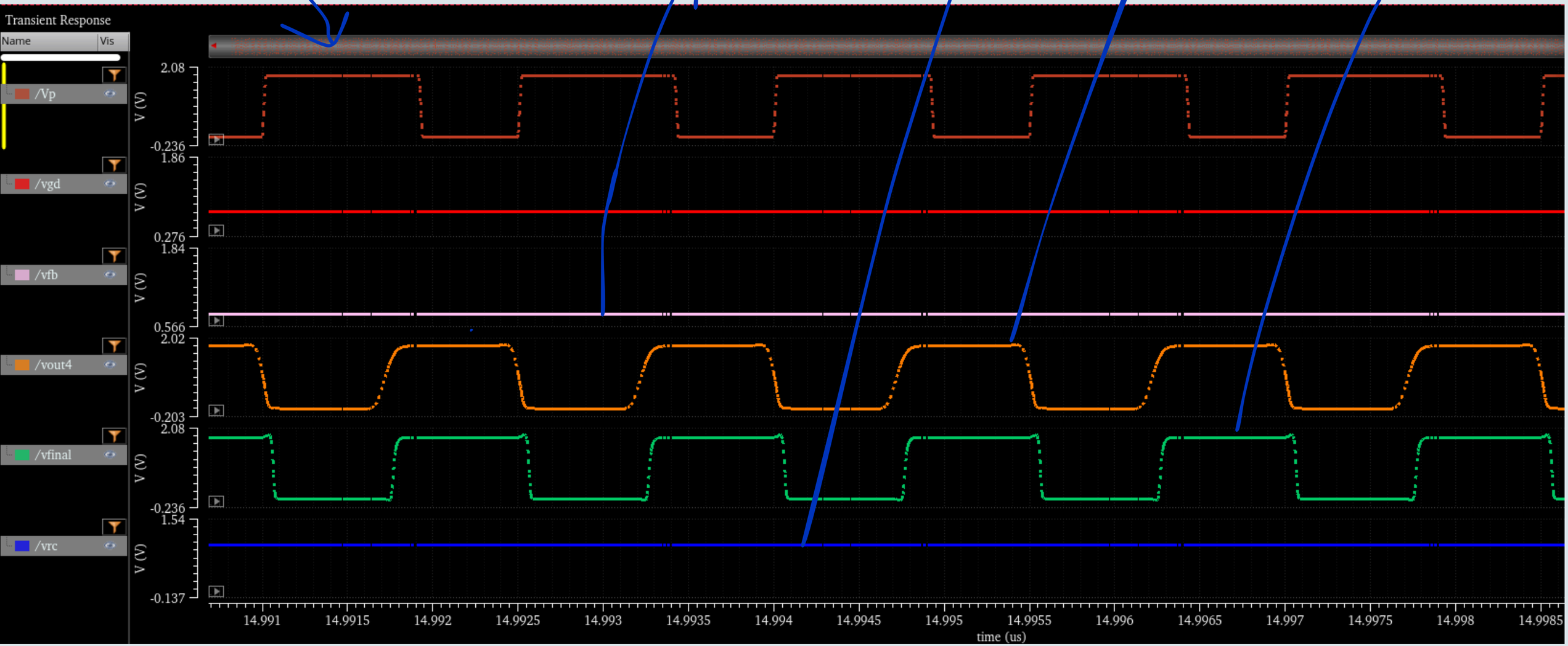
CLOCK INPUT

FEEDBACK(0.79).

after correction Vavg(0.9)

Voutput(~50%)

after buffer



Results

Circuit is working for specified frequencies i.e 0.5GHz to 1GHz but correction range is 35% to 65% and maximum error in the range is 3%. For asked correction range 30% and 60% errors were 6% maximum