NATIONAL INSTITUTE OF TECHNOLOGY, PATNA
END- SEMESTER EXAMINATION, 2022

Program: B.Tech 4th Sem CSE, B.Tech 5th Sem IT
Semester: 4th
Course Code: CS4404/5CS115
Full Marks: 60

Department: CSE
Course Name: Operating Systems
Duration of Examination: 3 hours

ANSWER ALL THE QUESTIONS
Use of GANTT Chart is mandatory in all Questions related to Scheduling
Assume Missing Data If Any

1. A system has 4 processes and 5 allocable resource. The current allocation and maximum needs are as follows-

	Allocated					Maximum				
A	1	0	2	1	1	1	1	2	1	3
B	2	0	1	1	0	2	2	2	1	0
C	1	1	0	1	1	2	1	3	1	1
D	1	1	1	1	0	1	1	2	2	0

If Available = [0 0 X 1 1], what is the smallest value of x for which this is a safe state? (6M)

2. Suppose we want to synchronize two concurrent processes P and Q using binary semaphores S and T. The code for the processes P and Q is shown below-

Process P:
```
while (1)
{
W:
print '0';
print '0';
X:
}
```

Process Q:
```
while (1)
{
Y:
print '1';
print '1';
Z:
}
```

Synchronization statements can be inserted only at points W, X, Y and Z. Which of the following will always lead to an output string with '001100110011'? (6M)

A. P(S) at W, V(S) at X, P(T) at Y, V(T) at Z, S and T initially 1
B. P(S) at W, V(T) at X, P(T) at Y, V(S) at Z, S initially 1 and T initially 0
C. P(S) at W, V(T) at X, P(T) at Y, V(S) at Z, S and T initially 1
D. P(S) at W, V(S) at X, P(T) at Y, V(T) at Z, S initially 1 and T initially 0

3. A certain computer system has the segmented paging architecture for virtual memory. The memory is byte addressable. Both virtual and physical address spaces contain 2^{16} bytes each. The virtual address space is divided into 8 non-overlapping equal size segments. The memory management unit (MMU) has a hardware segment table, each entry of which contains the physical address of the page table for the segment. Page tables are stored in the main memory and consists of 2-byte page table entries. What is the minimum page size in bytes so that the page table for a segment requires at most one page to store it? Also give the division of virtual address. (10M)

4. Consider a system using multilevel paging scheme. The page size is 1 GB. The memory is byte addressable and virtual address is 72 bits long. The page table entry size is 4 bytes. (10M)
Find-
1. How many levels of page table will be required? (2-level)
2. Give the divided physical address and virtual address.

5. Consider a single level paging scheme. The virtual address space is 16 GB and page table entry size is 4 bytes. What is the minimum page size possible such that the entire page table fits well in one page? (6M)

6. Consider the set of 4 processes whose arrival time and burst time are given below-

Process No.	Arrival Time	Burst Time		
		CPU Burst	I/O Burst	CPU Burst
P1	0	3	2	2
P2	0	2	4	1
P3	2	1	3	2
P4	5	2	2	1

If the CPU scheduling policy is Shortest Remaining Time First, calculate the average waiting time and average turnaround time. (6M)

7. Complete the following table- (6M)

Page Size	Page Table Entry Size	Outermost Page Table Size	Levels of Paging	Virtual Address Space Division
4 KB	4 bytes	256 bytes	1	?
4 KB	4 bytes	256 bytes	2	?
4 KB	4 bytes	256 bytes	3	?

8. A system uses 4-page frames for storing process pages in main memory. It uses the Least Recently used (LRU) and Most Recent Used (MRU) page replacement policy. Assume that all the page frames are initially empty. What is the total number of page faults that will occur while processing the page reference string given below- (10M)
7,0,1,2,0,3,0,4,2,3,0,3,2,1,2,0,1,7,0,1.
Also calculate the hit ratio and miss ratio.