cogenda

INTERNSHIP/ INDUSTRIAL TRAINING REFERENCE MANUAL

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Chapter 1: Introduction to Visual TCAD

The tool is design by the Cogenda semiconductors, Singapore. As per the tool is used for Device Modelling, Simulation and Characterization of the Device (transistors and diodes) are done using different methods. Analytical method is used for modeling which consists of closed form equations obtained using spice. Experimental method is required for characterization. Numerical methods which are based on the concept of 2D/3D meshing can be adopted for conducting simulation studies which requires Technology CAD. Different TCAD device simulators are MEDICI, SILVACO (ATLAS), SYNOPSIS (SENTAURAS), and COGENDA (Visual TCAD). Among this 2D/3D simulation is possible using COGENDA TCAD.

Cogenda TCAD consists of Genius powerful simulator and Visual TCAD interactive GUI in which 2-D structures and 3D structures can be created. Circuit simulation is also available in this tool. Core features are provision for advanced device modeling, Circuit schematic capturing, easy device simulation control, versatile device visualization, Syntax highlighted text editor, Spreadsheet and X-Y Plots for 2-D along with Z direction if used in 3-D. Multiple analysis modes such as DC / Transient / AC simulation and optical simulation are there in the tool itself. Advanced setup such as boundary conditions, material parameters, physical models are also available. By using Visual TCAD, One can gain clearer image of understanding semiconductor devices physics and Microelectronics

2-D device structures can be drawn and there are two methods for 3-D device drawing. Either 2-D structure can be drawn and extended to Z Axis or direct 3D structure can be formed using deck (code) format. In extended 3D method, meshes in the Z direction is automatically generated whereas there is provision for defining meshes in X,Y, and Z direction in deck scheme which makes it more accurate and interactive .

Various steps followed for device simulation are:

- Define X, Y, and Z mesh,
- Define regions and corresponding materials,
- Define doping Profile,
- Apply models,
- Apply bias,
- Export the output file

Using the Graphical User Interface

Visual TCAD is the integrated graphical user interface of the Genius device simulation package.

1. To start Visual TCAD in Linux.
   Open the terminal or Press [ctrl+alt+t]
   Type Visual TCAD or the corresponding alias name

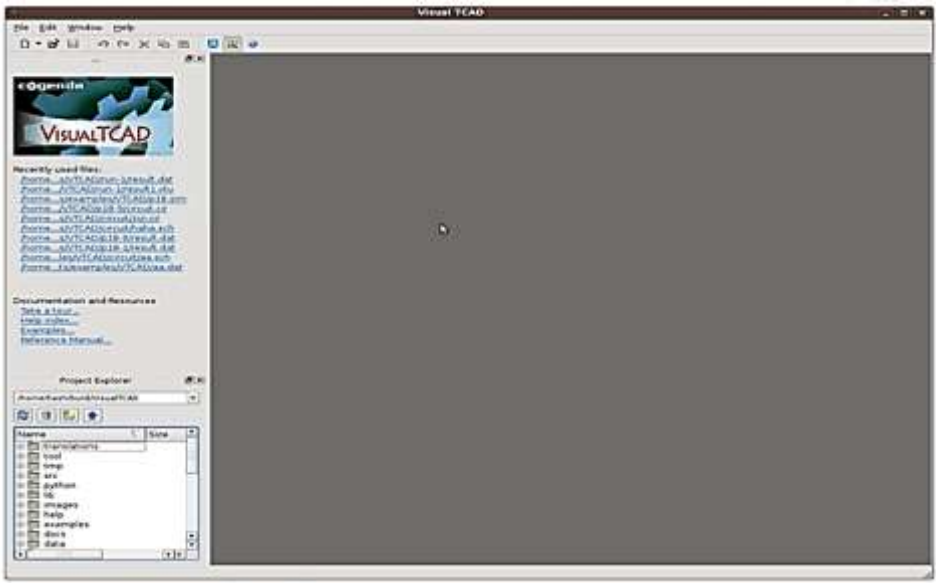

Figure 1:Visual TCAD Dialog Window

2. To draw new structure.
   - Click on file
   - New file
   - Device drawing
3. To write Deck file (code)
   - Click on file
   - New file
   - Text document
4. To do Device simulation
   - Click on file
   - New file
   - Device simulation
5. To Draw circuit schematic
   - Click the menu-File
     - Select→New file
     - Circuit schematic

The software version number and release details can be verified by clicking the → menu → Help → about. The information available through the dialog box is as indicated here.

Figure 2: Dialog Box indicating Visual TCAD Information.

Features of Visual TCAD

1. Advanced Device Drawing Tools

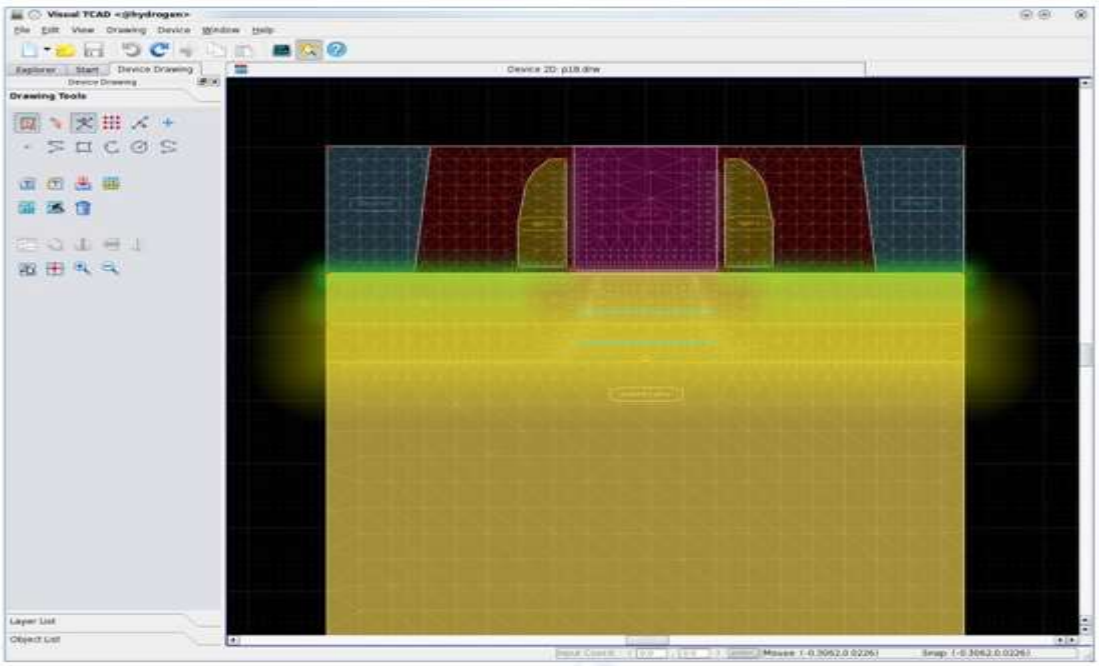

Figure 3: A demo NMOS device with mesh network

2. Easy Simulation Setup

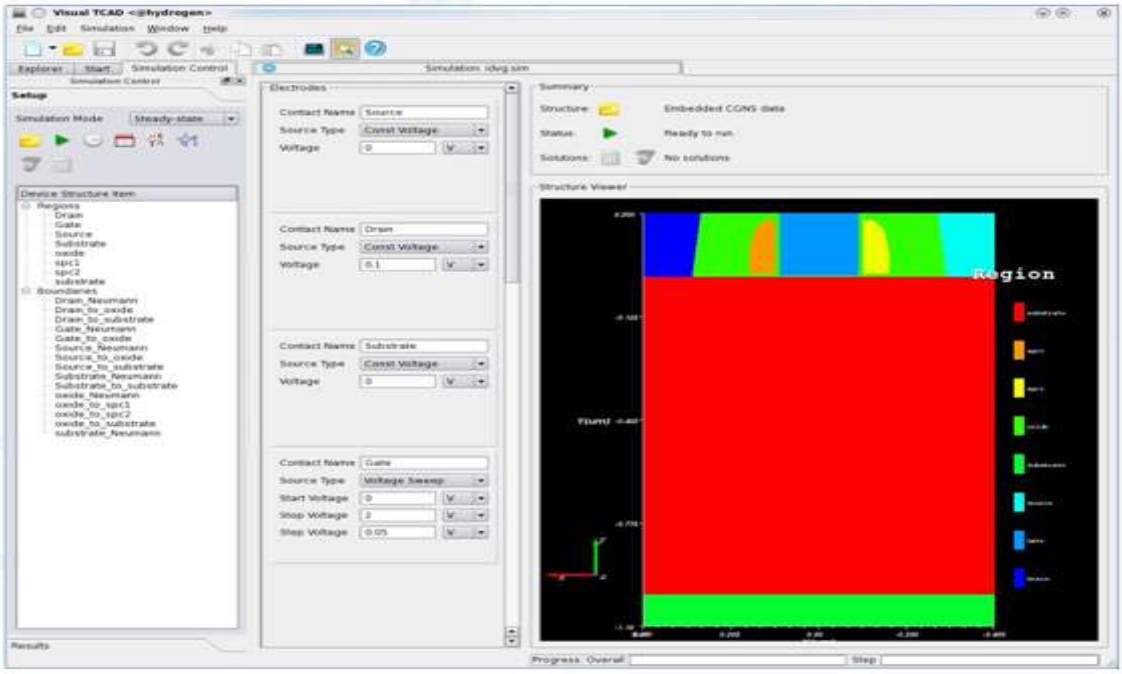

Figure 4: A demo NMOS device with simulation workbench

3. Versatility in Device Visualization

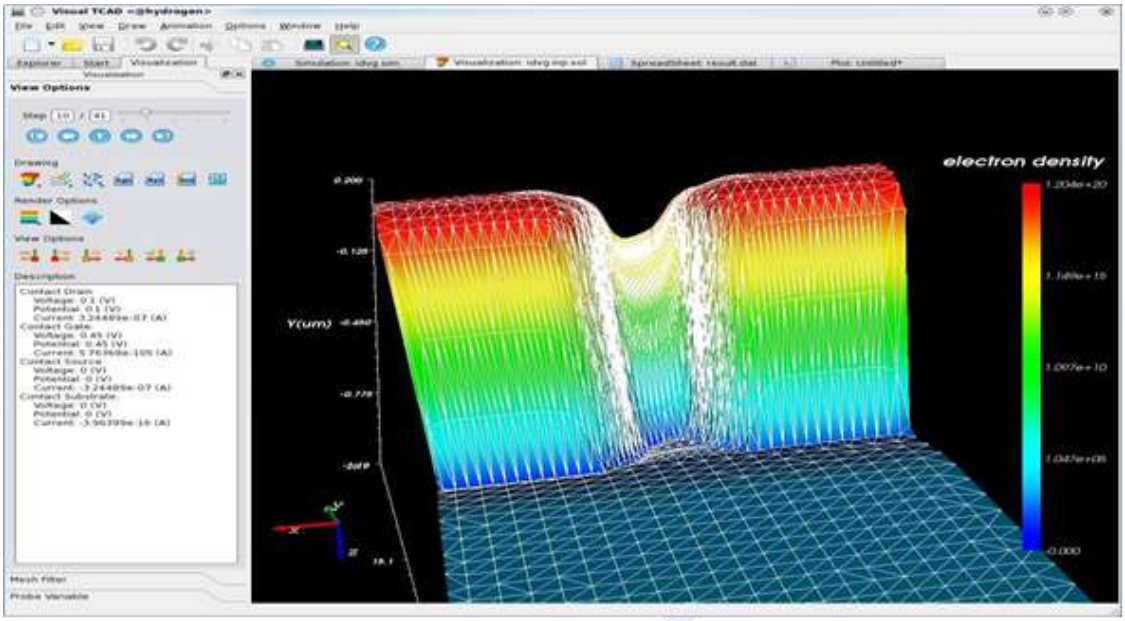

Figure 5:NMOS Device visualization post simulation

4. Keywords Highlighted Text Editor

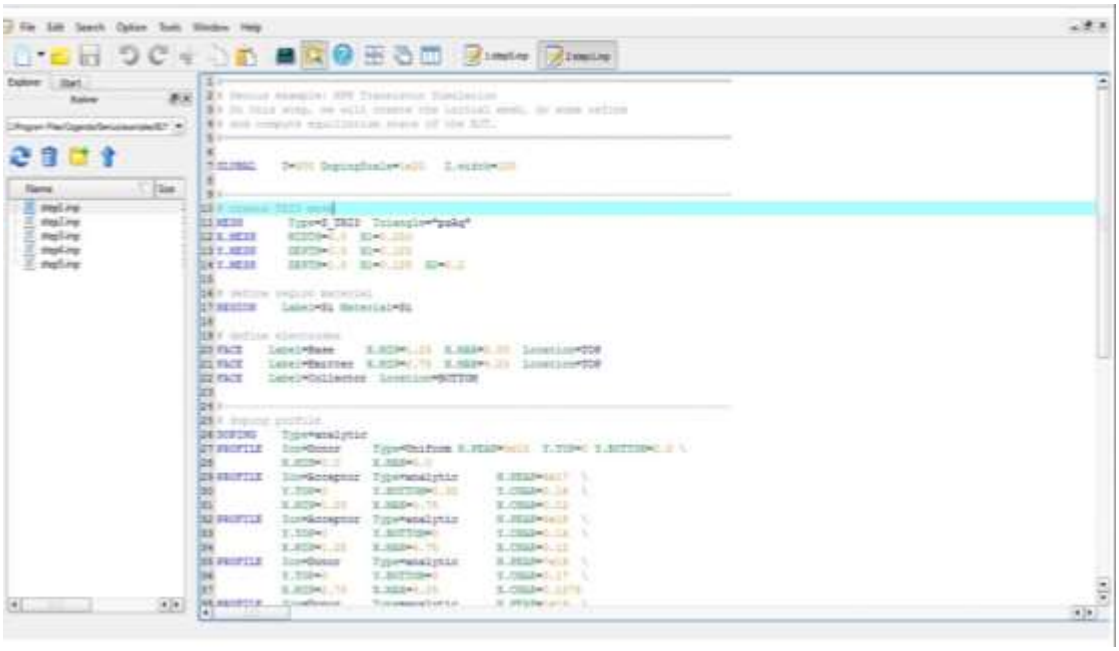

Figure 6: Display of simulation keywords – In Green Colour

5. Data Analysis: Spreadsheet and Plotting

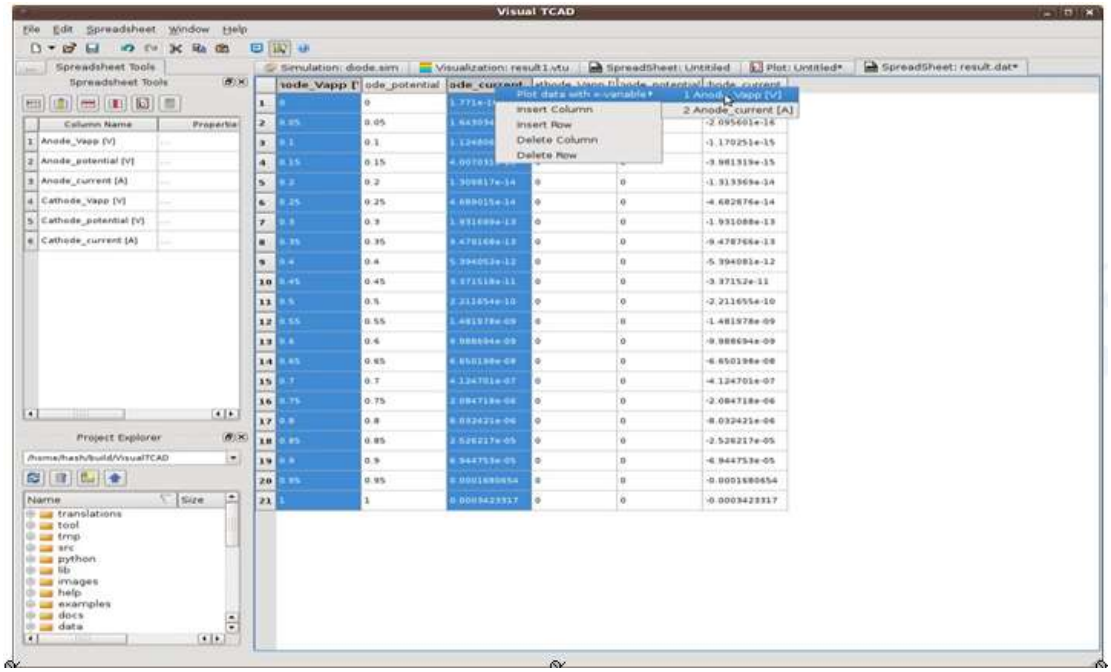

Figure 7: Tabulated Data Post Simulation

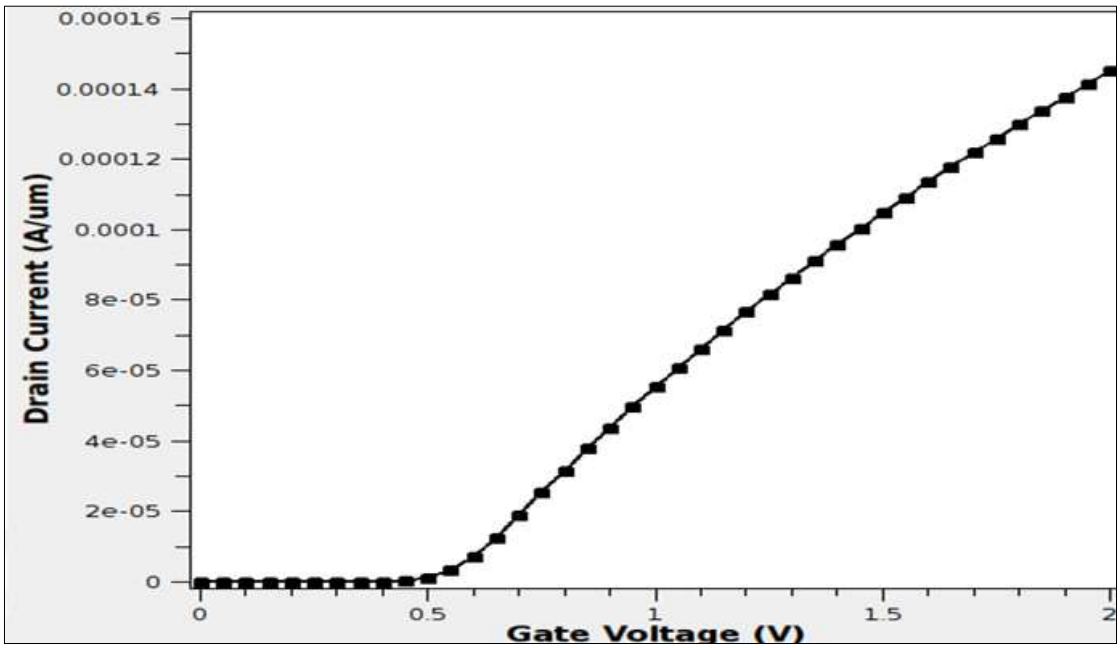

Figure 8 :Plot of data -Post simulation- Input Characteristics of NMOS device.

Chapter 2: PN JUNCTION -DIODE

Objective:

1. To analyse the PN junction VI Characteristics using Visual TCAD 2-D Simulation.
2. To assign custom defined symbol to the device structure and realize circuit schematic using the assigned symbol.
3. To analyse the electrical characteristics of the device connecting as a circuit element.

Pre-requisite: Fundamental Knowledge of P-N junction diode and its Voltage-Current (V-I) characteristics under forward and reverse biased condition.

Simulation Steps: To construct the PN junction diode 2-D structure, The first step is to construct the diode structure. From Menu, select→File →New Device Drawing , that will initiate the 2-D device drawing window, as shown.

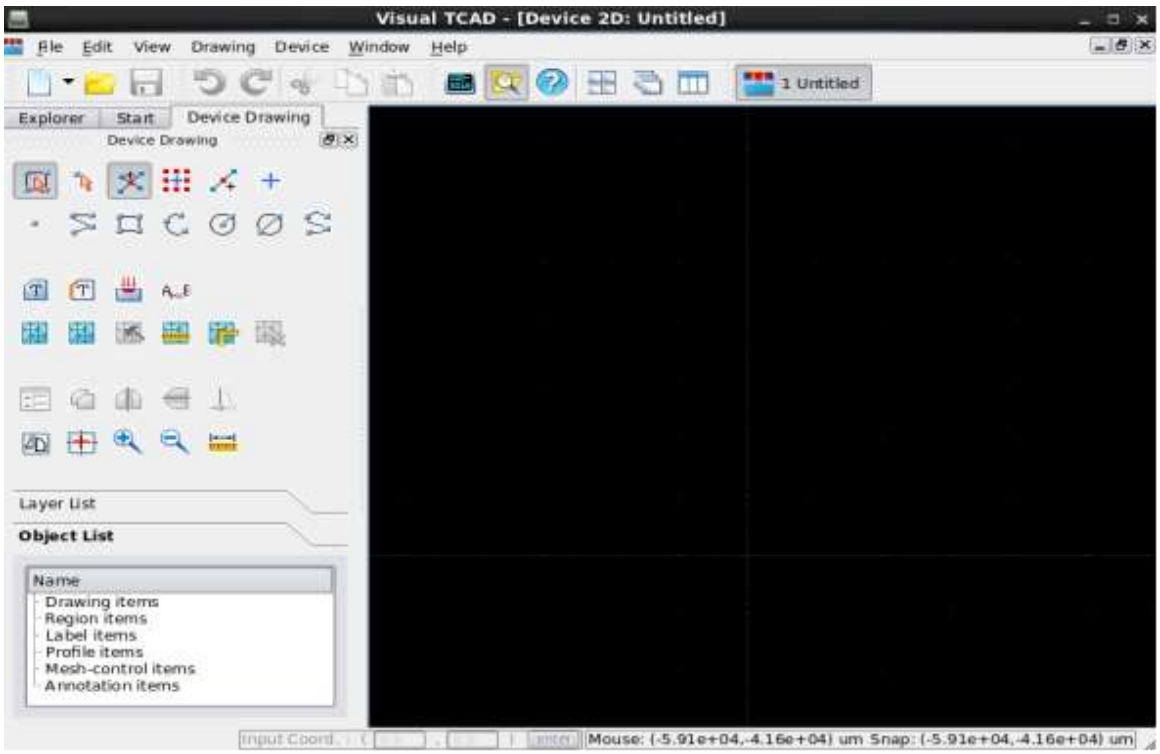

Figure 9: Device design window

Proceed with following steps-

1. A window with black background will open up with default grid spacing width= $0.01\mu m$.
2. The diode structure dimensions are $L = 4.4\mu m\ X\ H = 4\mu m$) with anode block dimensions ($L = 2\mu m\ X\ H = 0.2\mu m$) and cathode block($L = 4\mu m\ X\ H = 0.2\mu m$).
3. With the help of the shapes given on the left top select rectangular shape to design the device.

4. The outline of the device structure is shown in the figure :

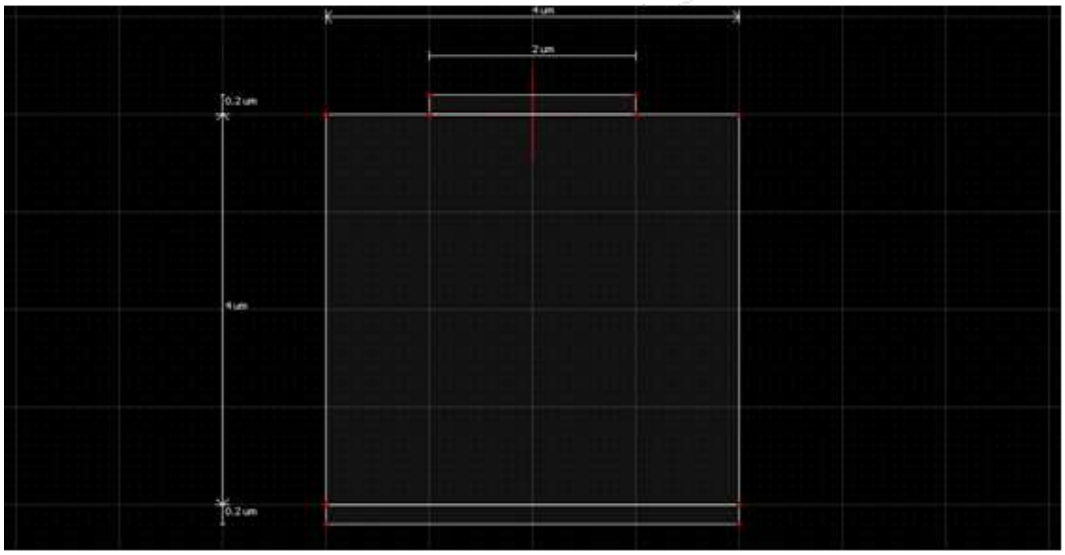

Figure 10: Device Structure

Material selection:

- Every enclosed region in the drawing must be labelled and assigned a material.
- Add the label to substrate region ($4\mu m\ x\ 4\mu m$) of the silicon material with the maximum mesh size $0.1\mu m$.
- Add the label to the anode and cathode blocks of ($2\mu m\ x\ 0.2\mu$m) & ($4\mu m\ x\ 0.2\mu m$) with the aluminum (Al) material and keep the mesh size by default.

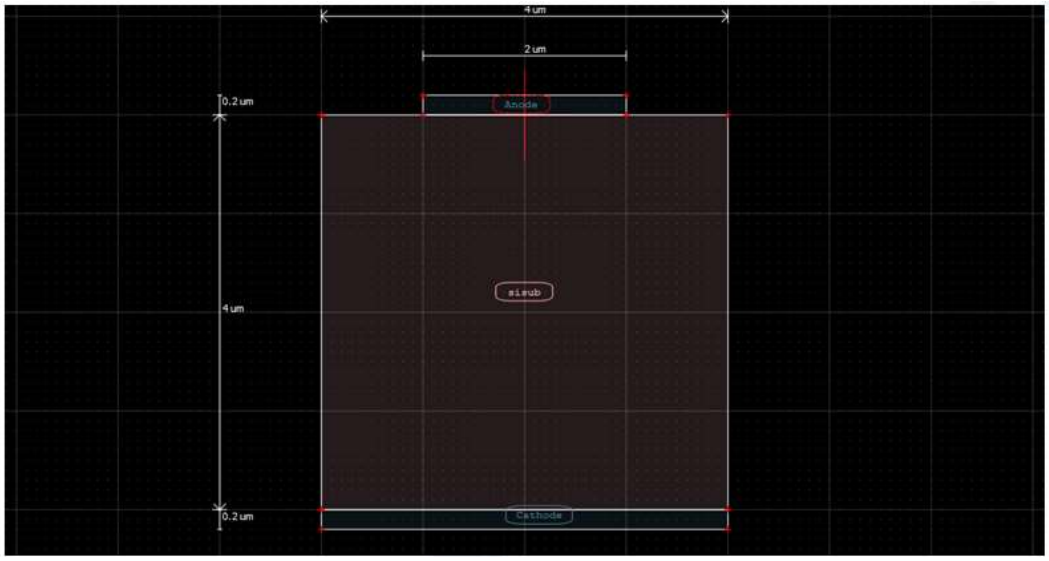

Figure 11: Anode and Cathode Structures

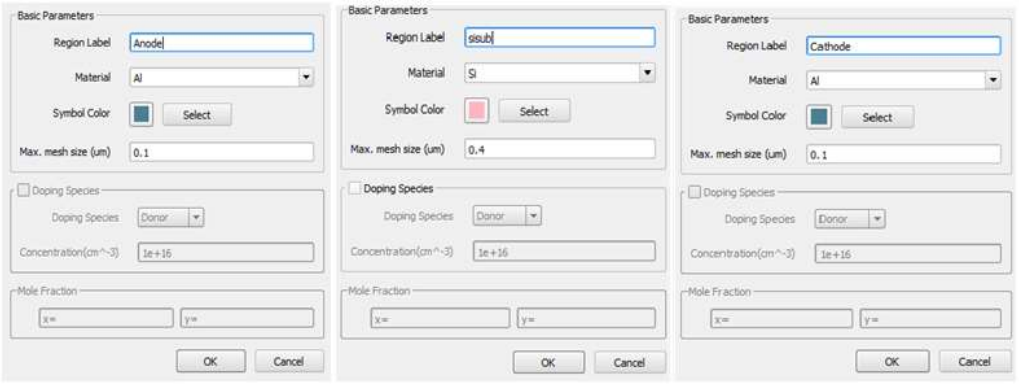

Figure 12: Device Structure: Device, anode and cathode each in sperate windows.

Adding Dopants to the Device Structure:

Doping is essential process in the device design. To create essential doping profile within the device structure, Select menu →add doping Profile →

- Choose doping profile as uniform with **N type / Donor** dopant material having doping concentration of $(\mathbf{1e+16})/\boldsymbol{cm^3}$ for the entire silicon $(4\mu m\ X\ 4\mu m)$ region.
- Choose the doping profile for P- type / Acceptor impurity below the Anode region from top to bottom having dimensions $(2\mu m\ x\ 0.1\mu m)$ along with the doping concentration ($1e+19$) $cm3$ and the Y-characteristics length will be 0.25um with X-Y ratio of 1.

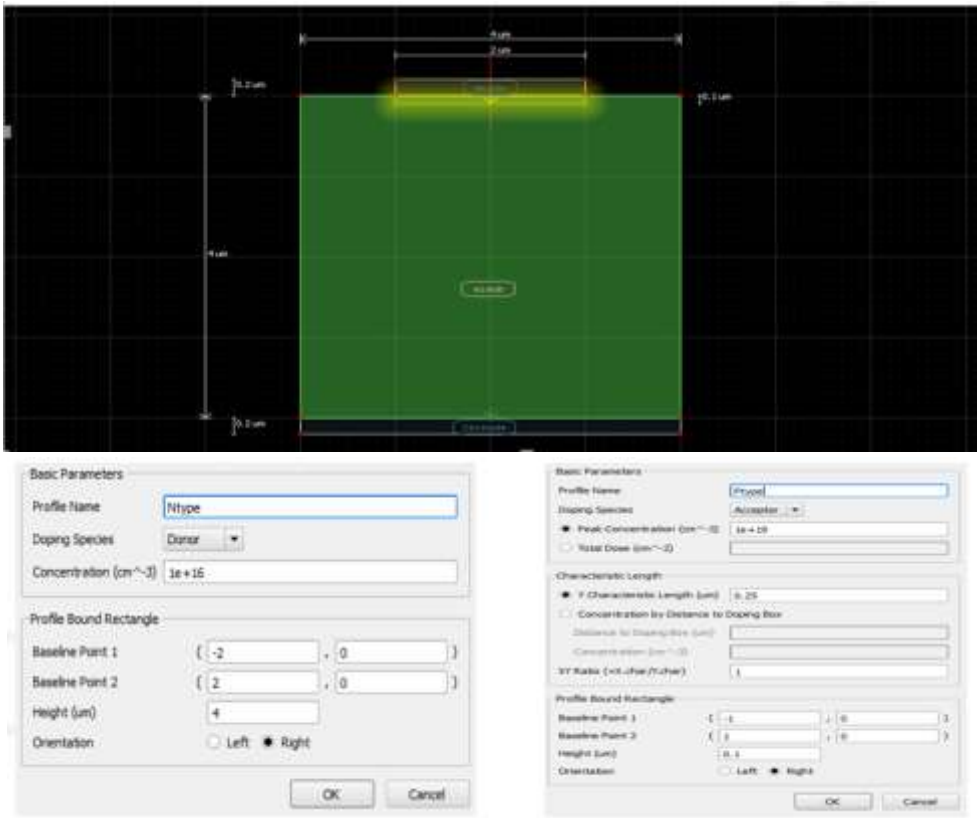

Figure 13: P and N Type doping profiles within a device structure and the dialog boxes used for setting the doping profiles.

Meshing:

The numerical device simulation always relies on a mesh grid that divides the device into many small elements. To set the meshing details, follow the steps as→

Menu → Do Mesh→ meshing refinement can be done using option →Refine Existing Mesh. Meshing details can also be chosen using spring method , the area of covering the junction will be more denser after refining it 2-3 times ,the tool automatically detects the Junction of material and aligns the density of the accordingly.

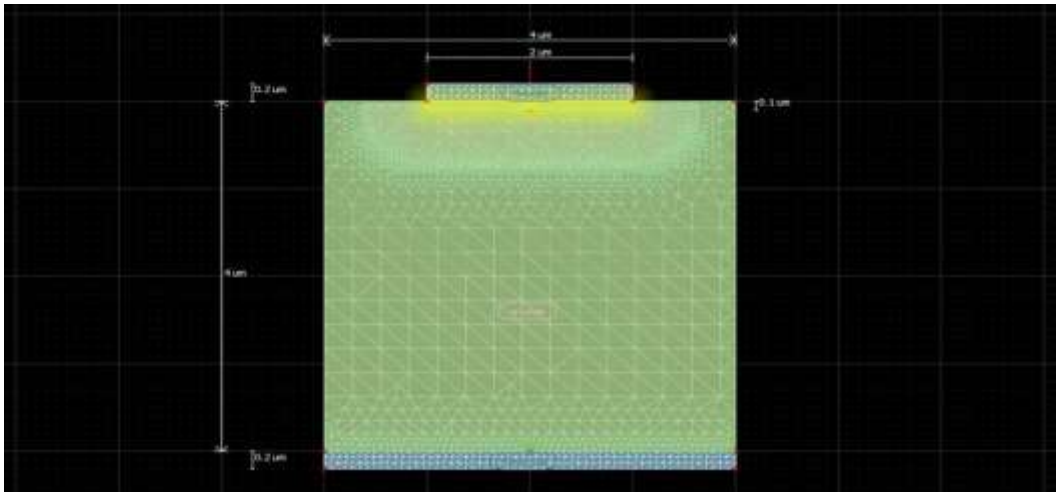

Figure 14: Setting up a Mesh for a Diode Device Structure.

After finalization of mesh settings the file in the **.tif** file format is to be saved using **Device** option in menu bar as →**Save mesh to file.**

Device Simulation:

After saving mesh file to .tif file go to the file option above and open the Device simulation.

- First load the device structure designed in the first stage by clicking→ Load button in the Summary section of the simulation control window. Select the diode.tif file, created. Please note that its takes a few seconds for Visual TCAD and Genius to analyse the .tif file and get loaded.
- The device structure is visible in the Structure Viewer window, with defined device electrodes indicated in the 'Electrodes' section. As in this example, the diode terminals have been named as Anode and the Cathode while creating the device structure.
- OR from the folder below Setup, browse the files to locate and load /open the .tif file. It will take some time or earlier load the structure from (.tif) file along with the contacts or electrode work areas for example in case of diode these area are namely anode and cathode.

Device Biasing:

- Observe the default settings in the in the Simulation Control dock widget, the default Simulation Mode is in Steady state. The other choices are Transient and Circuit-element. There is also the list of regions and boundaries in the device structure.
- Clicking on a region or boundary name results in highlighting the corresponding region or label in the Structure Viewer. The user can setup physical models,

boundary conditions and other solver options from the choice of options available in the dock widget. One can opt for the basic choices very easily however, to study all the choices in detail one needs to go through the Visual TCAD help file.

– Now with the help of **Run** button one can simulate the device by first saving it and then **create a folder** named as results or run or as per user wants to give name to it, after choosing the folder for simulation our simulation will be submitted and will give the results or we can open the file **result.dat** from the folder we have selected to simulate in Examining the I-V Characteristics

Examining the I-V Characteristics:

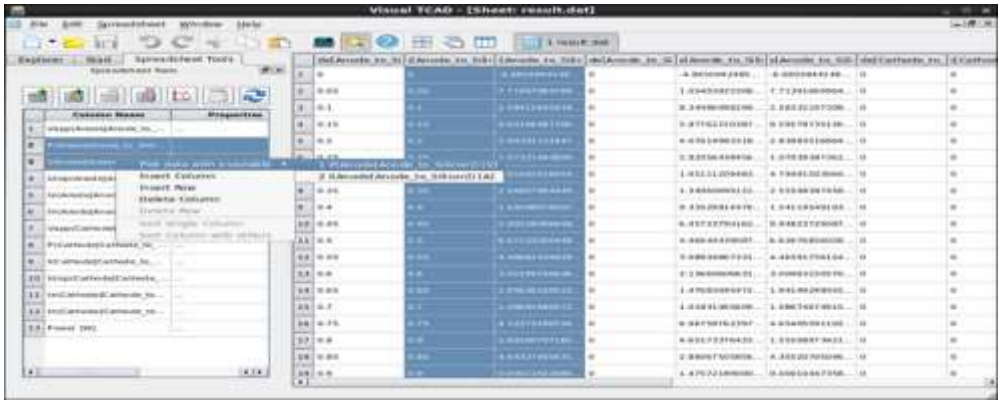

Figure 15 : Tabulation of the results obtained after simulating the device

Plotting theI-V Curve:

or plotting the curve, first select the anode terminal parameters namely $Anode\_Vapp$ and $Anode\_current$ from the respective columns. Similar to the most of the GUI applications, one can select multiple columns by clicking on the column header and holding the Control key. After selecting the columns , right-click to activate the context menu, and select the desired data for plotting the characteristics. The plot of V-I characteristics for the forward biased condition is shown in the figure below.

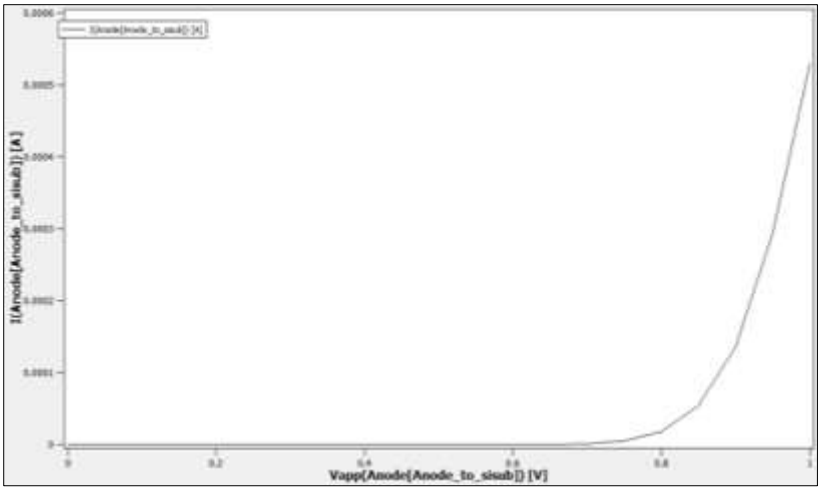

Figure 16: Plot for Forward voltage and current in PN junction diode.

Custom Symbol Generation and Circuit Simulation:

The user has choice to implement the designed device structure assigning a valid symbol to the device. To assign a symbol, one needs to first load **.sim** file and select the circuit element as indicated in the figure. Select diode from the list after scrolling down the device list, assigning the choice of the user defined symbol to the device. This is useful as the doping profile within the device is as per the user specifications and analysing device performance becomes an easy task with use of this symbol in circuit design.

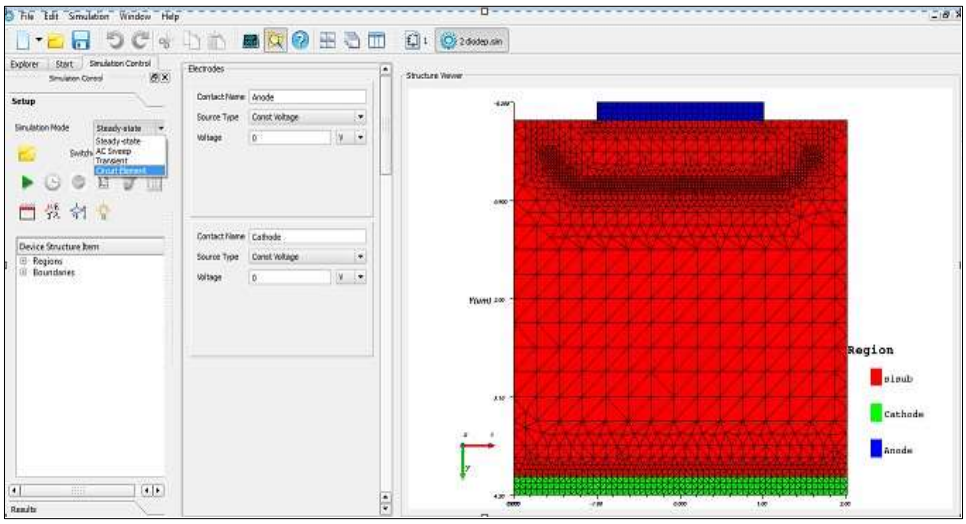

Figure 17: Device Structure and its terminals ready for symbolic representation.

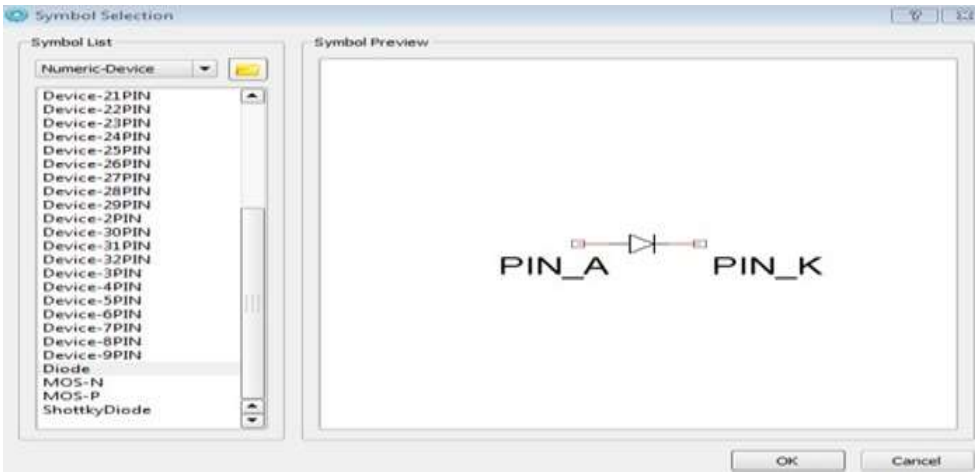

Figure 18: Symbol Assignment

Designing a circuit schematic using Custom Symbol:

– Let us design a half wave rectifier circuit using the customized device structure. To realize the circuit, go to the menu ,File→ New → Circuit Schematic and with the option numerical device[ ]. Since .sim file has been created for the device, the circuit element of diode, we need to create the half wave rectifier circuit using electrical components given namely voltage probe, electrical ground, wire connections , etc using simple drag and drop technique as per the specific circuit

schematic .a Circuit schematic for half wave rectifier circuit designed for performance analysis is shown in the figure below.

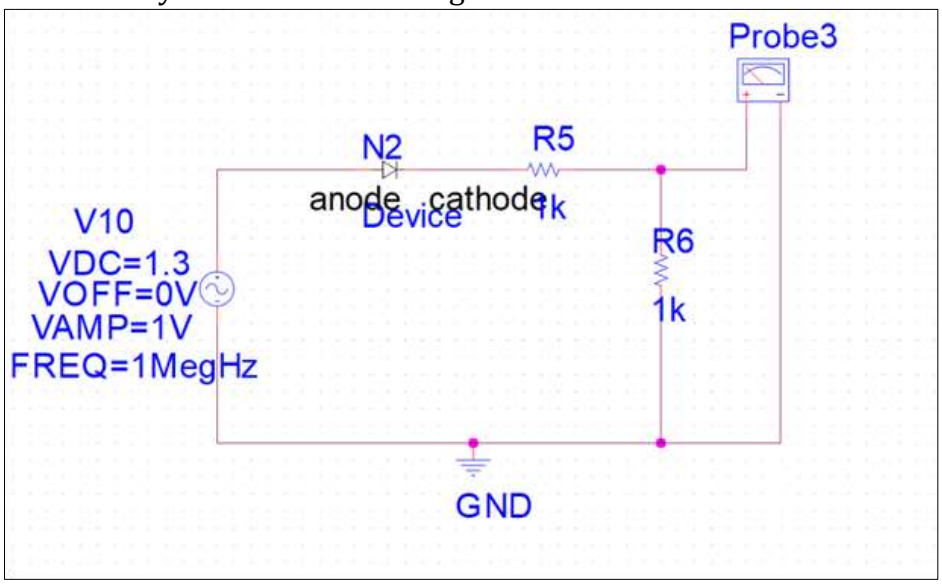

Figure 19:Half Wave Rectifier Circuit Schematic.

– Once a circuit with proper connection sis ready, one can analyse the electrical characteristics running the desired simulation profile. Here, to study the transient characteristics, having X-Axis as time , we need to select transient characteristics and time for which one wishes to run the simulation. The result obtained post simulation has all the nodal voltage and current values tabulated for the circuit schematic . the result data file has extension .dat which is ready for plotting the desired characteristics from the simulation result.

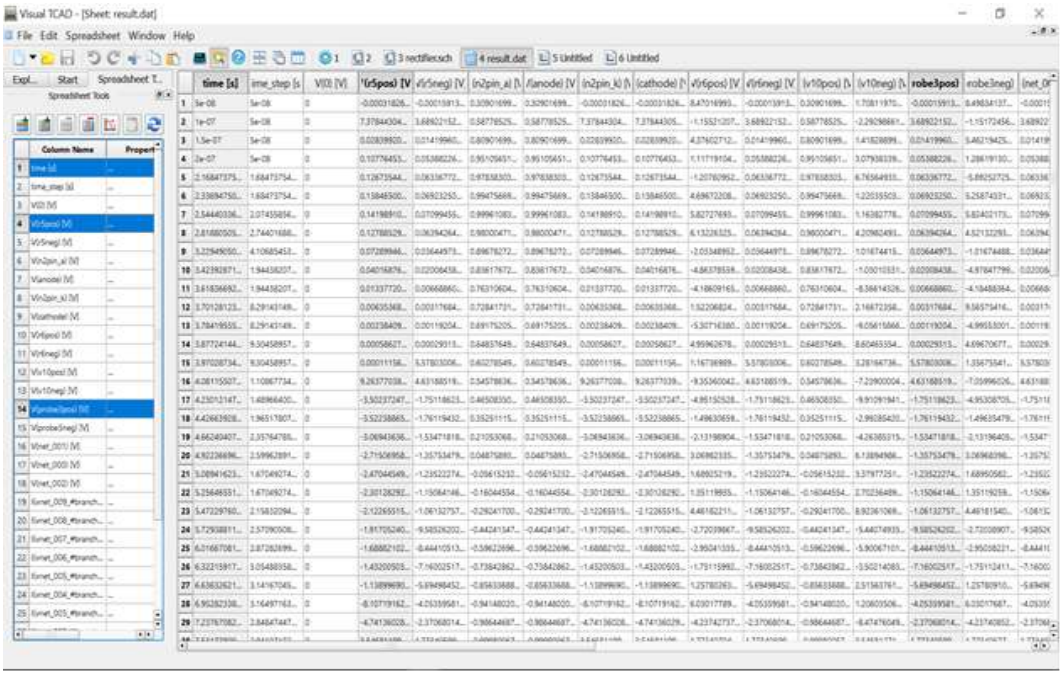

Figure 20 :Tabulation of electrical parameters of the nodes obtained after circuit simulation.

Plot Of Input and Output Waveform:

The plot of input and output signals can be obtained selecting the input voltage and output voltage value columns from the table to obtain a graph of the half wave rectifier as shown in the figure .

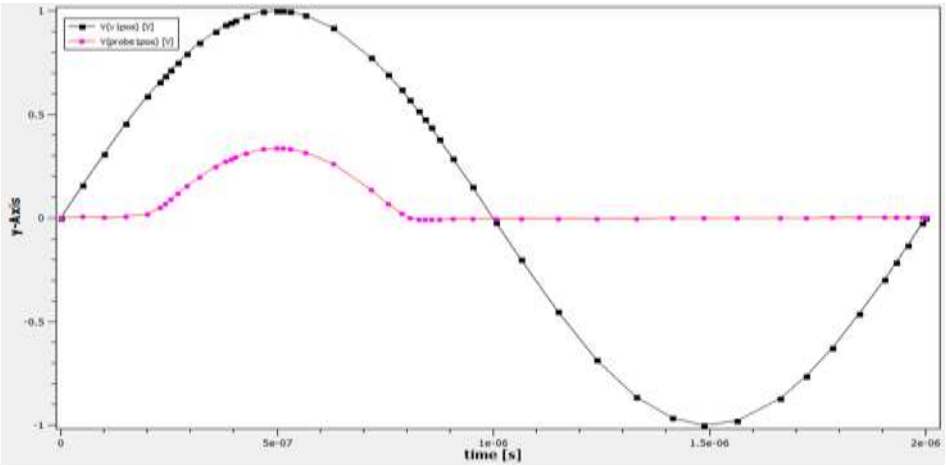

Figure 21: Input and output voltage plotted for the half wave rectifier circuit.

Such circuit analysis is essential for used analysis of user specific device structures. The analysis of the device for different dopant profiles aids enhancing PN junction conceptual knowledge and extending it further towards new device structures.

Chapter 3: NMOS Device Structure

Objective:

1. Design NMOS device structure using Cogenda Visual TCAD
2. Analyse its performance using device simulator tool.
3. Assign a user defined symbol and use it as a circuit element to study its electrical characteristics.

Pre-requisites: Fundamental knowledge of N-Channel Metal Oxide Semiconductor device structure. Depletion and enhancement NMOS device structures. Its internal capacitances Gate-to-Drain (C_{gd}), Gate -to-source, C_{gs}), Drain to SourceC_{ds}), , Body or substrate to drain and gate$C_{bd}.$, C_{bs}), N-channel enhancement and depletion MOSFET input and output characteristics and definition of parameters such as input impedance(R_{in}) , output impedance (R_{out}), threshold voltage(V_{TH}), Transconductance (g_m)subthreshold leakage current or subthreshold slope (SS) etc.

Device Design: N-channel Depletion MOSFET:

1. Open the Visual TCAD tool by clicking the icon in the start menu for windows user and for Linux(Ubuntu or rhel) open the terminal [ctrl+alt+t]
2. Go to the file menu →new file and choose the Device Drawing as an option. A window with black background will open up with default grid spacing width of $0.01\mu m$
3. To create the device structure lets us define the area for substrate, source, drain, oxide regions as well as metal gate. The defined drain area for source region is ($L = 0.6\mu m\ X\ H = 0.5\mu m$)and for the drain region ($L = 0.03\mu m\ X\ H = 0.1\mu m$) and Substrate area is ($L = 0.6\mu m\ X\ H = 0.5\mu m$) along with Gate ($L = 0.2\mu m\ X\ H = 0.03\mu m$) and oxide (L=0.2$\mu$m X H=0.01$\mu$m).
4. Choosing appropriate shapes for these regions from the shape toolbar such as a rectangular shape for substrate, drain, gate, source oxide regions etc a final device structure is developed. The n-channel MOSFET device is shown in the figure below

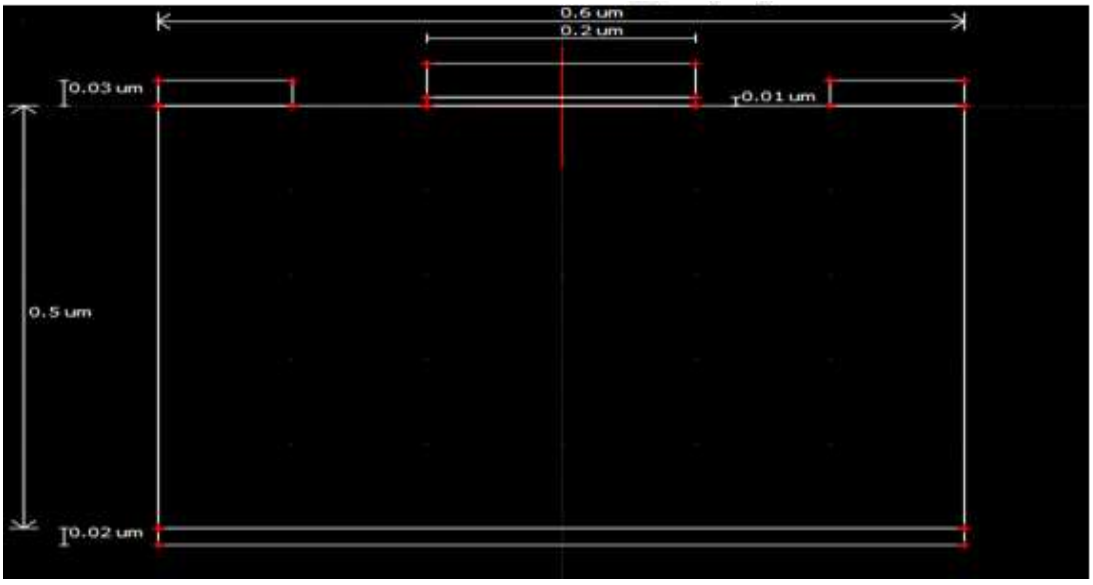

Figure 22: Custom Device Structure :N-Channel MOSFET

5. Add the region label substrate ($0.6\mu m\ x\ 0.5\mu m$) from the silicon material with the mesh size assumed as 1/10th of the block size e.g. as it is of $4\mu m$ block length so max. meshing size will be $0.05\mu m$.
6. Append the other labels for the remaining regions namely-Source($L = 0.1um\ x\ H = 0.03um$), Drain(L=0.1um x H=0.03um), Substrate (0.6um x 0.02um) with the aluminium (Al) region and keep the max mesh size same as given by default as we don't require to calculate on the metal-semiconductor junctions. Another two regions are Gate with material (N Poly Silicon) along with the oxide region below Gate region with material(SiO_2)with mesh dimension 0.05.

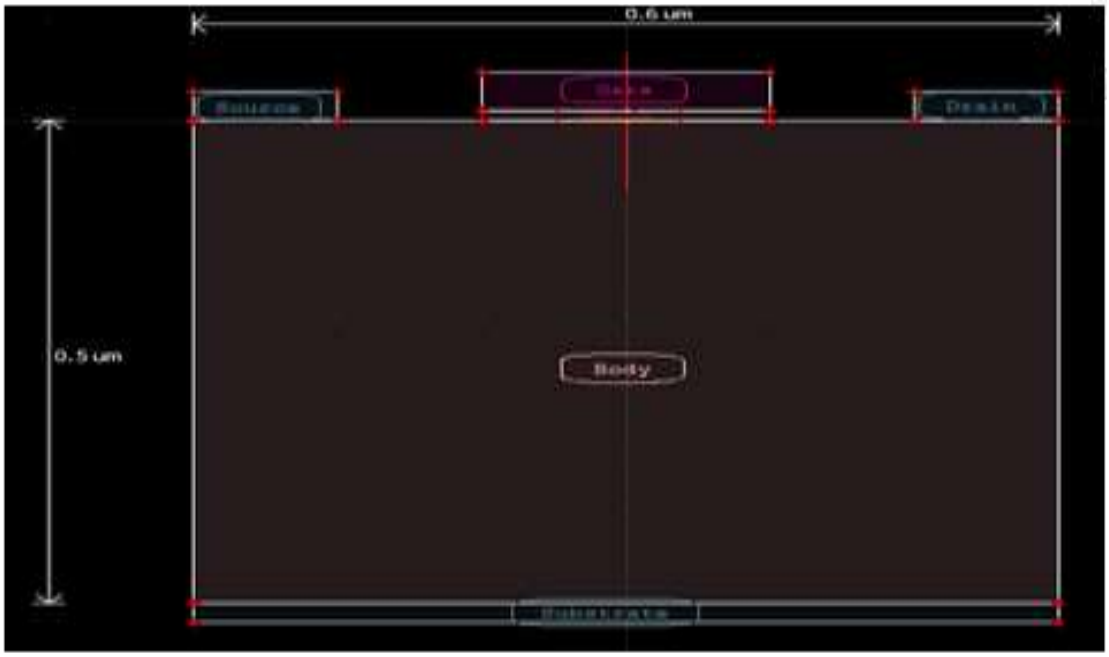

Figure 23: Device Structure with proper labels.

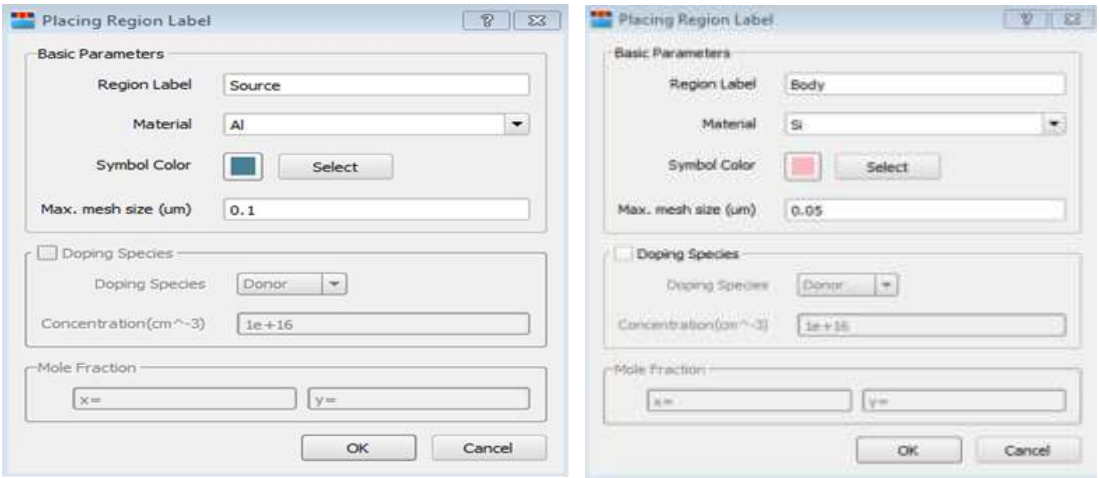

Figure 24: dialog box: Assigning label and setting properties for the source and body of the device

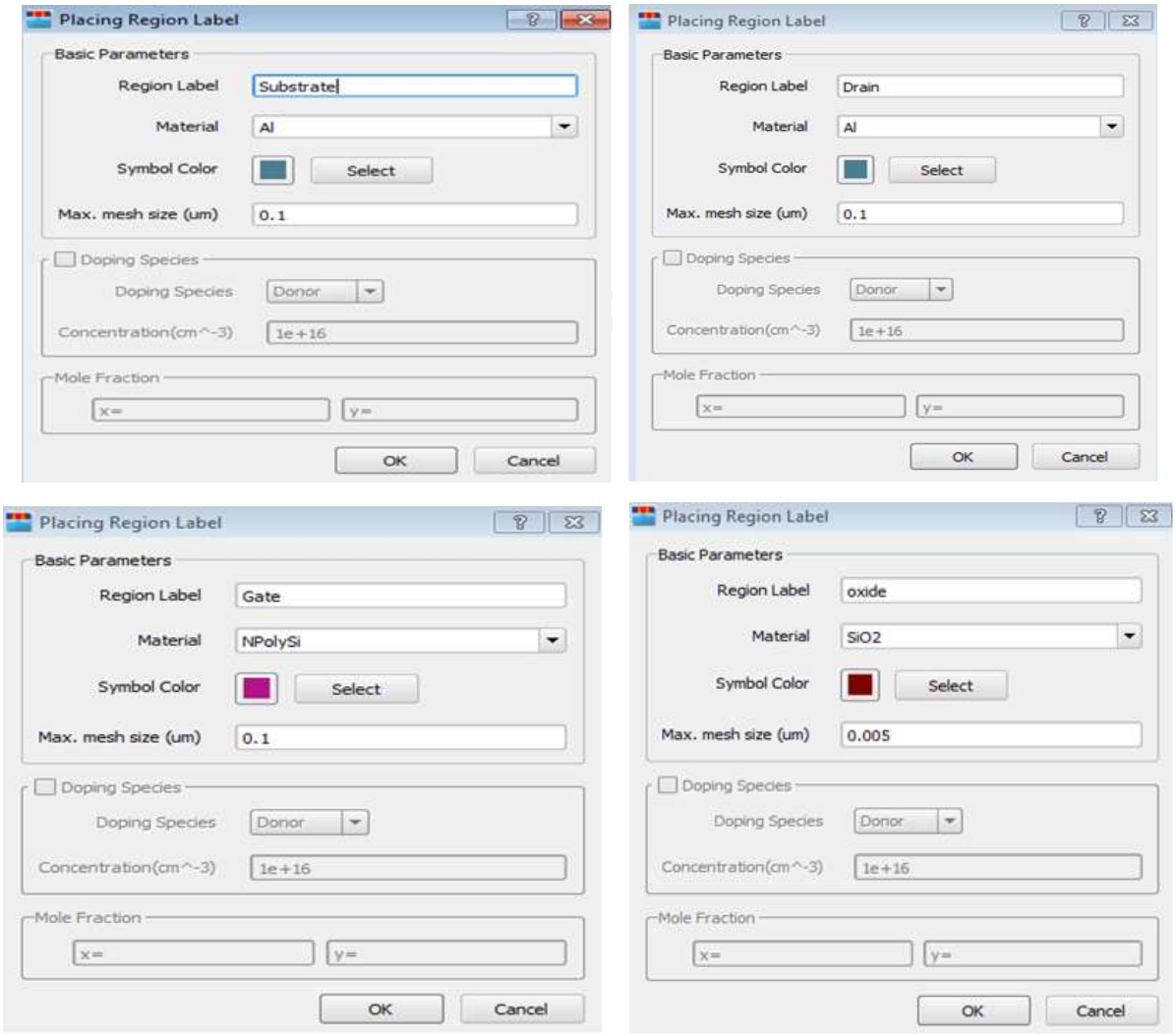

Figure 25: dialog boxes: Setting properties of Substrate ,Drain, Gate and Oxide regions of the device.

7. Using the menu option Add Doping Profile→two regions are formed
   - First doping profile is uniform profile of P type /Acceptor with the doping concentration of $(1e+16)/cm^3$ across the entire region from top to bottom uniformly or the area having dimension $(0.5\mu m\ X\ 0.6\mu m)$ above the Body region from top to bottom is doped with P-type impurity.

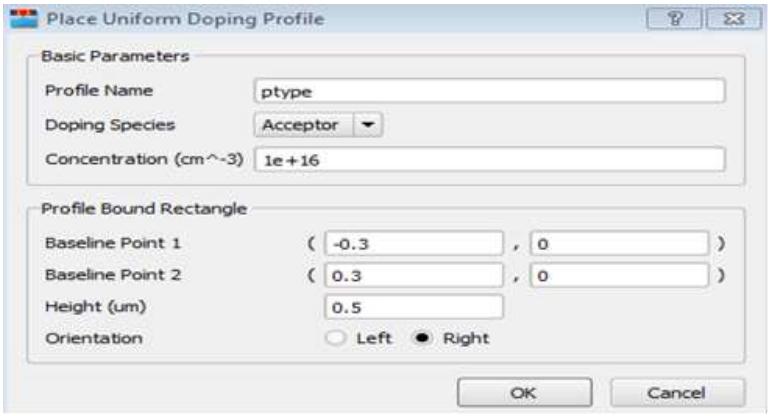

Figure 26: Setting uniform Doping profile

– Second, a lightly doped region (LDD) is formed having doping profile of N type / Donor that is located below the Oxide layer and from top to bottom towards both extreme left to the Source as well as extreme right to the Drain with the dimensions $(0.01\mu m\ X\ 0.2\mu m)$ along with the doping conc. $(1e+18)\ /cm^3$ and the Y-characteristics length will be $0.005\mu m$ with X-Y ratio of 1.

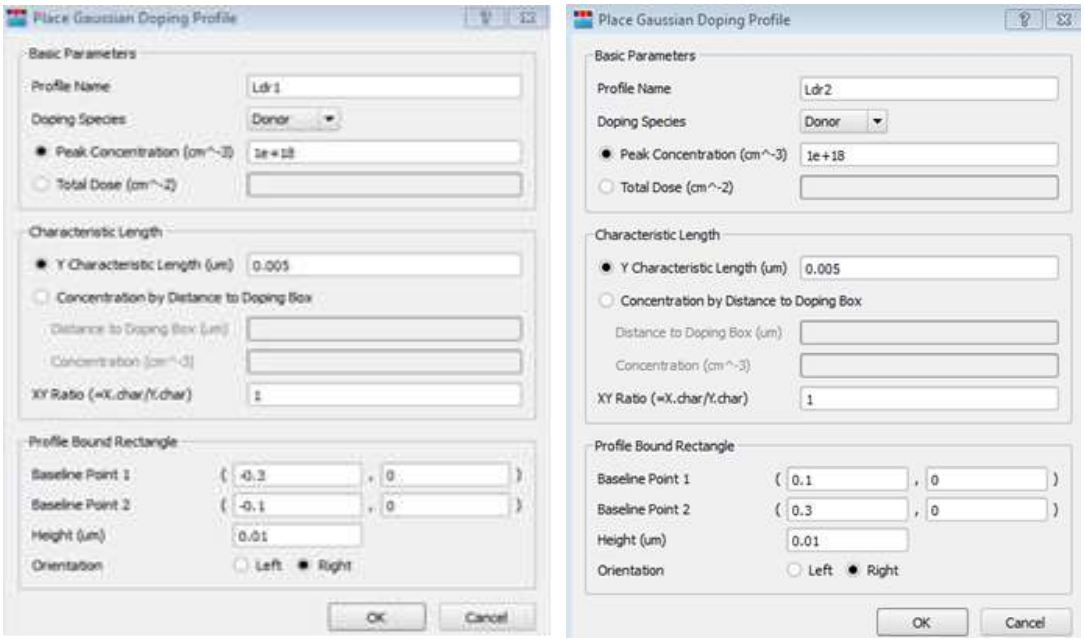

Figure 27: dialog Boxes used for setting dopant profiles for LDD

– Deep junction doping profile is also of N type / Donor starts below the mid of the Source and Drain with Oxide as common, from top to bottom towards both extreme left to the Source as well as extreme right to the Drain with the dimensions $(0.15\mu m\ X\ 0.02\mu m)$ along with the doping conc. $(1e+20)\ /\ cm^3$ and the Y- characteristics length will be 0.025μm with X-Y ratio of 0.8.

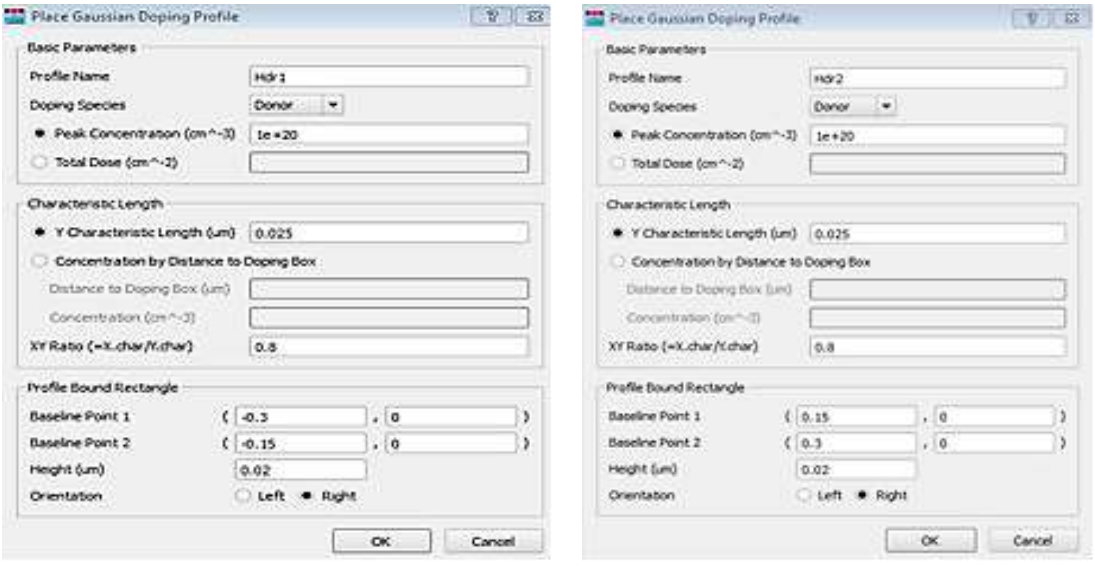

Figure 28: Dialog box used for setting dopant profiles of the deep junctions

– Fourth doping profile is of P type /Acceptor for the threshold voltage doping implant with the doping concentration $(1e+18)/cm^3$ along with the characteristics length of $0.01\mu m$ and X-Y ratio is 1.

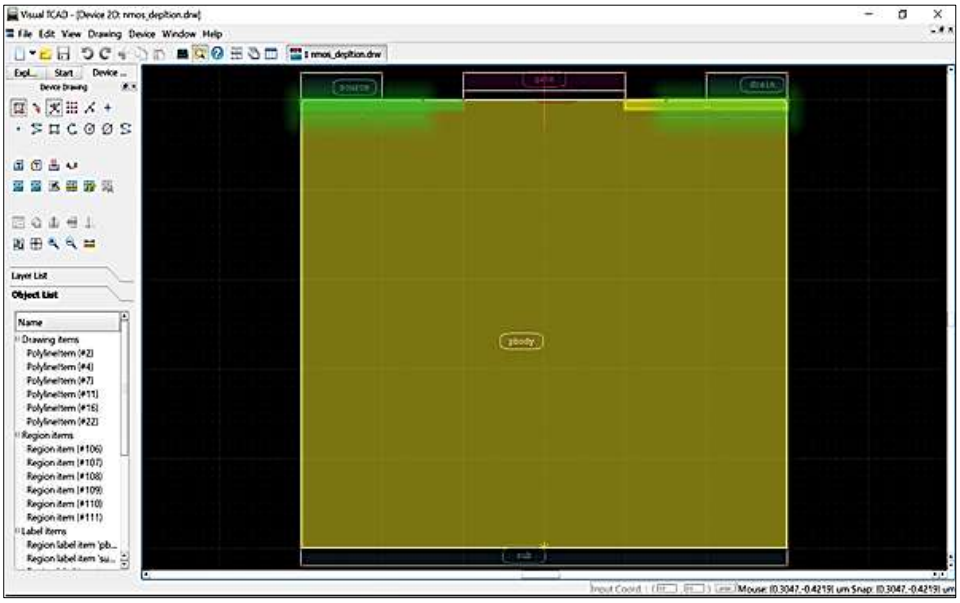

Figure 29: Final Device structure view after setting all the dopant profiles.

– Now the mesh settings are to be finalized. To proceed, choose the option → Do Mesh. The mesh refinement can be done using option→Refine Existing Mesh . The mesh can also be set using spring method. The method demands refinement to be done at least 2-3 times so that the area of junction can be made denser to pick up all the characteristics accurately during simulation. The spring method does the job automatically identifying the regions to set the density of the mesh according to the regions specified.

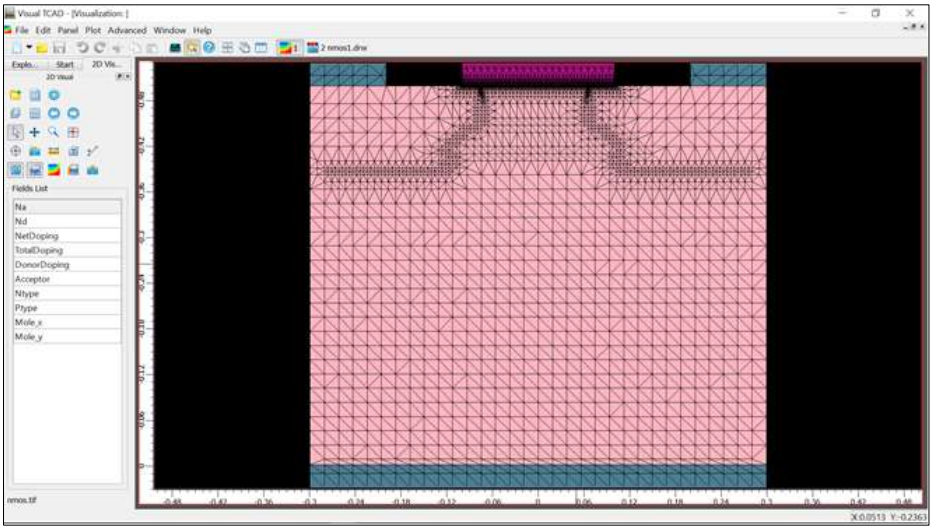

Figure 30: NMOS Device view after setting the mesh

– All the mesh settings are saved using option from the menu, Device→'Save Mesh to File'. Remember the file has extension (.tiff).(It is an image file format)

Device simulation:

Once the device structure is created, its time to apply bias voltages and perform simulation to study the characteristics of the device.

– After the mesh settings are saved to (.tif) file, go to the file option and open the →**Device simulation**. The .tiff file having device structure with meshing can also be opened browsing the location where it has been saved. Note that the loading of this image file format takes some time and once it is loaded , the device structure is visible with all the electrical contacts or electrodes namely Gate, Source, Drain and substrate. The dialog box used to set the biasing voltages prior to the simulation is shown here.

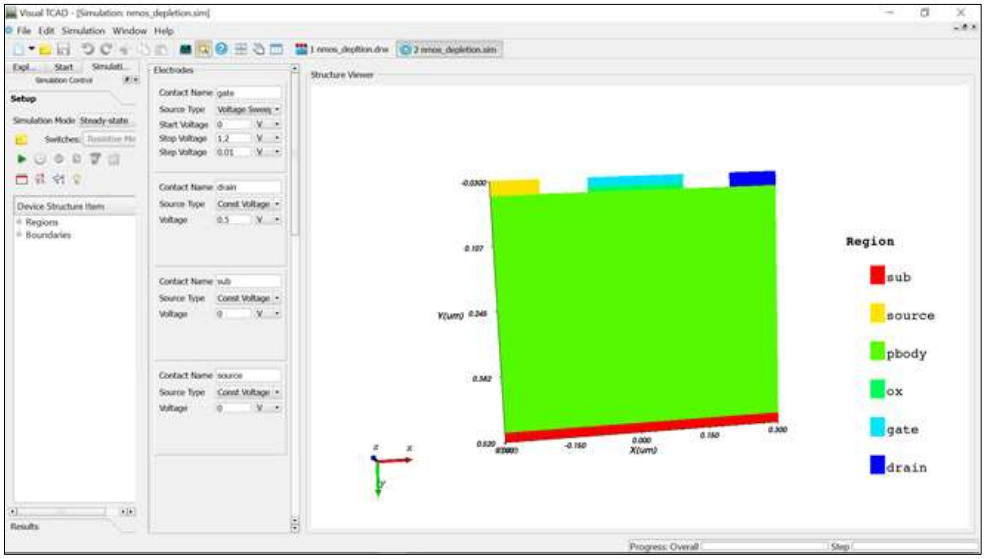

Figure 31: Device Simulation → Dialog box to set the biasing voltages prior to the simulation.

Biasing prior to the simulation:

– Provide some Voltage Sweep biasing to the GATE (1.2 V with step size 0.05) and Drain with Constant voltage and save with some name. Then ,with the help of option→**Run** button the device can be simulated to create a file having extension (.sim).
– Create a folder named as 'RESULTS' (you may assign any name). Run the simulation as per the user specifications sweeping the voltages with appropriate step size.
– The final outcome of these simulations are saved in a file having extension .dat.
– The (.dat) file having simulation data collected from all the nodes is made available to the user in a tabulated manner.

Plotting the Characteristics:

– As per the user requirements the columns from the tabulated data can be selected and plotting of data can be done choosing X and Y axis parameters. Here, for plotting transfer characteristics of the N-channel depletion MOSFET

, We are going to select drain current and gate voltage .i.e. I(Drain) and app(GATE).

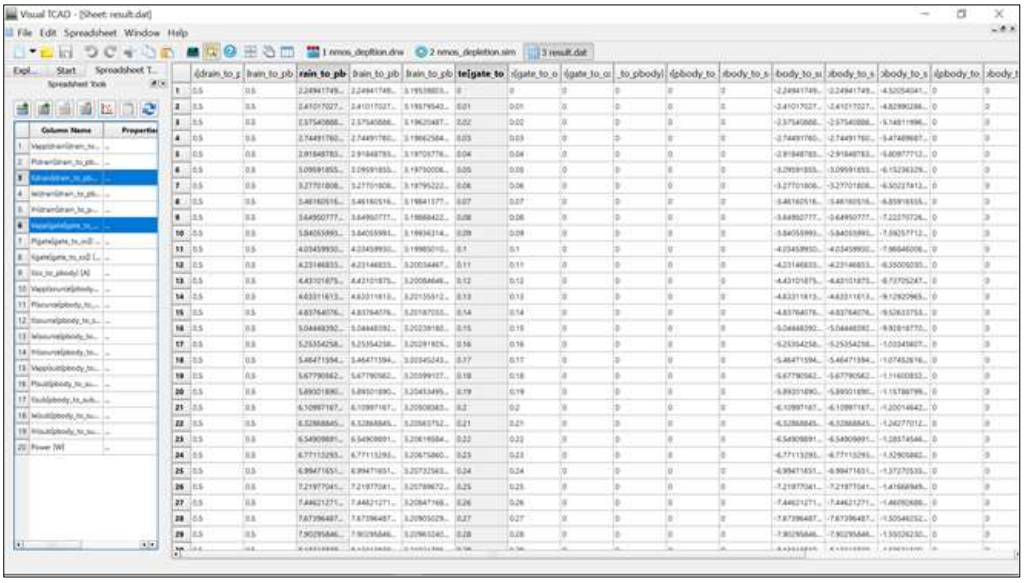

Figure 32: Simulation result:File with .dat extension having electrical parameters collected from the device nodes.

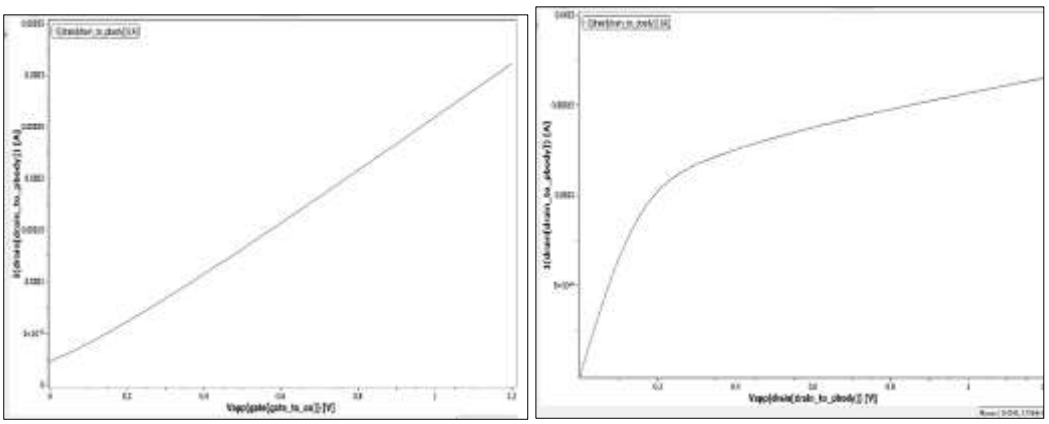

Figure 33: Plot of Gate voltage Vs Drain current and Drain voltage Vs Drain Current for the N-channel depletion-MOSFET.

Enhancement Type N-Channel MOSFET

Procedure to design enhancement type N-MOSFET:

There are two ways the enhancement MOSFET characteristics can be studied using depletion MOSFET.

1. By adding implanted channel (Threshold implant) below the gate terminal in the device structure
2. As we know applying negative gate voltage to the N-type depletion MOSFET , it behaves as enhancement type MOSFET.

In first case, we introduce additional dopant profile (N^+)below the Gate terminal during the device design. The structure of the device can be viewed as shown in the figure.

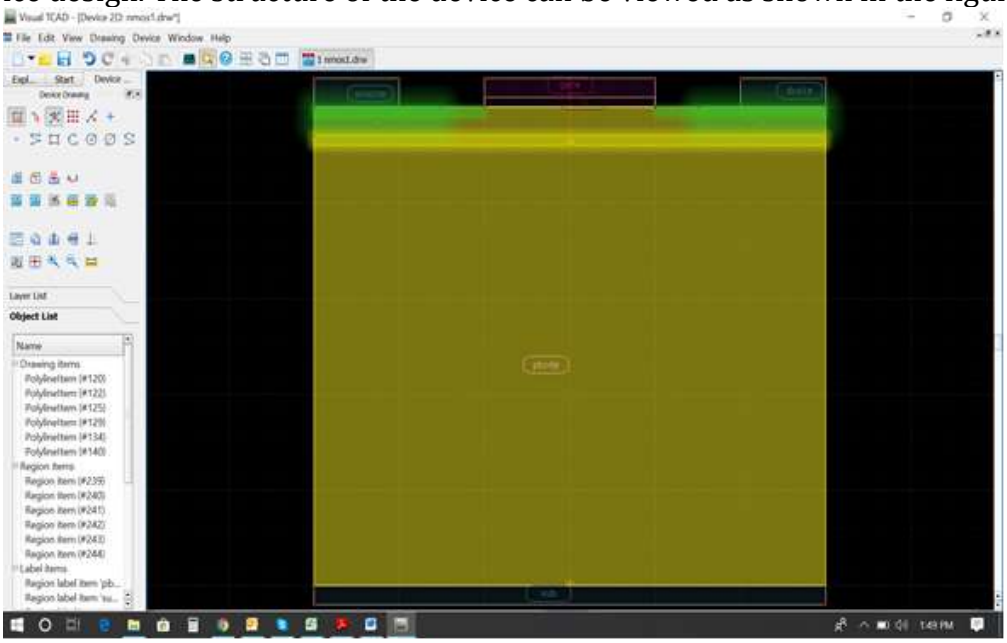

Figure 34:Device structure view after channel implant below the gate terminal.

Once the channel is implanted, meshing is done using option →Do mesh. The mesh is refined 2-3 times using option →Refine Existing Mesh. The mesh settings can also be done using spring method which results into creation of an image file of the device having extension(.tiff). The density of the mesh will be automatically adjusted after 2-3 refinements to pick up electrical parameters during simulation according to the regions defined in the device structure. The mesh file is saves using option→ **Save mesh to file.**

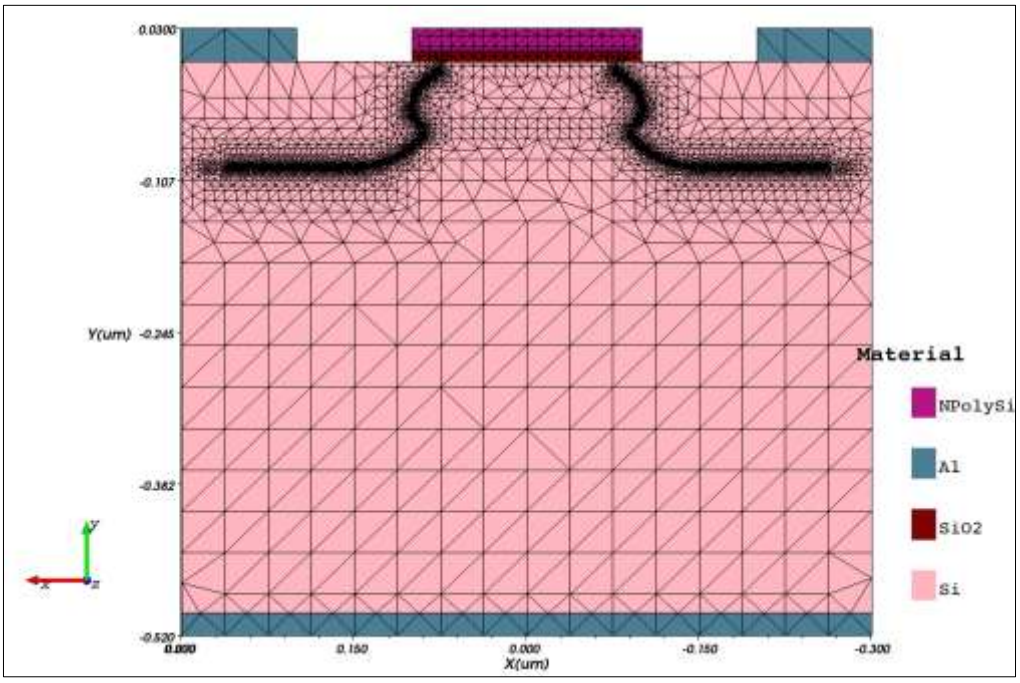

Figure 35: Device structure after setting the mesh.

Device Simulation:

Once the mesh file (.tiff) is saves go to the option→ File→ Device Simulation.
The other option for simulation is to open the (.tiff) file directly browsing its location from the folder. Please note that loading of this file takes some time . Upon getting loaded, the device structure can be viewed along with all the electrical contacts defined in the device structure namely GATE, SOURCE, DRAIN, and SUBSTRATE.

Applying Bias Voltages:

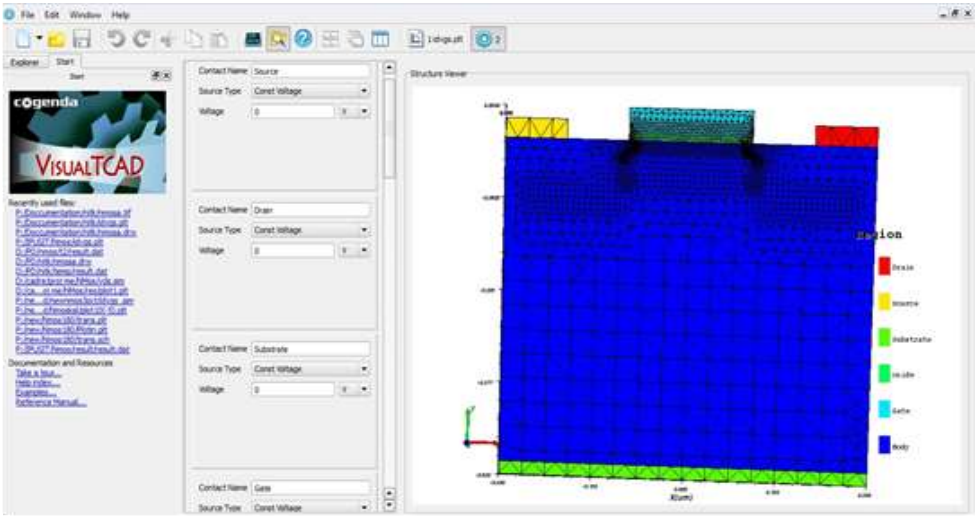

Figure 36: Device structure view from the dialog box after →Device simulation option.

– Prior to the simulation, a device needs to be applied a biasing voltage. Here we apply a Voltage Sweep biasing to the GATE terminal (2 V with step size 0.05 V) and Constant voltage to the Drain terminal. The setting is saved. Then choose → RUN button to run the simulation. A file having extension(.sim) is created. Also the data obtained as a result of simulation is saved in the (.dat) file. The destination of these files can be set by the used or it gets saved in the default folder.

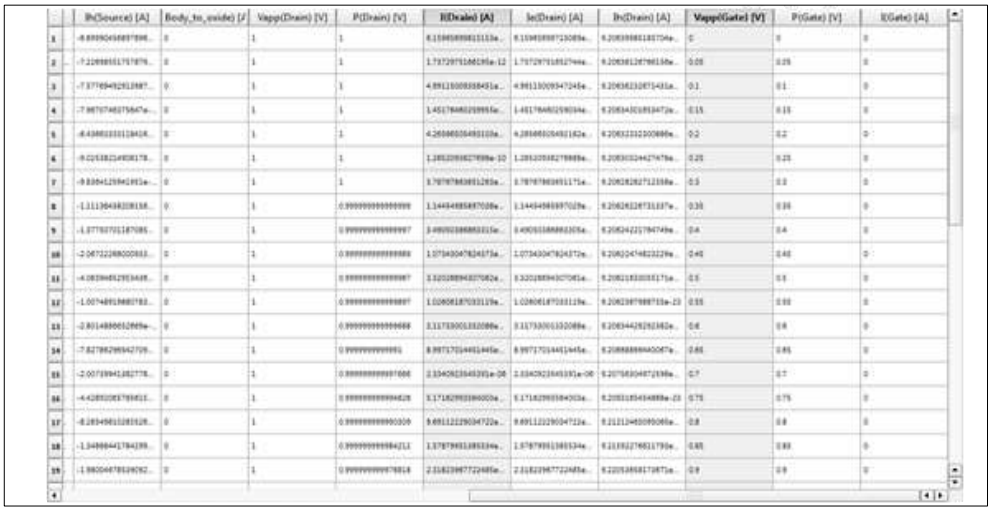

Figure 37: Post simulation data obtained in the from of (.dat) file

Plotting the Characteristics:

In order to plot the transfer characteristics we select gate voltage and drain current columns from the tabulated data and setting X and Y Axes data to be studied from the plot.

To obtain the drain characteristics we plot the characteristics between drain current and drain voltage. Both tese plots are shown in the figure below.

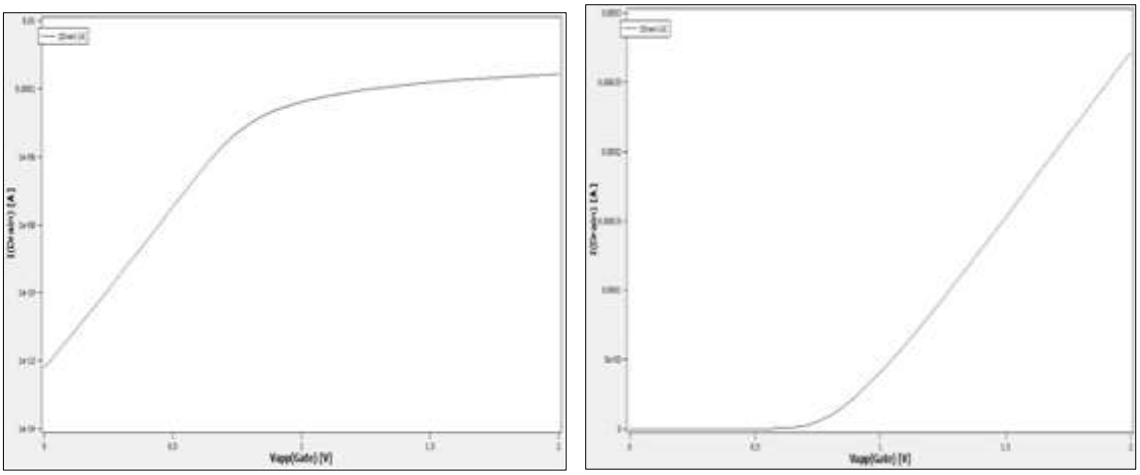

Figure 38: Transfer characteristics on regular and logarithmic scale

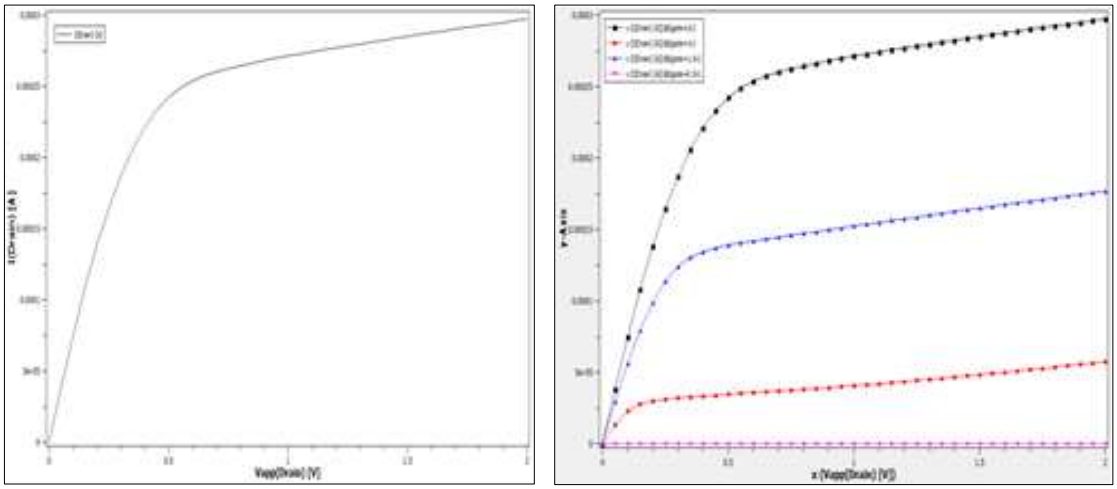

Figure 39: Drain Characteristics ($(V_{drain}\ Vs\ I_{drain})$ keeping V_{gate} as constant.

Assigning user defined symbol to the device structure:

Once the device is ready, it can be assigned a symbol and an electrical circuit can be realized for studying the device behaviour in detail. This technique is known as mixed mode simulation.

- To assign a symbol, load the device simulation file having file extension (.sim) by selection→Device Simulation option from the menu. Then select the **Circuit element** in **Simulation Mode** option as shown

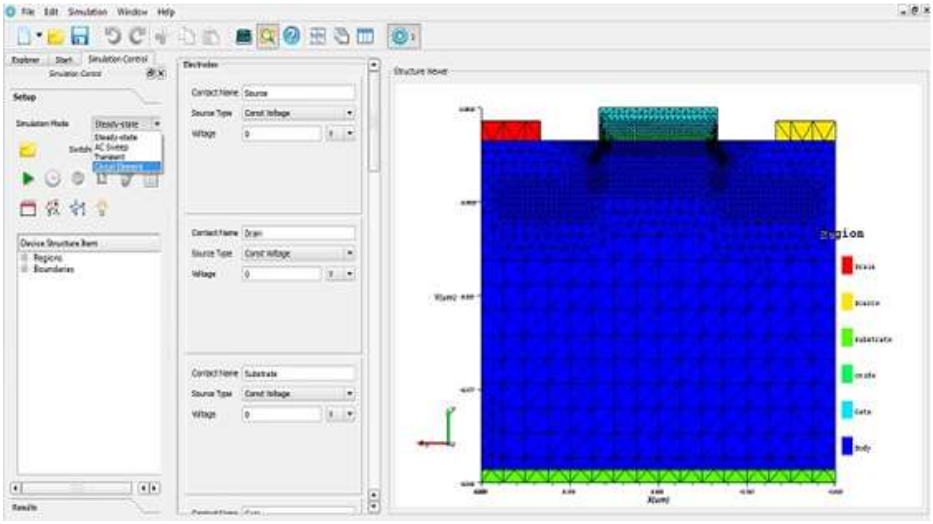

Figure 40: Device structure view after selecting option →Device Simulation before assigning symbol

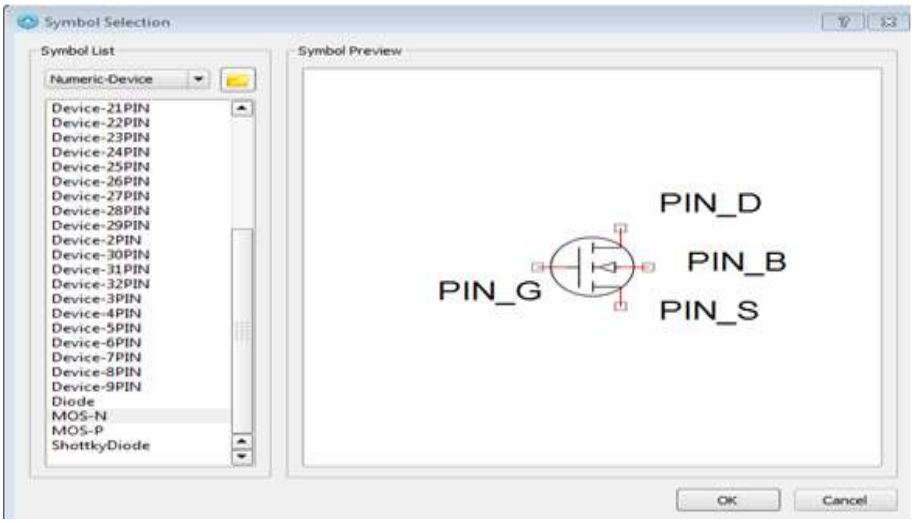

Figure 41: Dialog box after →Device Simulation → Circuit element in Simulation Mode

Now go to the file > Circuit Schematic and load the .**sim** file and from the option Numerical device and make a mixed mode circuit by choosing the 180 nm technology.

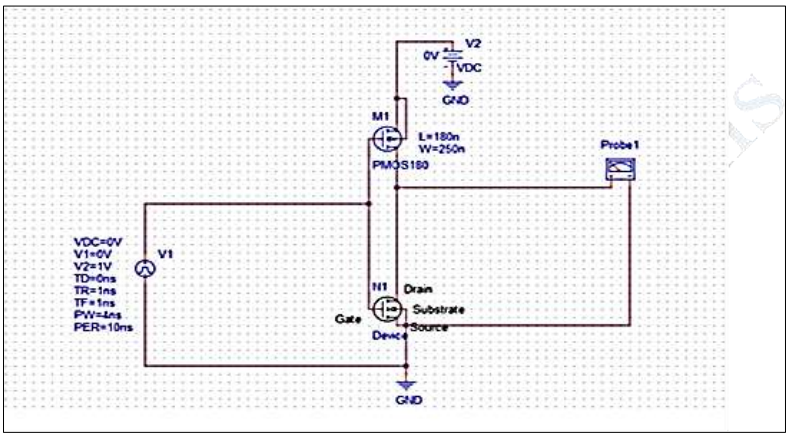

Figure 42:Circuit Schematic selecting PMOS load from the library and custom NMOS Device.

For simulating the user defined NMOS we choose a load device as a P-MOSFET from the library and realize the proper connections as per the circuit schematic shown in the figure. The circuit elements are placed by simple drag and drop technique. The voltage source , probe and connecting wires are selected from the components list available in the dialog box.

The technique is termed as **mixed mode simulation** since we have used user defined device (NMOS)with a load device from the library to realize the circuit schematic.

To verify the device performance, we have placed AC voltage source that provides pulse waveform at the input. The parameters for the V_{pulse} are T_D-Delay time after which you wish to initiate the pulse waveform, T_R- Rise time of the pulse, T_F-Fall time of the pulse, P_W-Pulse width, PER −Pulse repetition rate. Please set these values carefully to study the behaviour of the NMOS device as a switch.

This is a transient mode simulation. The simulation run time is carefully selected to obtain at least two complete pulse waveforms at the output.

A plot of input and output waveform plotted from the result of simulation can be seen in the figure below.

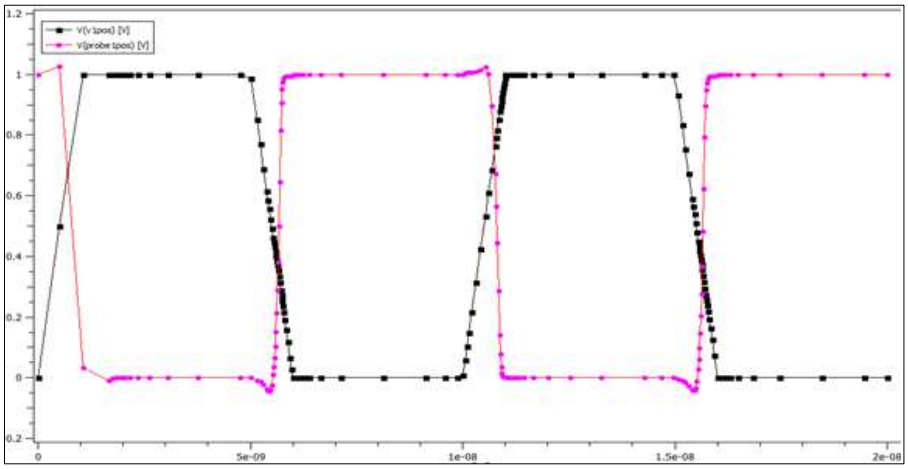

Figure 43: input and Output waveform of the NMOS inverter with active load through mixed mode simulation.

Assignment Task:

The participants are expected to carry out similar task to design a PMOS Device structure and simulate the same circuit schematic through mixed mode simulation technique by selecting user defined PMOS and library NMOS device to obtain similar result indicating input and output waveforms.

Hint→ It is expected to reverse the dopant profiles in the device i.e. instead of N type dopant , you will use P-type dopant while designing the device structure.