HTARGH MOHAN SASON Overflow detection 20) of ("covery ento sign - bit") = (any-out from sign - bit) -> 0 F To check whether there is an overflow or not, we need to check the following cases: 1.) adding 2 positive #5 -> Sum y negative # 2.) adding 2 negative #5 -> Sum y pasitive # Example for 1.) 4+5 > 0100

Here we get a -ve # because most let bit is =.

This occurred because 4 but #13 represent from (-8+07) and 9 is a 5 bit # 1001 when taken Is two's complement, we get 1001=>0110>0110 0111 > which 47, our vflow 2.) -8+(-1)=-9 1000 0 111 is (+7), they resulting in a toe #, DOTTI /44 causing an overflow. when two unsigned numbers are added,
overflow occurs if there is any carry out on
the soft most hit the left most bit. 8+8= 1000 Dood causing an unsigned of

40] Amdahil's law: This law shows how much laterice can be taken out of a performance task by introducing parallel computing. In other words, it is a formula used to find The maximum improvement possible by just improving a particular part of the system. Speedup. It udefined as the ratio of performance for the entire task using the enhancement and performance for the entire task without using enhancement. Speedup = Pel Pw where Pe is the performance for entire task using the enhancement when possible Puristice performance for entire task without using enhancement, Ewis the execution time for entire task without enhancement and Ee is the execution time for entire task using the enhancement when possible. Speedup = (1- fraction manced) + (fraction manced)

2 = (1- 0.70)+0.30

(1- 0.70)+0.30 2 = (1-0.70)+0.30 speedup enhanced