HARSH MOHAN SASON

1.]

(a) 6ns + 4ns + 5ns + 3ns = 18ns

(b) 6ns + 4ns + 5ns + 6ns + 3ns = 24ns

(c) 6ns + 4ns + 5ns + 6ns + 3ns = 24ns

(d) 6ns + 4ns + 5ns + 3ns + 3ns = 21ns

(e) The system clock cycle time will be 24ns because the the slowest instruction determines the clock cycle time of a single-cycled CPU; in this case the lw instruction.

(f) 6ns + 3ns = 9ns. Jump instructions take a portion of an absolute address. They concatenate the result with the upper 4 bits of PC + 4. Datapath is: fetch instr (6ns) → shift left 2

↳ PC → add (3ns)

(2.)

a.) Clock cycle time of Multi cycled implementation is the sum of all the component times ⇒ 6ns + 4ns + 5ns = 15ns

b.) Series of component times for add: 6ns + 4ns + 5ns + 4ns = 19ns

Series of component times for lw: 6ns + 4ns + 5ns + 6ns + 4ns = 25ns

Series of component times for sw = 6ns + 4ns + 5ns + 6ns = 21ns

Series of component times for beq = 6ns + 4ns + 5ns = 15ns

Series of component times for j (jump): 6ns + 4ns = 10ns

Speed up values = $\frac{\text{Multicycle}}{\text{single cycle}}$

add: $\frac{19}{18} = 1.05$

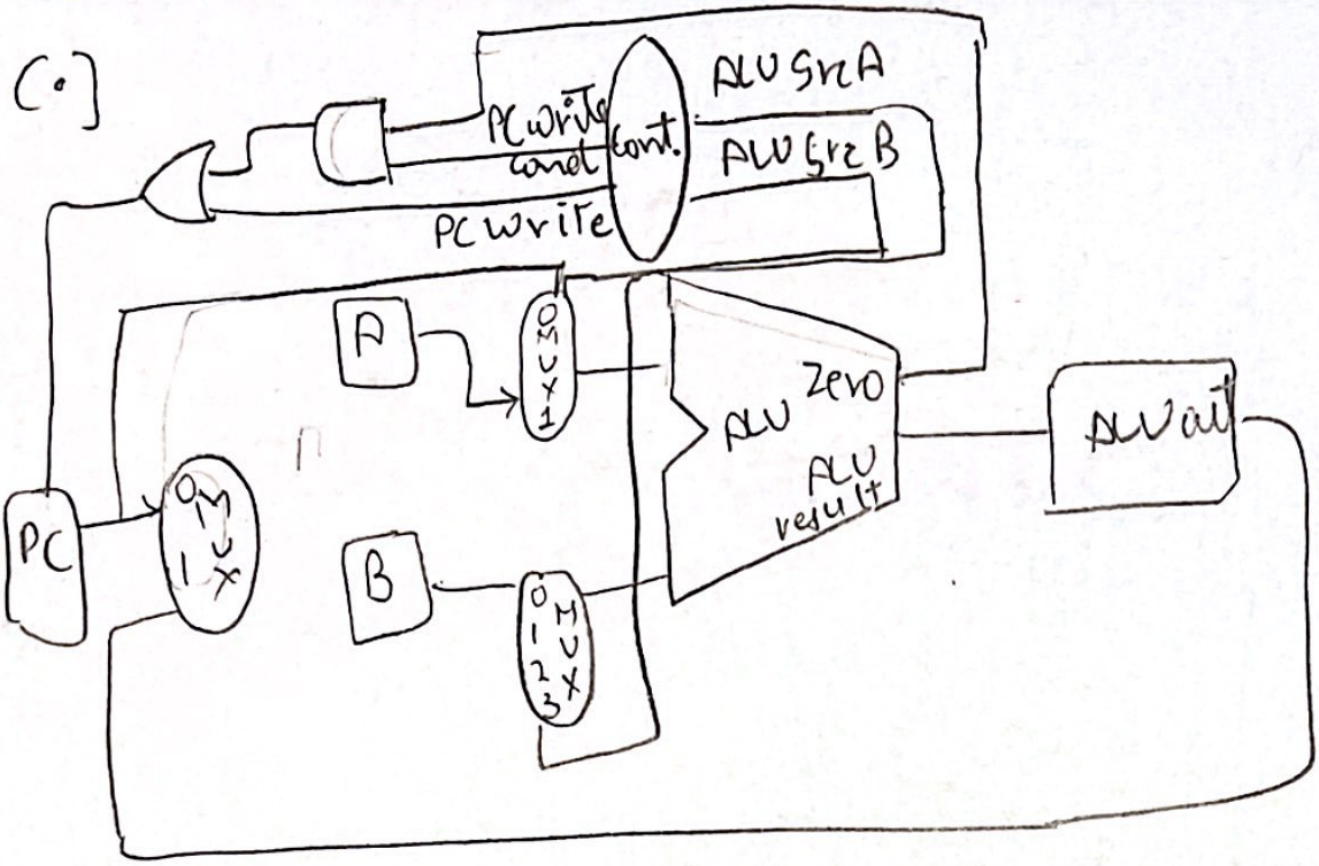
lw: $\frac{25}{24} = 1.04$

sw: $\frac{21}{24} = 0.875$

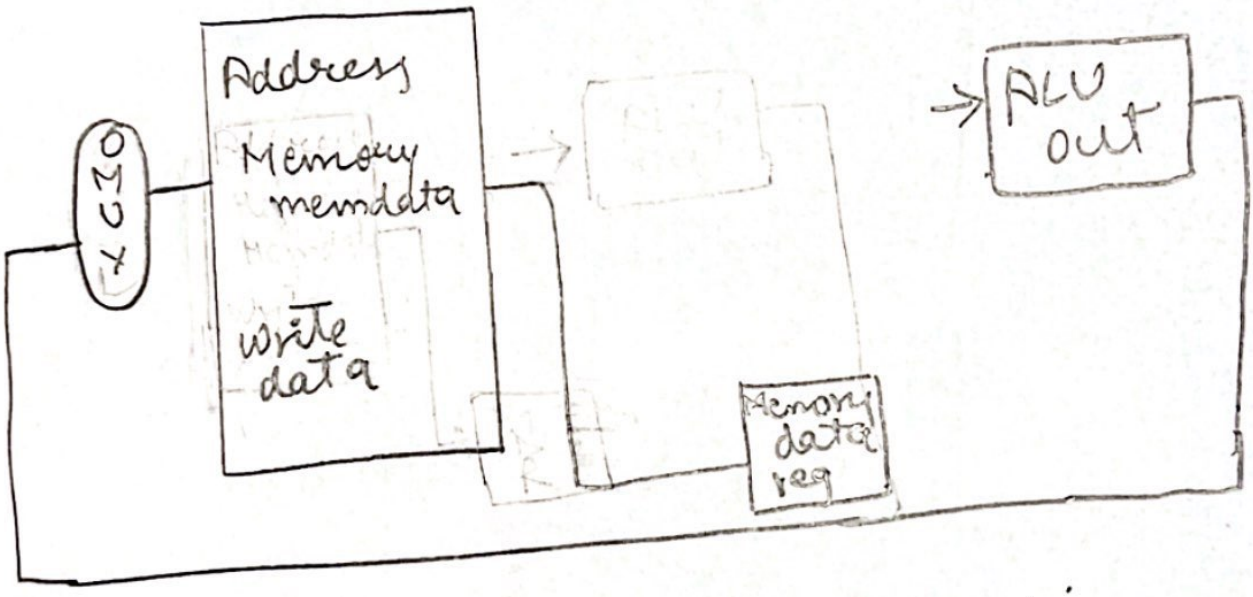
beq: $\frac{15}{21} = 0.625$

j (jump): $\frac{16}{9} = 0.66$

c.]



d.]



e.] Value stored in ALU out is now stored in memory data register

(c)