Design and Implementation of Lookahead Carry Adder (LACA)

1. Introduction

The Lookahead Carry Adder (LACA) is a fast digital adder circuit that overcomes the delay limitations of ripple carry adders by calculating carry signals in advance, based on the generate and propagate concepts. This significantly improves the speed of binary addition, especially for higher-bit operations.

2. Working Principle

Generate and Propagate

In LACA, each bit pair generates two signals:

- Generate (G): Indicates whether a bit pair will generate a carry, defined as *G = A & B*.
- Propagate (P): Indicates whether a carry will propagate through, defined as *P = A ^ B*.

The carry-out of each bit is calculated using these signals, not by waiting for the previous carry, but by expressing it as:

```
C[0] = CIN;
C[1] = G[0] | (P[0] & C[0]);
C[2] = G[1] | (P[1] & G[0]) | (P[1] & P[0] & C[0]);
C[3] = G[2] | (P[2] & G[1]) | (P[2] & P[1] & G[0]) |
       (P[2] & P[1] & P[0] & C[0]);
C[4] = G[3] | (P[3] & G[2]) | (P[3] & P[2] & G[1]) |
       (P[3] & P[2] & P[1] & G[0]) |
       (P[3] & P[2] & P[1] & P[0] & C[0]);
ASSIGN SUM = P ^ C[3:0];
```

THIS EXPLICITLY MEANS:

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ASSIGN SUM[0] = P[0] ^ C[0];
ASSIGN SUM[1] = P[1] ^ C[1];
ASSIGN SUM[2] = P[2] ^ C[2];
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ASSIGN SUM[3] = P[3] ^ C[3];

ASSIGN COUT = C[4] ; THIS PARALLEL COMPUTATION SIGNIFICANTLY REDUCES THE OVERALL DELAY.

3. Verilog Implementation

The 4-bit LACA is implemented using Verilog. It includes:

- Inputs: 4-bit operands A, B and a single-bit carry-in Cin
- Outputs: 4-bit sum and single-bit carry-out

The sum is computed by XORing each propagate signal with the corresponding carry-in.

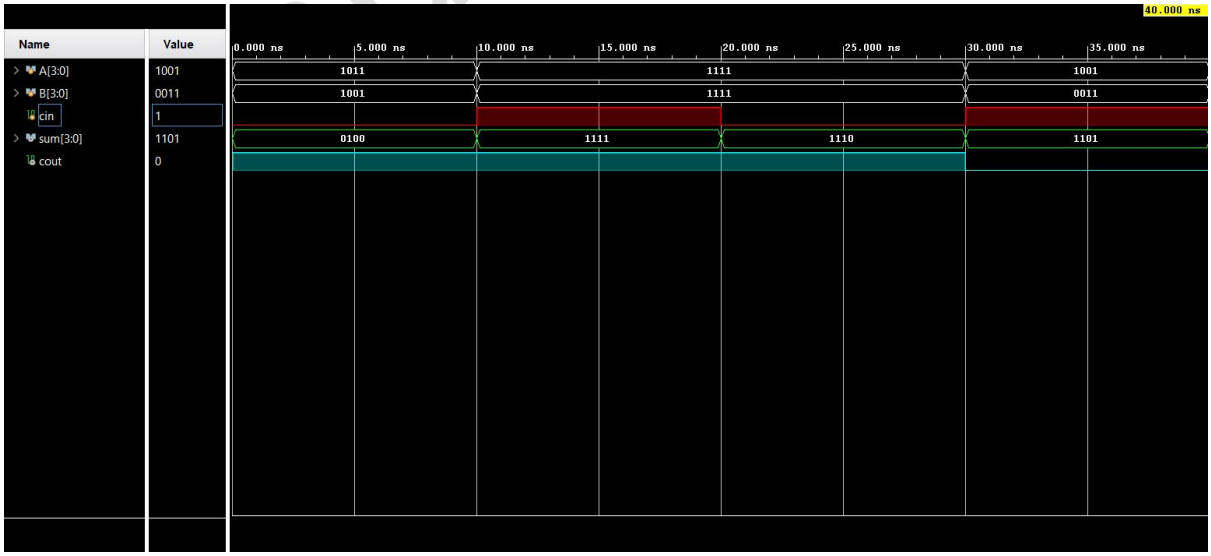
4. Output Results

The following are the test cases used to verify the functionality of the Lookahead Carry Adder:

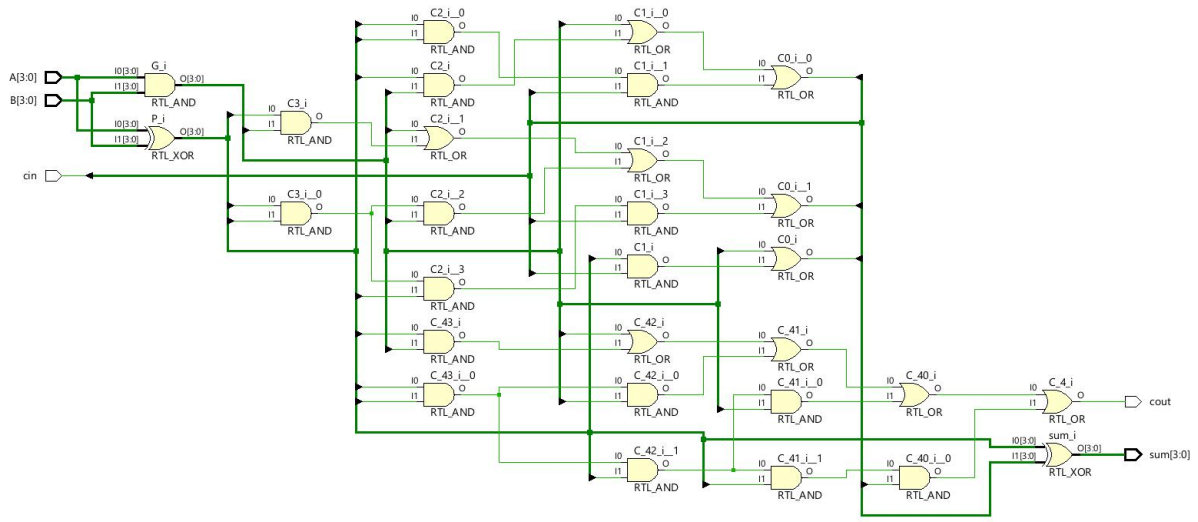
A	B	CIN	SUM	COUT
1011	1001	0	0100	1
1111	1111	1	1111	1
1111	1111	0	1110	1
1001	0011	1	1101	0

These results match the expected outputs and confirm correct functionality.

5. Simulation Diagram



6. Block Diagram



7. Conclusion

The Lookahead Carry Adder demonstrates significant performance improvements in binary addition through the use of parallel carry computation. This design is ideal for high-speed arithmetic logic units (ALUs) in modern processors.