BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: B.Tech
BRANCH: CSE/AIML

SEMESTER : III/ADD
SESSION : MO/2024

SUBJECT: CS235 COMPUTER ORGANIZATION AND ARCHITECTURE

TIME: 3 Hours

FULL MARKS: 50

INSTRUCTIONS:

1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions. Mention Section
3. The missing data, if any, may be assumed suitably.
4. Before attempting the question paper, be sure that you have got the correct question paper.
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

			CO	BL
Q.1(a)	Simplify the Boolean function F(ABCD)=Σ(0,1,2,5,8,9,10) in SOP and POS form.	[5]	1	3
Q.1(b)	Show with the help of a block diagram how the Boolean function f=AB+BC+CA can be realized using only a 4:1 Multiplexer. Find the IEEE754 floating point number for -13.25 in single and double precision	[5]	1	3
Q.2(a)	Convert into assembly language: While(save[i]==k) i+=1;	[5]	2	2
Q.2(b)	Explain the process of subroutine implementation. Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely opcode, two source register identifiers, one destination register identifier, and a twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 200 instructions, calculate the amount of memory (in bytes) consumed by the program text.	[5]	2	3
Q.3(a)	Explain with example 1 and 2 bit branch predictor	[5]	3	4
Q.3(b)	(i)Consider a 3-stage pipelined processor having a delay of 10 ns (nanoseconds), 20 ns, and 14 ns, for the first, second, and the third stages, respectively. Assume that there is no other delay and the processor does not suffer from any pipeline hazards. Also assume that one instruction is fetched every cycle. Determine the total execution time for executing 100 instructions on this processor (ii) The stage delays in a 4 stage pipeline are 800,500,400 and 200picoseconds. The first stage is replaced with a functionality equivalent design involving two stages with respective delays 600 and 350 picoseconds. Calculate the throughput increase of the pipeline	[5]	3	5
Q.4(a)	(i) The cache parameters are 128 B cache,12-bit address,2-way set associative ,32B block. Analyze the cache miss and hit for two times for the following main memory addresses:0x070,0X080,0X068,0X190,0X084,0X178,0X08C,0XF00,0X064. Also calculate the hit ratio. (ii)The Logical address space in a computer system consists of 256 segments. Each segment can have up to 64 pages of 8K words in each. Physical memory consists of 8K blocks of 8Kwords in each. Formulate the logical and physical address formats. (iii A 4- way set associative cache memory with a capacity of 36 KB is built using a block size of 8 words. The word length is of 64 bits. The size of the physical address space is 4GB. Determine the number of bits in the tag field and the tag directory size.	[5]	4	4
Q.4(b)	Explain cache inclusion and exclusion policies. A system has a write through cache with access time of 200ns and hit ratio of 90%.The main memory access time is 400ns.The 75% of the memory references are for read operations. Determine: a) AMAT for read operations only b) AMAT for write operations only c) AMAT for read-write operations. d)Effective hit ratio	[5]	4	4
Q.5(a)	Explain the working of DMA with neat diagram. Consider a computer with a 5 MHz processor. Its DMA controller can transfer 8 bytes in 1 cycle from a device to main memory through cycle stealing at regular intervals. Find the data transfer rate (in bits per second) of the DMA controller if 1% of the processor cycles are used for DMA?	[5]	5	4
Q.5(b)	Explain briefly any two i) Daisy Chaining priority (ii) Snoopy bus protocol (iii) UMA Vs NUMA (iv) Cache coherence (v) SIMD array processor	[5]	5	2

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