## Experiment 8

**Aim** : Programming and interfacing using 8086 hardware kit ( 8253-PIT and 8086)

**Theory**:

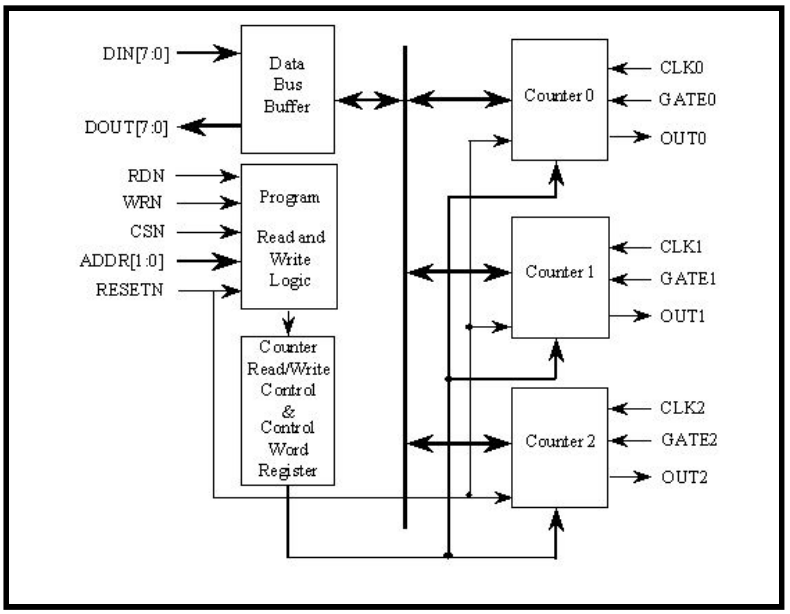


Fig 1:Architecture of the 8253 Programmable interrupt timer

The programmable Interval Timers are specially designed by Intel called 8253 and 8254 constructed for microprocessors to perform timing and counting functions by using three 16-bit registers. Each counter has 2 input pins, i.e. Clock & Gate, and 1 pin is for "OUT" output. To perform a counter, a 16-bit count is loaded in its register. On giving command, it begins to decrease the count until it reaches 0, then it produces a pulse that can be used to interrupt the CPU.

The most prominent features of 8253/54 are as follows −

1. It has three independent 16-bit down counters.
2. It can handle inputs from DC to 10 MHz.
3. These three counters can be programmed for any count that is either binary or BCD count.
4. It is compatible with almost all microprocessors.
5. 8254 consists of powerful command called READ BACK command, which allows the user to check the count value, the programmed mode, the current mode, and the current status of the counter.

In the above figure, there are three counters, a data bus buffer, Read/Write control logic, and a control register. Each counter consists of two input signals - CLOCK & GATE, and one output signal - OUT.

**Data Bus Buffer :** It is a tri-state, bi-directional, 8-bit data buffer, which helps in interfacing the 8253/54 to the system data bus. It has three basic functions −

1. Programming the modes of 8253/54.
2. Loading the count registers.
3. Reading the count values.
4.

**Read/Write Logic :** It includes 5 signals, i.e. RD, WR, CS, and the address lines A0 & A1. In the peripheral I/O mode, the RD and WR signals are connected to IOR and IOW, respectively. In the memory mapped I/O mode, these are connected to MEMR and MEMW. Address lines A0 & A1 of the CPU are connected to lines A0 and A1 of the 8253/54, and CS is tied to a decoded address. The control word register and counters are selected according to the signals displayed on lines A0 & A1

**Control Word Register :**This register helps in accessing lines when A0 & A1 are at logic 1. It is used to write a command word, which specifies the counter to be used, its mode, and either a read or write operation. Following table shows the result for various control inputs.

**Counters**: Each counter contains a single, 16 bit-down counter, which can perform operations in either binary or BCD. Its input and output signals are configured by the mode selection that are stored in the control word register.

**code**:

| | |
|---|---|
| MOV AL,80<br>OUT 33,AL<br>MOV AL,55<br>OUT 30,4L<br>MOV AL,AA<br>OUT 31,AL<br>MOV AL,0F<br>OUT 32,AL | B0 , 80<br>E6 , 33<br>B0 , 55<br>E6 , 30<br>B0 , AA<br>E6 , 31<br>B0 , 0F<br>E6 , 32 |