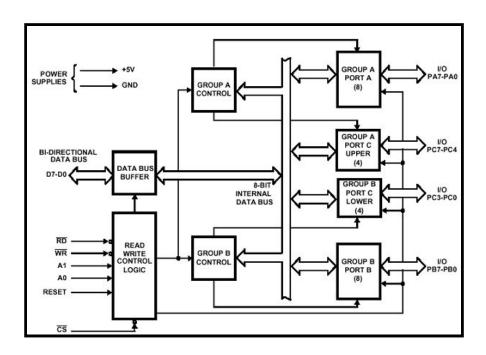
# **Experiment 9**

Aim: Programming and interface using 8086 hardware kit (8255-PPI with 8086)

### Theory:



The 8255A is a general purpose programmable I/O device designed to transfer the data from I/O to interrupt I/O under certain conditions as required. It can be used with almost any microprocessor.

It consists of three 8-bit bidirectional I/O ports (24I/O lines) which can be configured as per the requirement.

Ports of 8255A: 8255A has three ports, i.e., PORT A, PORT B, and PORT C.

- 1. Port A contains one 8-bit output latch/buffer and one 8-bit input buffer.
- 2. Port B is similar to PORT A.
- 3. Port C can be split into two parts, i.e. PORT C lower (PC0-PC3) and PORT C upper (PC7-PC4) by the control word.

These three ports are further divided into two groups, i.e.

- 1. Group A includes PORT A and upper PORT C.
- 2. Group B includes PORT B and lower PORT C.

These two groups can be programmed in three different modes, i.e. the first mode is named as mode 0, the second mode is named as Mode 1 and the third mode is named as Mode 2.

# Operating Modes: 8255A has three different operating modes –

- 1. **Mode 0** In this mode, Port A and B is used as two 8-bit ports and Port C as two 4-bit ports. Each port can be programmed in either input mode or output mode where outputs are latched and inputs are not latched. Ports do not have interrupt capability.
- 2. **Mode 1** In this mode, Port A and B is used as 8-bit I/O ports. They can be configured as either an input or output ports. Each port uses three lines from port C as handshake signals. Inputs and outputs are latched.
- 3. **Mode 2** In this mode, Port A can be configured as the bidirectional port and Port B either in Mode 0 or Mode 1. Port A uses five signals from Port C as handshake signals for data transfer. The remaining three signals from Port C can be used either as simple I/O or as handshake for port B.

# Features of 8255A - The prominent features of 8255A are as follows -

- 1. It consists of 3 8-bit IO ports i.e. PA, PB, and PC.
- 2. Address/data bus must be externally demux'd.
- 3. It is TTL compatible.
- 4. It has improved DC driving capability.

### Code:

B0,30
E6,53
B0,05
E6,50
B0,00
E6,50

