Electronics and communication engineering
Institute Of Technology Nirma University, Ahmedabad, India

DLD PROJECT

Topic: Traffic Signal Controller using FSM

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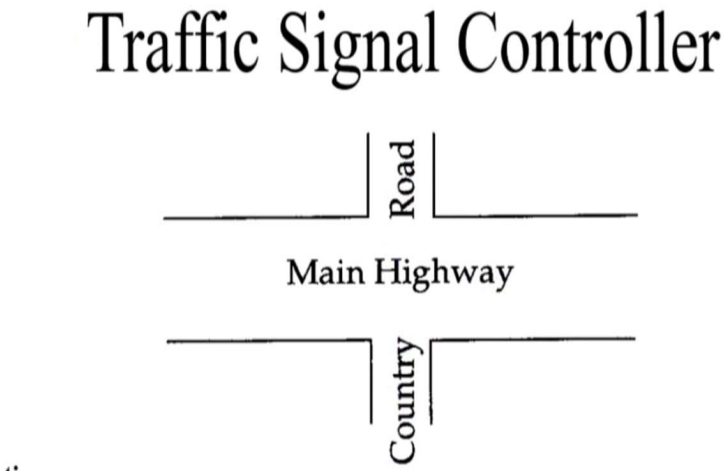
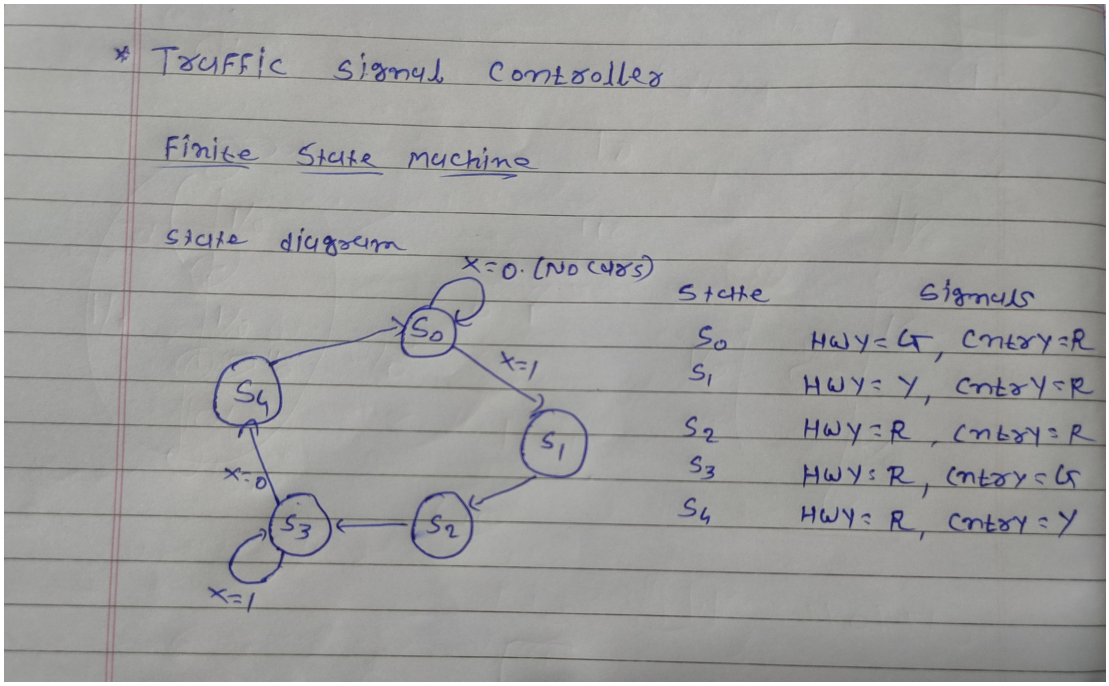
Specification:

- As soon as there are no cars on the country road, the country road traffic signal turns yellow and then red and the traffic signal on the main highway turns green again.
- There is a sensor to detect cars waiting on the country road. The sensor sends a signal X as input to the controller. X = 1 if there are cars on the country road; otherwise, X= 0.
- There are delays on transitions from \$1 to \$2, from \$2 to \$3, and from S4 to SO. The delays must be controllable.
- The traffic signal for the main highway gets highest priority because cars are continuously present on the main highway. Thus, the main highway signal remains green by default. Occasionally, cars from the country road arrive at the traffic signal. The traffic signal for the country road must turn green only long enough to let the cars on the country road go.
- Build a verilog model for Traffic signal control using state machine diagram.

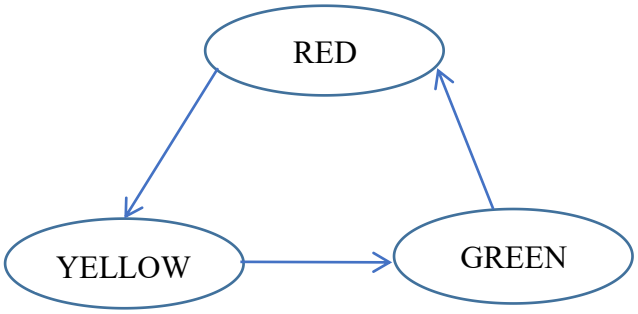


[Fig-1-Traffic Signal Diagram]



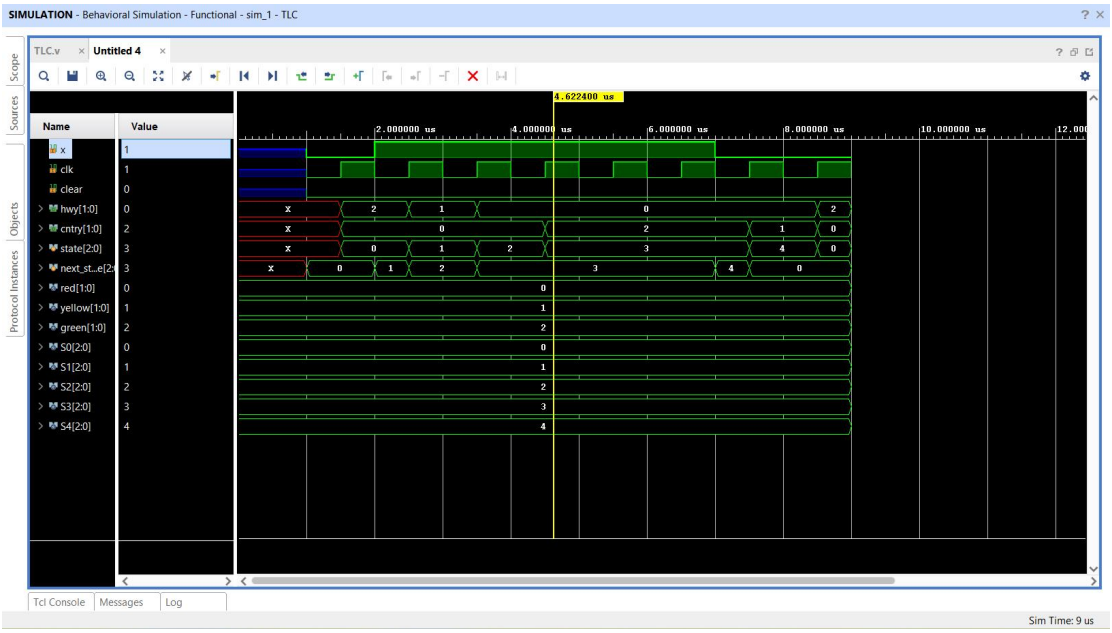
[Fig-2- State Diagram]

Red = 00
Yellow=01
Green=10



[Fig-3- RYG Light]

OUTPUT:



[Fig-4- Output Waveform]