MCA-104: Computer System Architecture
Master of Computer Applications
Semester First, Nov/Dec 2017

Time: Three Hours **Max. Marks: 70**

1.

a. What is the advantage of using 2s complement to represent negative numbers over 1s complement. **(2)**

a. Explain with diagram match logic for one word of associative memory. **(5)**

b. A digital computer has a memory unit of 64K X 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. Answer the following **(2+2+1=5)**

i. How many bits are there in the tag, index, block and word fields of the address format?

ii. How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit.

iii. How many blocks can the cache accommodate?

2.

a. Why does DMA have priority over the CPU when both request a memory transfer? **(3)**

b. Why are the read and write control lines in DMA controller bidirectional? Under what condition and for what purpose are they used as outputs? **(3)**

c. What is the difference between isolated I/O and memory-mapped I/O? What are the advantages and disadvantages of each? **(5)**

3.

a. Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks. **(3)**

b. Write a program to evaluate the arithmetic statement given below using an accumulator type computer with one address instructions. **(4)**

$$X= [A-B+C*(D*E-F)] / [G+H*K]$$

c. The sub operations performed in each segment of the pipeline are as follows:

$R1 \leftarrow A_i$, $R2 \leftarrow B_i$

$R3 \leftarrow R1 * R2$, $R4 \leftarrow C_i$

$R5 \leftarrow R3 + R4$

The pipeline has the following propagation times: 40ns for the operands to be read from memory into registers R1 and R2, 45ns for the signal to propagate through the multiplier, 5ns for the transfer into R3, and 15ns to add the two numbers into R5. **(1+2+2+1=6)**

i. What is the minimum clock cycle time that can be used?

ii. A nonpipeline system can perform the same operation by removing R3 and R4. How long will it take to multiply and add the operands without using the pipeline?

iii. Calculate the speedup of the pipeline for 10 tasks.

iv. What is the maximum speed up that can be achieved?

4.

a. What are the basic differences between a branch instruction, a call subroutine instruction and program interrupt? **(3)**

b. Draw the block diagram of a Bidirectional shift register with parallel load and explain the operation by means of a function table. **(5)**

c. An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is: **(5)**

i. Direct
ii. Immediate
iii. Relative
iv. Register indirect
v. Index with R1 as the index register.

5.

a. Write difference between Reduced Instruction Set Computer (RISC) and Complex Instruction Set Computer (CISC) class of computer system architecture. **(4)**

b. Write an assembly language program to evaluate the logic exclusive-OR of two logic operands. **(4)**

c. Given the instructions related to AR as follows:

R'T0 : AR <- PC
R'T1 : IR <- M[AR]
R'T2 : AR <- IR(0-11)
D7'IT3: AR <- M[AR]
RT0 : AR <- 0
RT1 : M[AR] <- TR
D0T4 : DR <- M[AR]
D1T4 : DR <- M[AR]
D2T4 : DR <- M[AR]
D3T4 : M[AR] <- AC
D4T4 : PC <- AR
D5T4 : M[AR] <- PC, AR <- AR +1
D5T5 : PC <- AR
D6T4 : DR <- M[AR]
D6T6 : M[AR] <- DR

Design logic diagram for all the control inputs, i.e., load, increment and clear of AR register. **(4)**

6.

a. Using DeMorgan's theorem, show that: **(2)**

A+A'B+A'B'=1

b. Construct a 2-to-4 line decoder with only NOR gates. Include an enable input. **(3)**

c. Design a combinational circuit that performs the four logic operation of exclusive-OR, exclusive-NOR, NOR, and NAND. Show the logic diagram of one typical stage. **(4)**