Modeling of nano-scale PLL using Verilog HDL

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Abstract

The design of integrated circuits at the nano scale has become a focal point in the contemporary semiconductor industry, which pursues low power consumption and high-speed operation. This research focuses on leveraging nano processes for manufacturing chips, emphasizing the use of phase-locked loops (PLL) in various engineering domains that demand precise phase alignment of signals and frequency source synthesis. The developed Verilog HDL model of PLL includes essential components like pre-divider, main-divider, scalar, voltage-controlled oscillator (VCO), phase frequency detector and charge pump. The study comprehensively implements three operating characteristics – Start-Up operation, Bypass mode operation and Glitch-Free Scaler operation. Utilizing ModelSim and Xilinx vivado environment.

Keywords : Nano-scale integrated circuits, Phase-Locked Loop (PLL), Verilog HDL, Pre-divider, Main-divider, Scalar, Voltage-Controlled Oscillator (VCO), Phase Frequency Detector, ModelSim, Xilinx Vivado.

1 Introduction

The advancement in semiconductor manufacturing process technology has enabled the integration of tens of thousands of transistors into a single chip. Refining the line width of semiconductor circuits through nano processes holds the promise of reducing power consumption and increasing speed. However, the introduction of nano processes has brought challenges, narrowing the gap between architectural limits and devices and leading to increased RC delay and heating issues. Manufacturing chips through nano processes introduces additional complexities such as fab-in and fab-out periods, as well as production costs. These considerations underscore the importance of minimizing design errors during circuit development, relying on high-accuracy and reliable models from the early stages of modeling. A well-defined model significantly aids in designing circuits more efficiently and accurately.

This study focuses on Verilog HDL modeling for a Phase-Locked Loop (PLL) designed with a nano process. PLLs find applications in various fields, particularly in the communication sector, where rapid data transmission, reception, and signal processing demand increased frequencies. Verilog HDL proves advantageous over analog modeling due to its ability to provide clear results composed of 0s and 1s, facilitating efficient result verification. Digital modeling significantly accelerates the verification process, crucial for PLLs requiring simulations with extensive test vectors. This project is structured into two main parts: first, it elucidates the mode-specific behavioral characteristics of the modeled PLL block, and subsequently, it presents simulation results obtained through Verilog HDL.

2 Motivation

"Modeling of nano-scale PLL using Verilog HDL" is to design a PLL (Phase Locked Loop) with a nano process applied, which can be used in various engineering fields that require phase fixation of signals and synthesis of frequency sources. The design of integrated circuits with nano-processes has established itself as an important center in the modern semiconductor industry, and to utilize the advantages of low power and high speed, a lot of effort is being made to manufacture chips through nano processes. The project aims to contribute to chip development by reducing design errors as much as possible based on models with high accuracy and reliability from the modeling stage.

3 Related works

1. Multigate transistors as the future of classical metal–oxide– semiconductor field-effect transistors.
Author: Isabelle Ferain, Cynthia A. Colinge, and Jean-Pierre Colinge
Year: 2018
Abstract: Transistors have been shrinking exponentially in size, and therefore the number of transistors in a single microelectronic chip has been increasing exponentially. Such an increase in packing density was made possible by continually shrinking the metal–oxide–semiconductor field-effect transistor (MOSFET). In the current generation of transistors, the transistor dimensions have shrunk to such an extent that the electrical characteristics of the device can be markedly degraded, making it unlikely that the exponential decrease in transistor size can continue. Recently, however, a new generation of MOSFETs, called multigate transistors, has emerged, and this multigate geometry will allow the continuing enhancement of computer performance into the next decade.

2. Digital signal propagation delay in a nano-circuit containing reactive and resistive elements
Author: Vijay K. Arora, Desmond C.Y. Chek, and Abdul Manaf Hashim
Year: 2018
Abstract: The transient switching delay in a micro/nano-scale circuit containing resistive and reactive elements are sternly affected by the surge in the resistance arising from sub-linear current–voltage (I–V) characteristics limited by the velocity and current saturation. The saturation arises due to the realignment of randomly oriented velocity vectors to the unidirectional streamlined ones in a high electric field when voltage applied across a resistor exceeds its decreasing critical value with reduced channel length. The frequency response $f = 1/2\pi\tau t$ is affected by a transit time delay τt is lower than that predicted from the application of Ohm's law. The resistance surge dramatically boosts the RC time constant and switching delay and attenuates the L/R time constant and switching delay.

3. A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors

Author: I.A. Young, J.K. Greason, and K.L. Wong
Year: 2017
Abstract: A microprocessor clock generator based on an analog phase-locked loop (PLL) is described for deskewing the internal logic control lock to an external system lock. This PLL is fully generated onto a 1.2-million-transistor microprocessor in 0.8-mu m CMOS technology without the need for external components. It operates with a lock range from 5 to 110 MHz. The clock skew is less than 0.1 ns, with a peak-to-peak jitter of less than 0.3 ns for a 50-MHz system clock frequency.

4. Design of a Digital PLL Real Number Model Using SystemVerilog
Author: Nikolaos Georgoulopoulos, and Alkiviadis Hatzopoulos
Year: 2019
Abstract: Mixed-signal applications constitute a significant trend in the semiconductor industry. Huge effort is focused on creating fast and accurate mixed-signal designs, which include both analog and digital parts. A widely used mixed-signal circuit in modern electronics is the phase-locked loop (PLL).

4 Proposed Method

The PLL system is modeled using Verilog HDL and has a wide-output-frequency range for frequency synthesis. Fig. 1 shows the block diagram of the PLL Model. For the PLL Modeling, the model was composed of a 6-bit Pre-Divider, a 10-bit Main-Divider, a 3-bit Scaler, a Voltage Controlled Oscillator(VCO), a Phase Frequency Detector, and a Charge Pump.

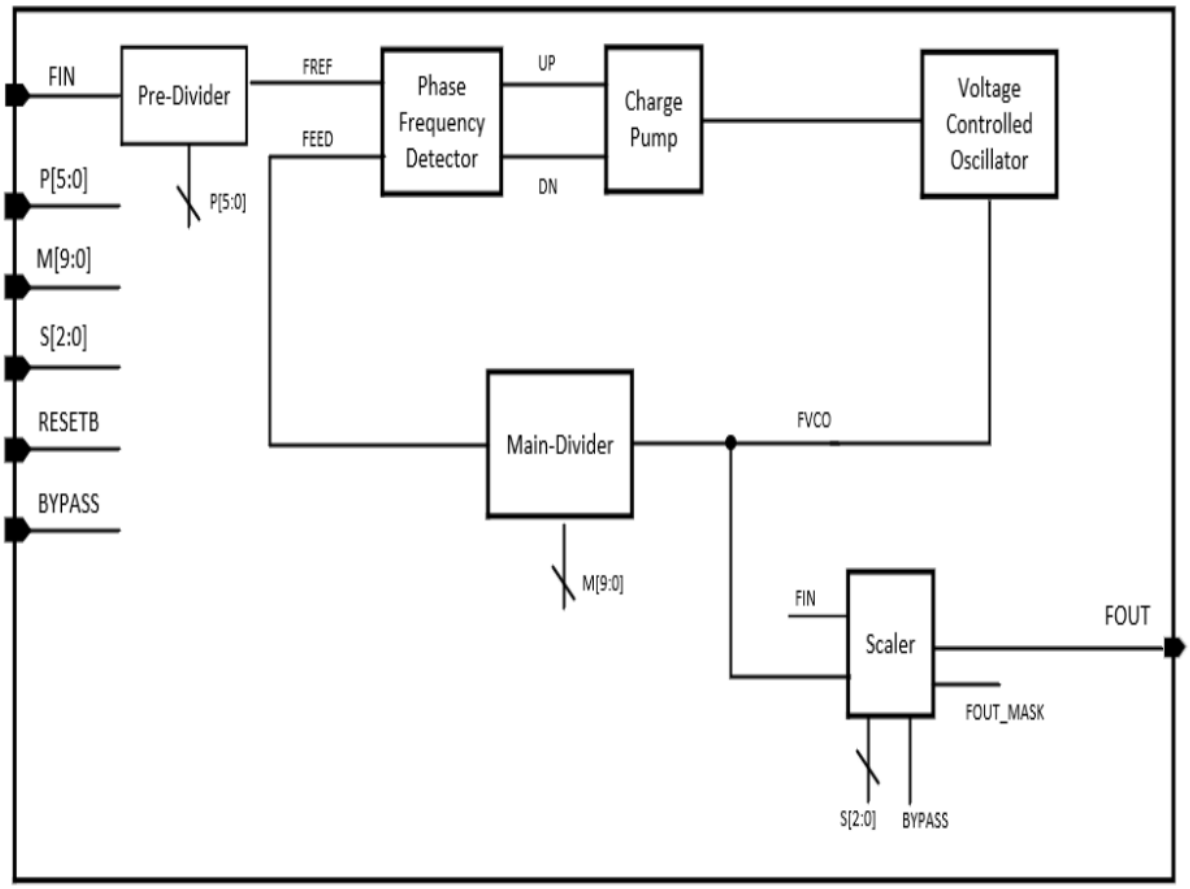

Figure 1: PLL Modeling Functional Block Diagram

The output frequency is related to the input frequency through the following equations.

$$F_{FREF} = \frac{F_{FIN}}{p}$$

$$F_{FVCO} = \frac{(m \times 2 \times F_{FIN})}{p}$$

$$F_{FOUT} = \frac{(m \times 2 \times F_{FIN})}{p \times 2^{s}}$$

On each equation, p, m, and s are values represented by P[5:0], M[9:0], and S[2:0], respectively. The maximum output frequency of the PLL is 7.5GHz.

Figure 2 shows the frequency characteristics of our proposed model. The input frequency(F_{FIN}) ranges from 4MHz to 300MHz. The reference frequency(F_{FREF}) is a frequency that comes through the Pre-Divider, ranging from 4MHz to 12MHz. The VCO range of the output frequency(F_{FVCO}) is 3300MHz to 7500MHz and the frequency of the PLL's output(F_{FOUT}) can cover from 51.563MHz to 7500MHz.

Characteristics	***Symbol***	***Min***	***Max***	***Unit***
Input frequency	F_{FIN}	4	300	MHz
Reference frequency (F_{FIN} / p)	F_{FREF}	4	12	MHz
Frequency of VCO's output	F_{FVCO}	3300	7500	MHz
Frequency of PLL's output	F_{FOUT}	51.563	7500	MHz
Lock Time	T_{LT}	-	150	cycles

Figure 2: Electrical characteristics of PLL

when en is 0, the output frequency F_{FOUT} comes out zero, whatever the value of bypass is. On the other hand, when en is 1, there is a difference between when bypass is 0 and 1. When bypass is 0, the output frequency F_{FOUT} operates as an unstable clock before the lock time, and after the lock time, it is output as (3). When bypass is 1, the PLL enters the Bypass mode, and the output frequency F_{FOUT} becomes the same value as the input frequency F_{FIN}. The relationship between en and bypass is shown in Figure 3.

en	bypass	F_{FOUT}
0	0	0
0	1	0
1	0	Unstable clock (before lock time) F_{FOUT} $=F_{FVCO}/(S^2)$ (after lock time)
1	1	F_{FIN}

Figure 3: Functional description of F_{FOUT}

5 Results and Discussion

The implemented nano-scale PLL model with power report, utilization report, RTL Schematic and simulation are shown in the following figures.

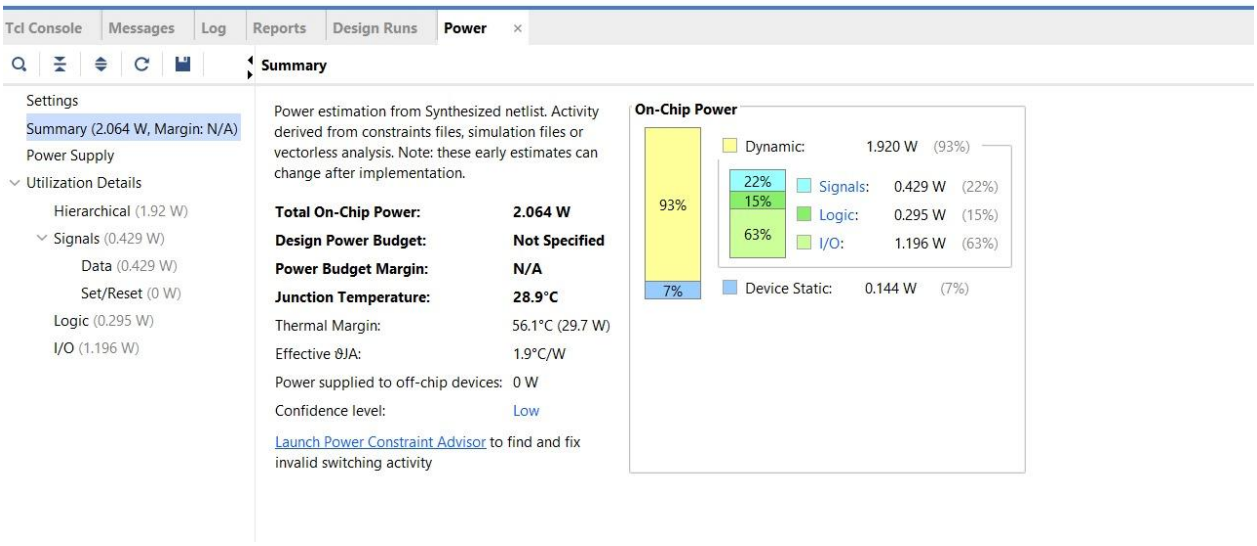

Figure 4: Power Report

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	38	0	134600	0.03
LUT as Logic	38	0	134600	0.03
LUT as Memory	0	0	46200	0.00
Slice Registers	20	0	269200	<0.01
Register as Flip Flop	20	0	269200	<0.01
Register as Latch	0	0	269200	0.00
F7 Muxes	0	0	67300	0.00
F8 Muxes	0	0	33650	0.00

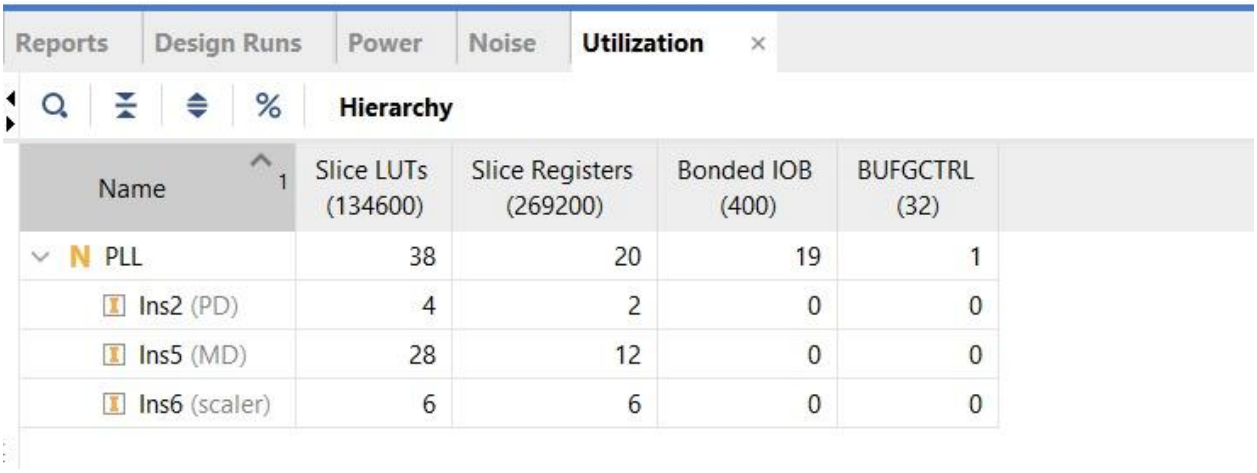

Figure 5,6: Utilization Report

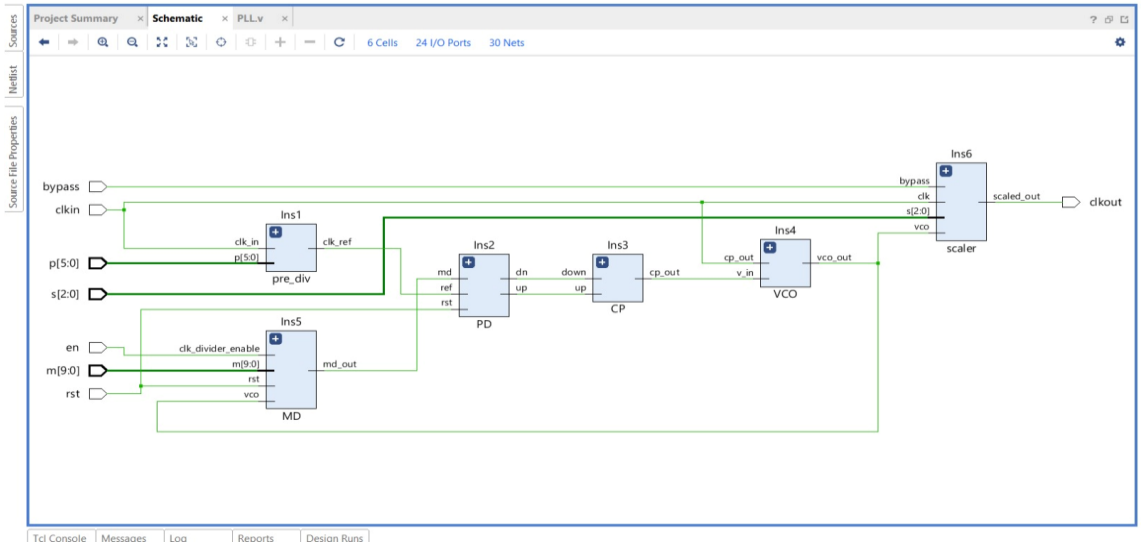

Figure 7: RTL Schematic

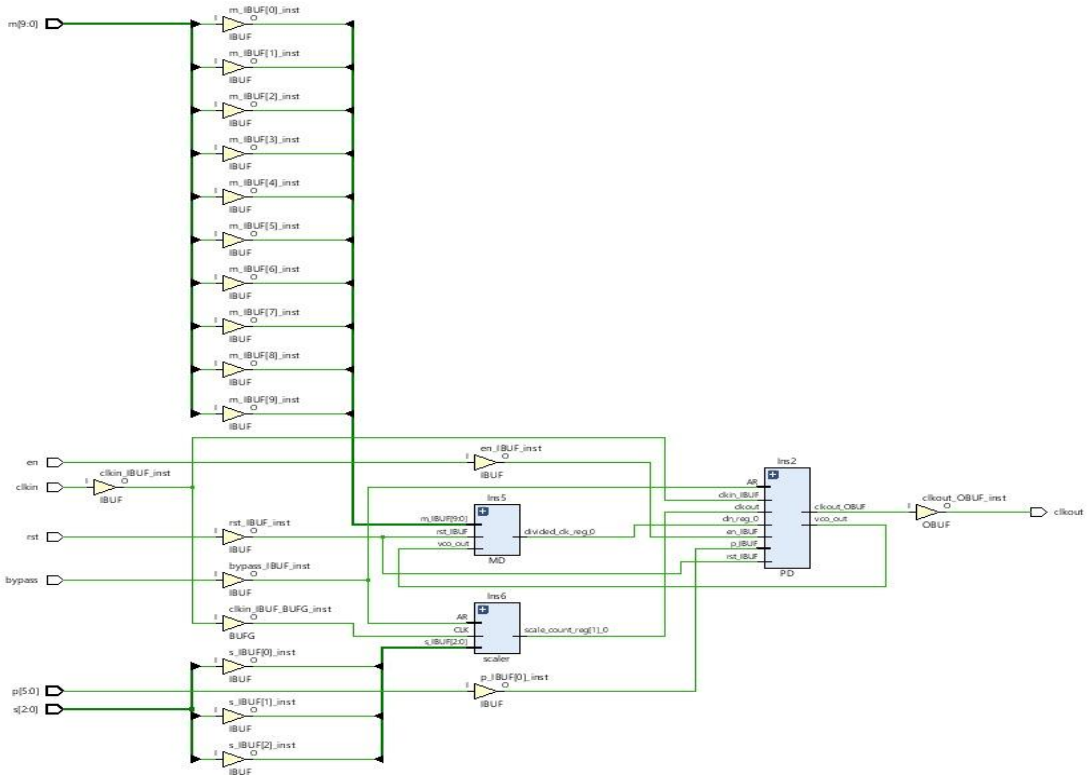

Figure 8: Synthesis design

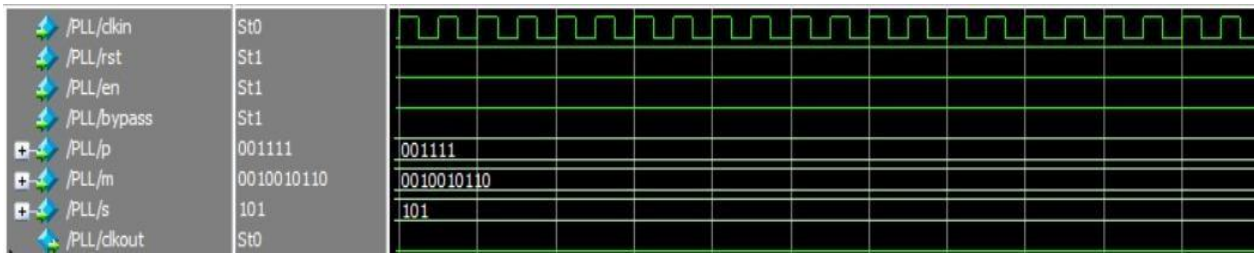

Figure 9: Case 1: rst (reset) = 1 [All Modules are Intialized]

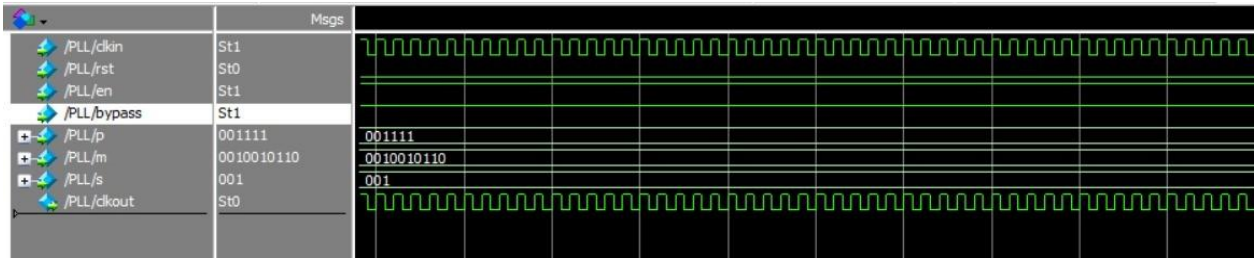

Figure 10: Case 2: rst (reset) = 0 , bypass = 1

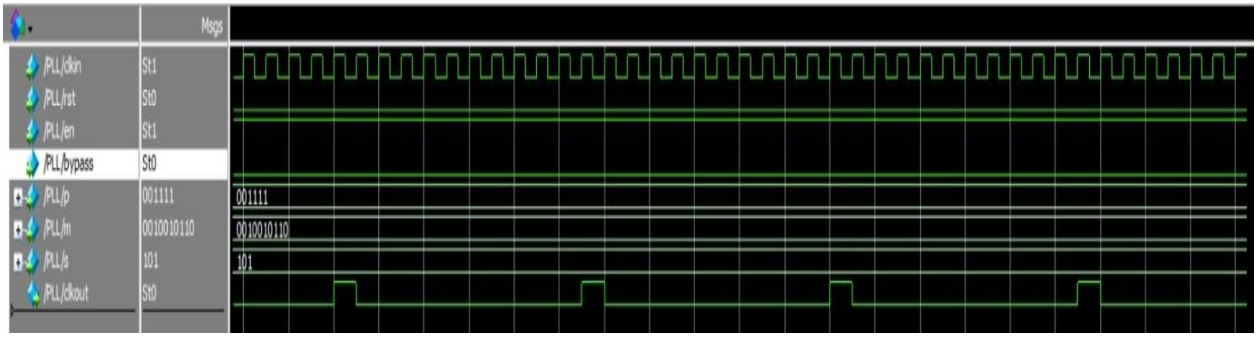

Figure 11: Case 3: s (scaler operation factor) = 5

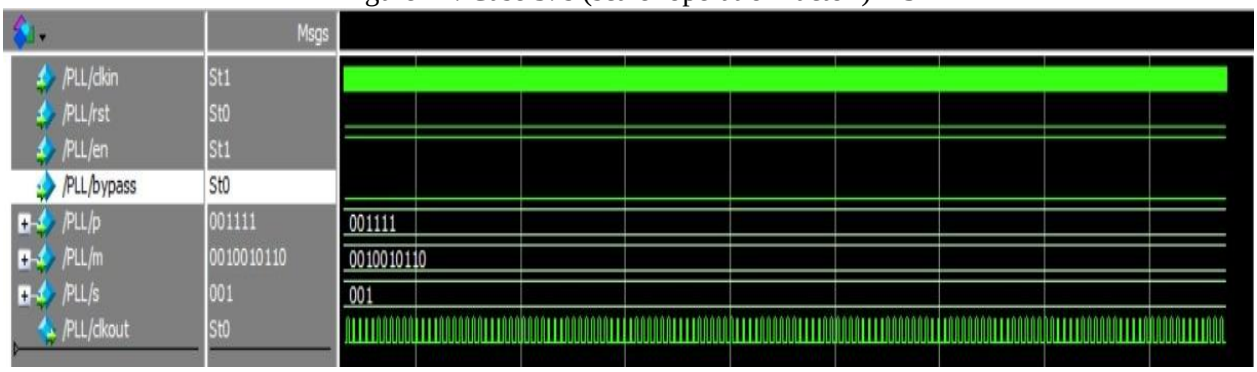

Figure 12: Case 4: s (scaler operation factor) = 1

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