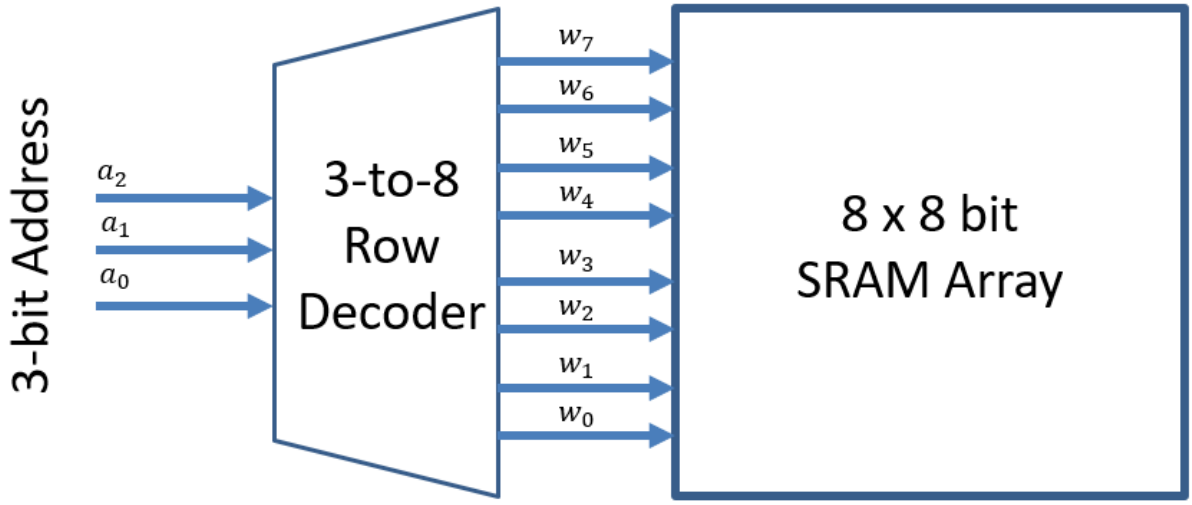
EE224 Project Description

8x8 bit SRAM Array with a Row Decoder



The project is about building a 8 x 8 bit SRAM array, using 6T SRAM cells built in 65nm technology. The data read or written from or to the SRAM Array is controlled using a 3-to-8 row decoder with an input of a 3-bit address.