Analysis and Simulation of a CMOS VCO

1. Schematic setup

Using a library gpdk045 technology in cadence, create the schematic shown in Figure 1. This is an LC-based CMOS voltage controlled oscillator (VCO) which is designed to operate around 1.9GHz. The component values are shown in tables 1-2. The LC tank is formed by inductors L1 and L0 (with a Q factor of around 5 at the resonance frequency of the tank determined by resistors R2, R3), and the varactors implemented with pmos transistors P0 and P1. C0 and C1 represent a load parasitic capacitance. The negative conductance necessary to start and sustain the oscillations is implemented with the cross coupled nmos transistors N0 and N1.

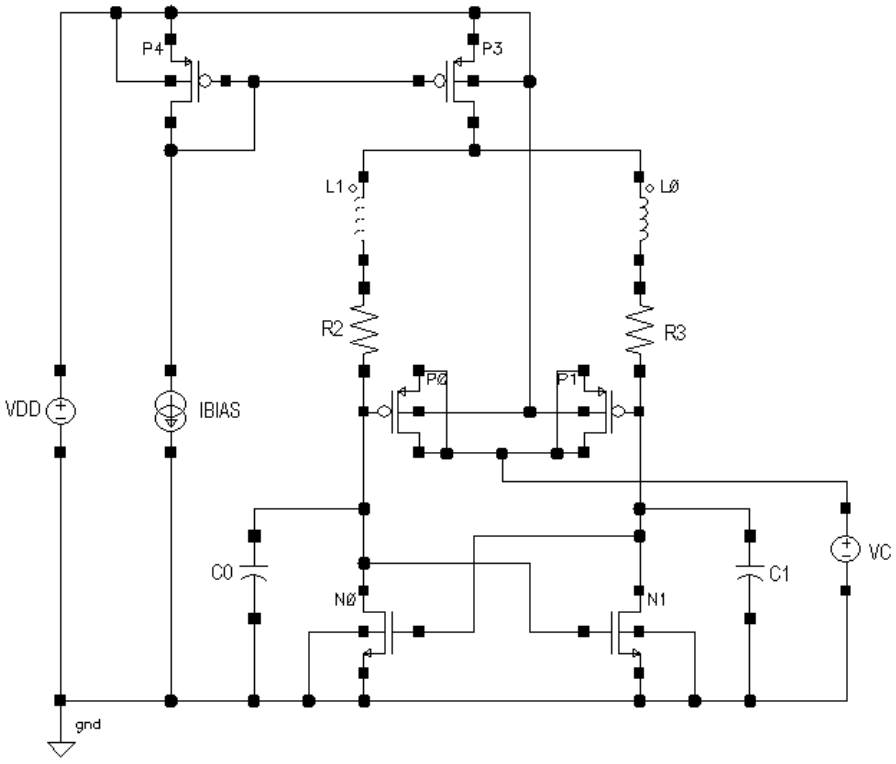

Figure 1. VCO circuit schematic

Table 1. Transistor parameters

Transistor	W [um]	L [um]	Multiplicity
N0, N1	9	0.6	8
P0, P1	15	1.2	12
P3, P4	30	1.8	16

Table 2. Component values

Component	Value
L0, L1	8n
R2, R3	20ohms
C0, C1	200fF
IBIAS	1mA
VC	2V
VDD	3V

2. Transient simulation

A transient simulation is a relatively fast way to verify the functionality of the VCO and estimate its settling time and output frequency. Run a conservative transient analysis for a period of around 20ns. If the oscillations do not start you may need to add an initial condition to one of the output voltages. Go to the menu Simulation -> Convergence Aids -> Initial Condition… and set one of the output nodes to be few mV higher or lower than its regular operating point.

Plot the output of the oscillator, you can measure the frequency of oscillation using the calculator. Take note of the time it takes to the VCO to have a stable amplitude since this time will be used in the PSS simulations.

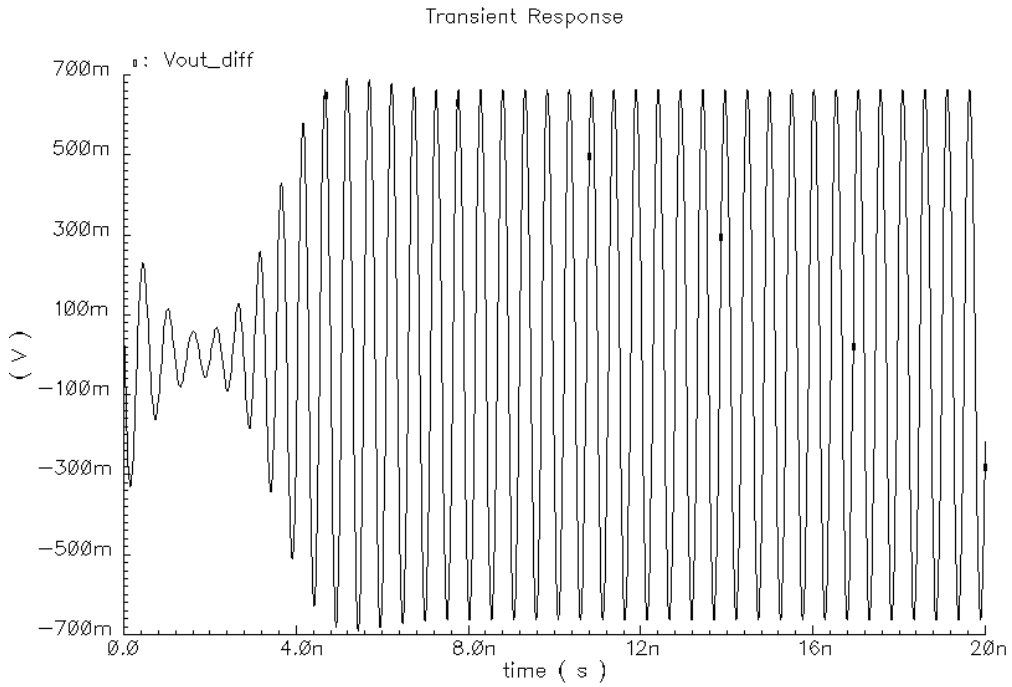

Figure 2. Transient response of the VCO

3. PSS simulation

PSS analysis can be used to find the oscillation frequency, spectrum and amplitude of the VCO. To obtain the phase noise, pnoise analysis must also be performed.

2.1 Simulation setup for the VCO.

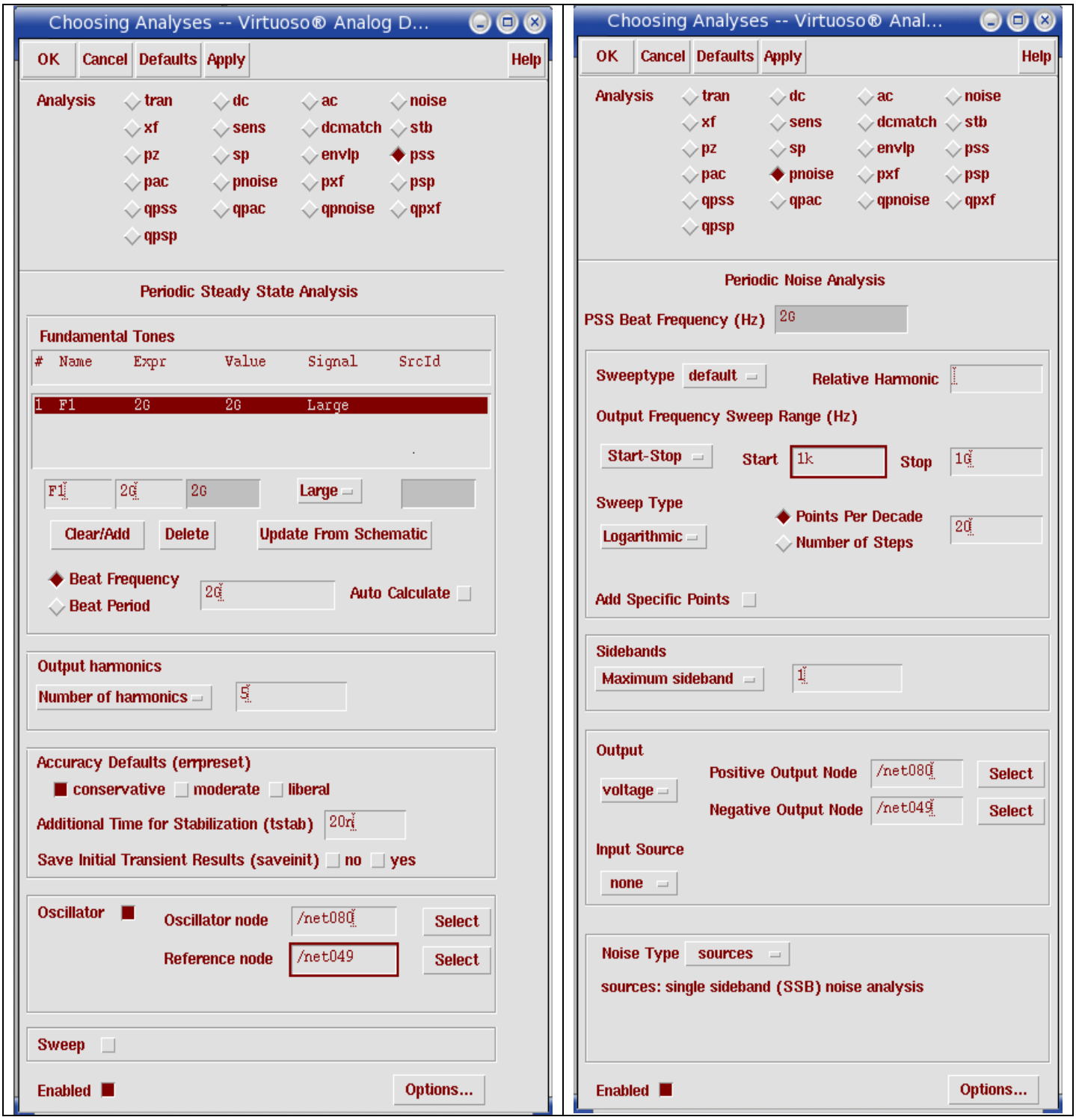

Figure 3. PSS and pnoise simulation setups

NOTE:

- The positive and negative output nodes are the drain/gate terminals of transistors N0 and N1.
- It is very important to choose a conservative analysis to obtain accurate phase noise simulation results. Choosing moderate analysis can change the results by a number of dBs.
- Choose the time for stabilization according to the results of your transient simulation.
- The fundamental frequency in this case is just a starting assumption. PSS will accurately find the actual period of the oscillations.

When the simulation is finished, configure the results window as shown in Figure 3.

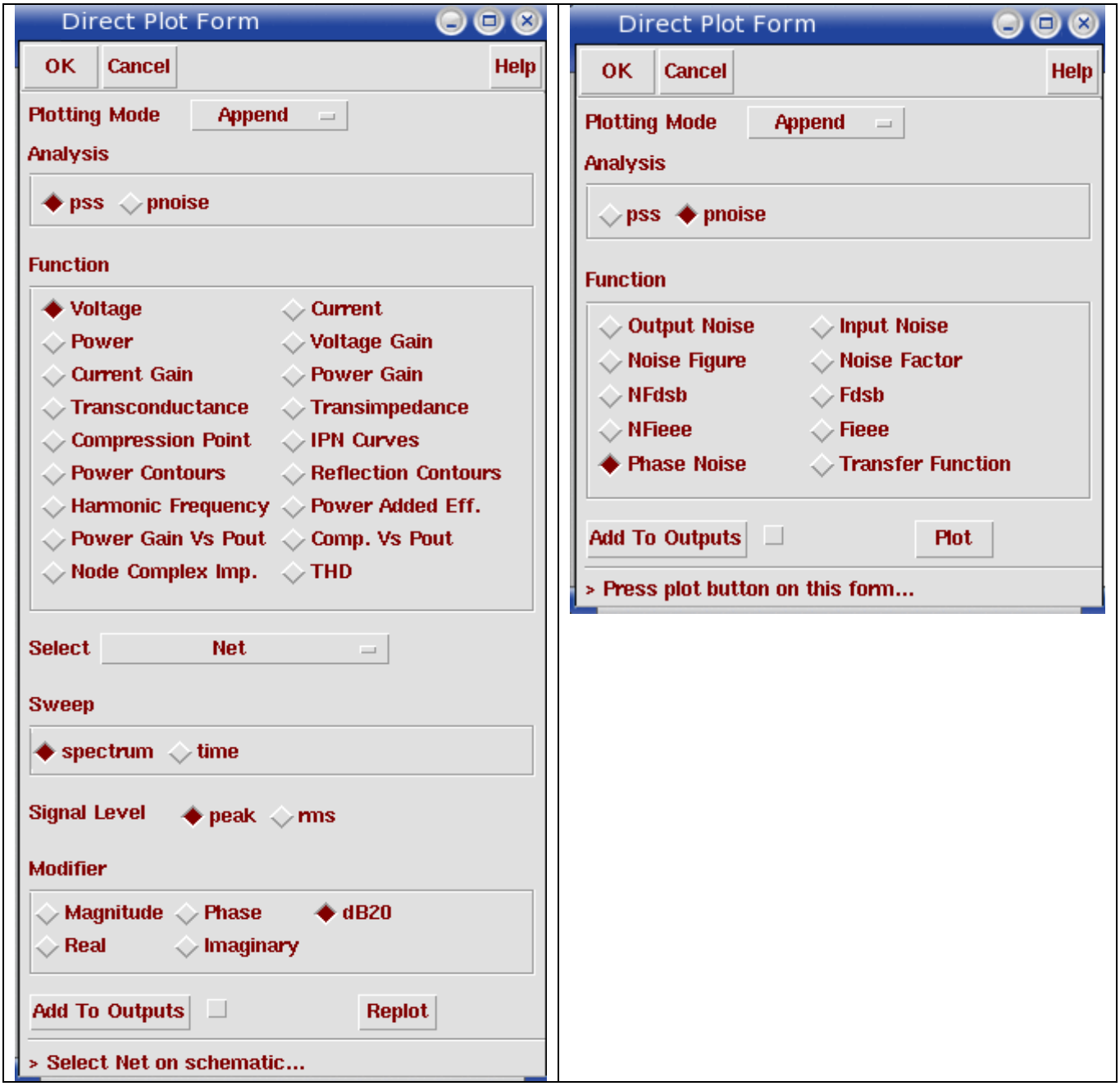

Figure 4. PSS results setup

Select one of the differential outputs to plot the single ended output voltage as shown below.

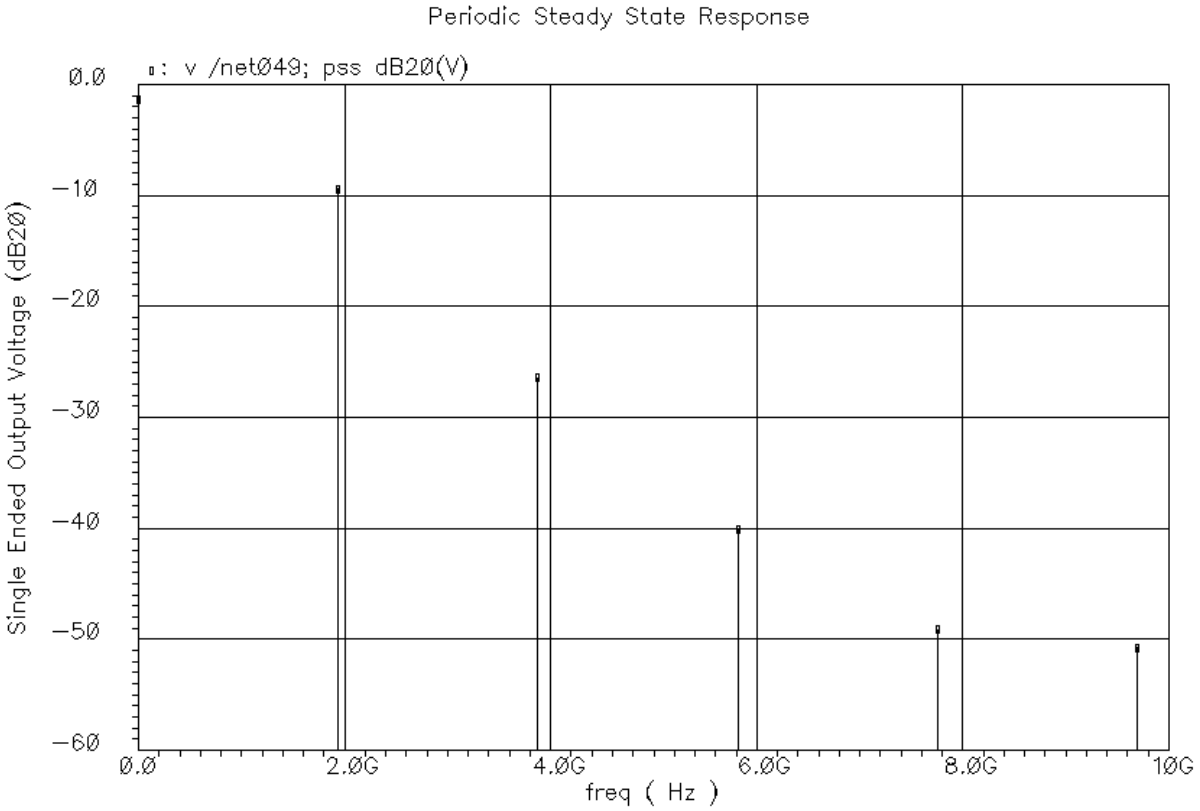

Figure 5. VCO Output spectrum

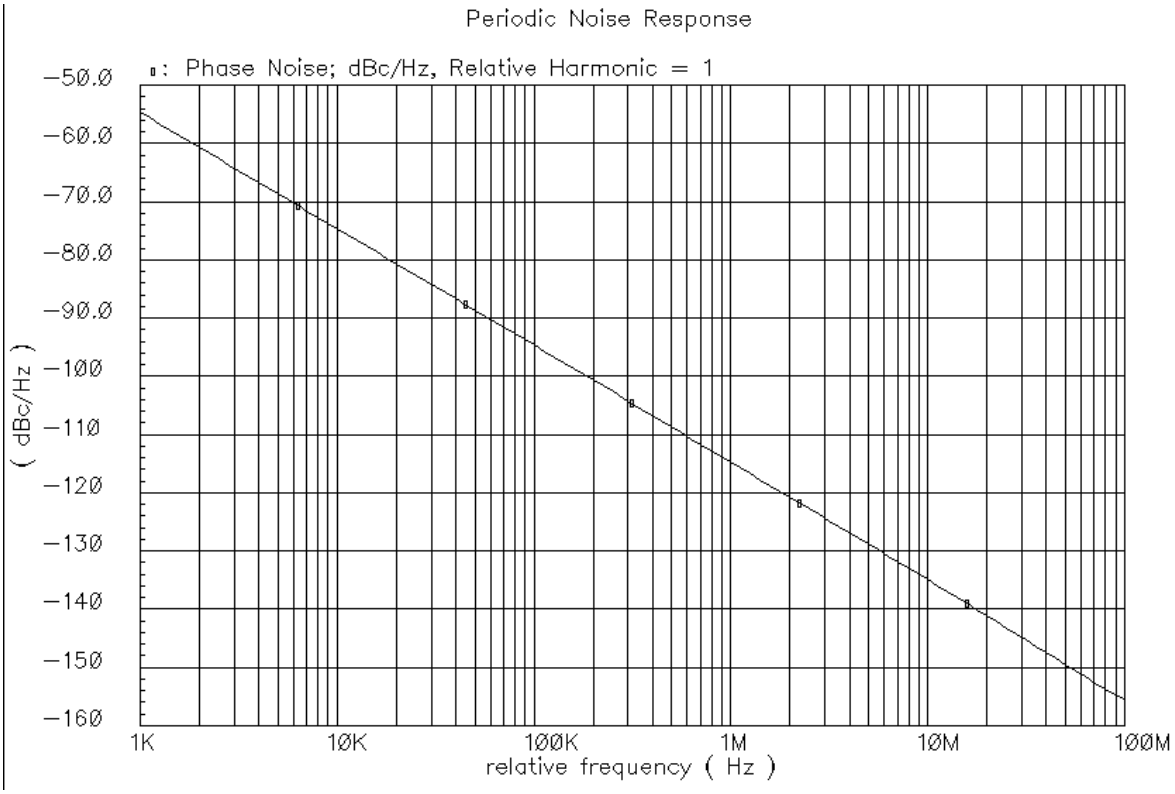

Figure 6. VCO Phase noise

4. Parametric simulation

To observe the behavior of the VCO with respect to the tuning voltage, a parametric simulation can be used. Set the control voltage as a variable and sweep in the range shown in figure 7. Keep both, the transient and the PSS simulations active with the same settings as in sections 2 and 3. The simulation results (output waveform and phase noise) will show multiple curves. To obtain parametric plots like the ones shown in figures 7 to 9, use the calculator and select the curves with the button 'family'. Then apply the corresponding command: 'frequency', 'ymax' and 'value' interpolated at 1M (for the phase noise).

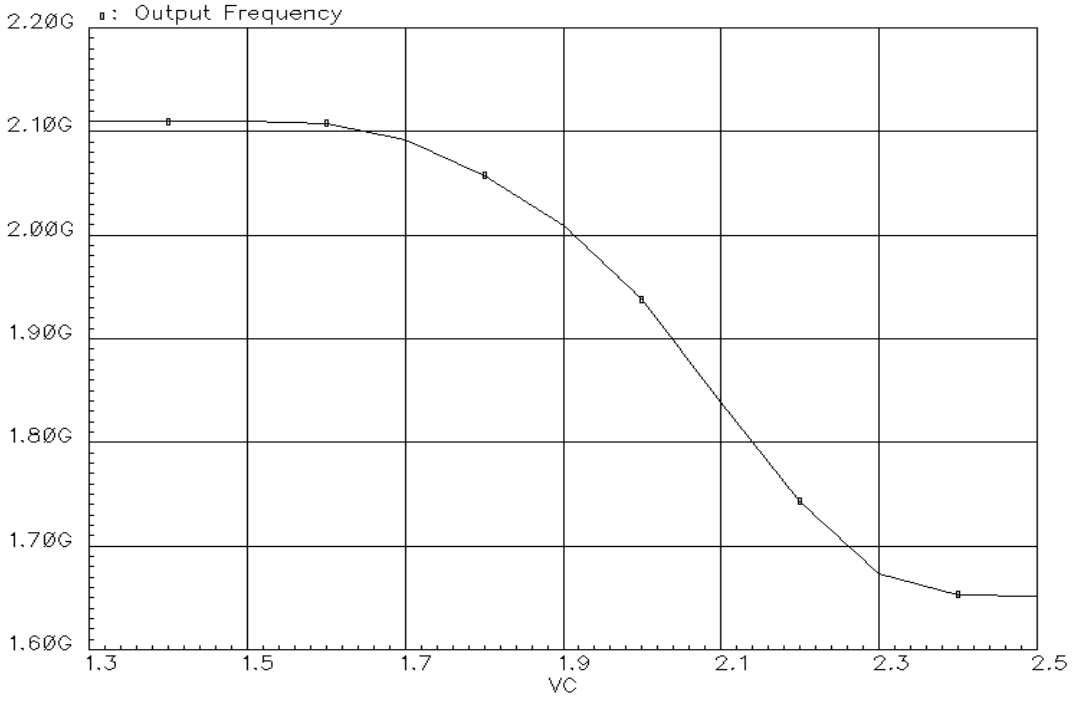

Figure 7. Frequency of oscillation Vs. VC

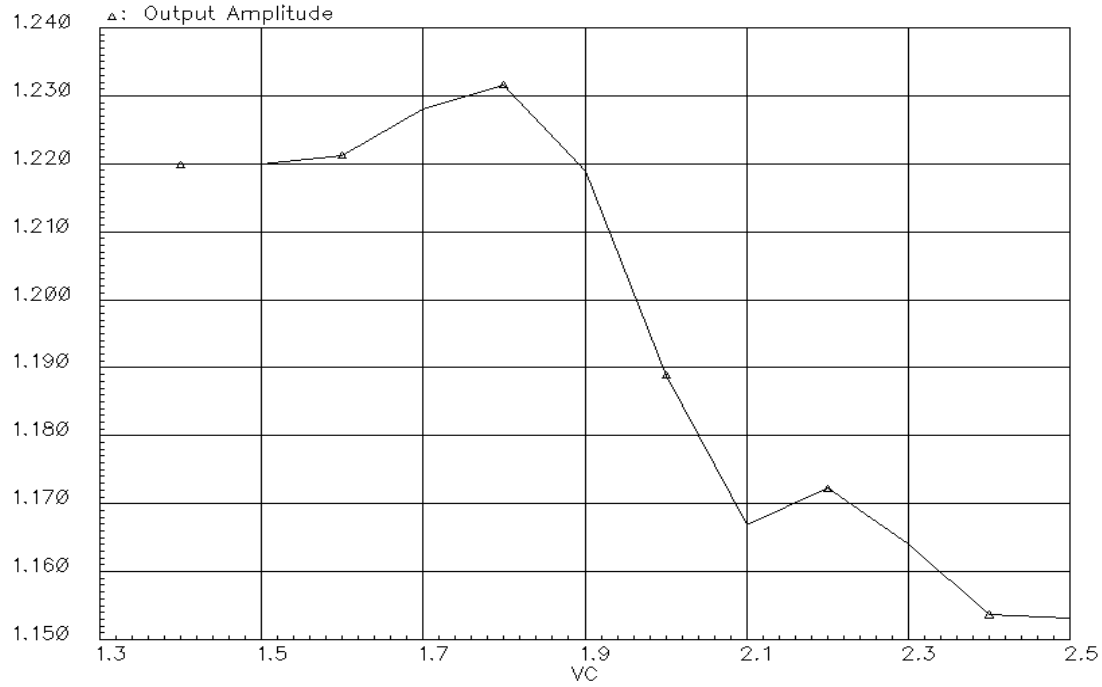

Figure 8. Output amplitude Vs. VC

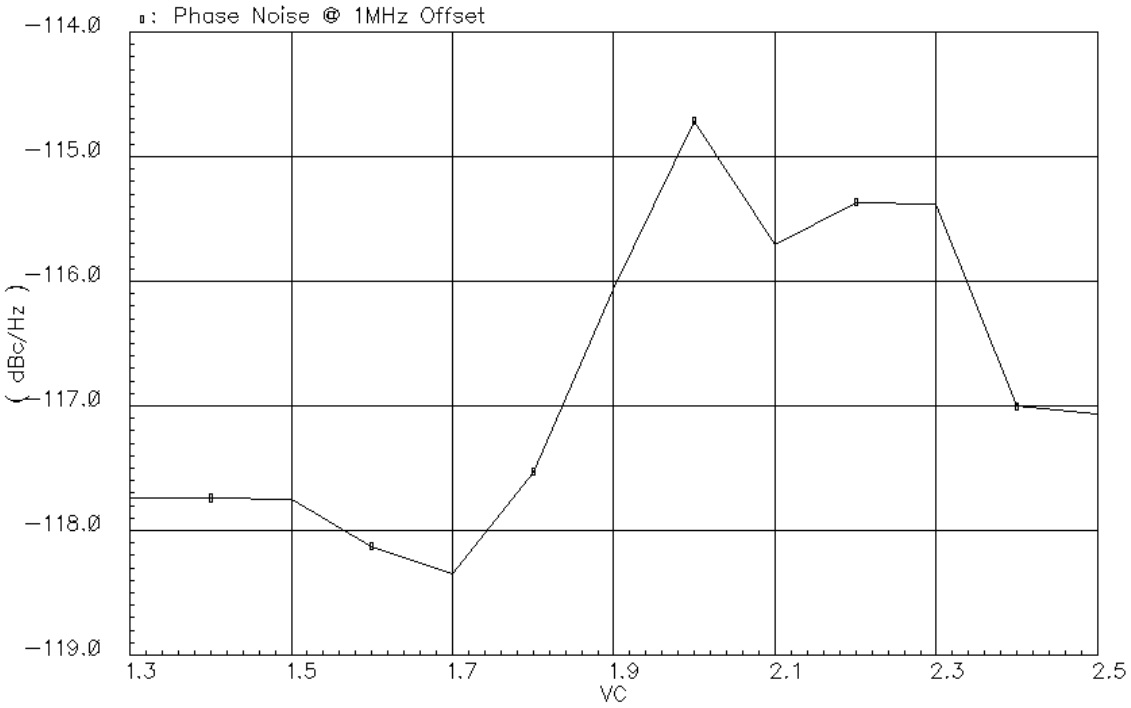

Figure 9. Phase noise Vs. VC

5. VCO analysis

5.1 Explain the role of varactors on VCO performance such as tuning range, quality factor, linearity of gain, etc.

5.2 Explain how each of the main design variables (bias current, gm of the cross-coupled transistors and Q factor of the LC tank) affect the oscillation amplitude and the phase noise. For a given bias current, what are the trade-offs involved in the choice of the W/L for the nmos transistors?

5.3 Change the Q factor of the modeled inductor from 5 to 9 and obtain parametric plots like the ones shown in section 4. How much does the phase noise change? By how much do you need to change the bias current to obtain the same phase noise as with a Q of 5?

5.4 Measure the Q of the tank. From the measured Q and the gm, and bias current obtained from a DC simulation, estimate the phase noise @1MHz offset. How does this estimation compare with the simulation results?