

:: M.C.Q. ::

1. An equivalent representation for the Boolean expression $A + A'$ is:
(a) 1
(b) 0
(c) A
(d) A'
2. A NOT gate has...
(a) Two inputs and one output
(b) One input and one output
(c) One input and two outputs
(d) None of above
3. A XNOR gate has inputs A and B and output Y. Then the output equation is:
(a) $Y = A + B$
(b) $Y = AB + A'B$
(c) $Y = A'B' + AB$
(d) $Y = A'B + AB'$
4. Which is correct?
(a) $A \cdot 1 = A$
(b) $A \cdot A = 0$
(c) $A + A = A$
(d) $A' \cdot A' = 0$
5. Demorgan's theorem is
(a) $A \cdot A' = 0$
(b) $A'' = A$
(c) $(A + B)' = A'B'$
(d) $(AB)' = A'B'$
6. An equivalent representation for the Boolean expression $A' + 1$ is:
(a) A
(b) A'
(c) 0
(d) 1
7. On a Karnaugh map, grouping the 0s produces:
(a) A "Don't Care" condition
(b) A SOP Expression
(c) A POS Expression
(d) None of the above
8. A two-input NAND gate will produce a logic 0 output when:
(a) Both of the inputs are at logic 0
(b) Either one of the inputs is at logic 0
(c) Both of the inputs are at logic 1.
(d) None of the above.
9. $A \cdot (B + C) = A \cdot B + A \cdot C$ is the expression of _____
(a) Demorgan's Law
(b) Commutative Law
(c) Distributive Law
(d) Associative Law

- 1.56**

10. What is the output state of an OR gate if the inputs are 0 and 1?
(a) 0 (b) 1
(c) 2 (d) 3

11. Which of the following gates generates the truth table shown?

x	y		F
0	0		1
0	1		0
1	0		0
1	1		1

(a) OR gate (b) NAND gate
(c) XNOR gate (d) XOR gate

12. A NOT gate has...
(a) Two inputs and one output (b) One input and one output
(c) One input and two outputs (d) none of above

13. Logic states can only be ____ or 0.
(a) 0 (b) 1
(c) 2 (d) 3

14. A NAND gate is equivalent to an AND gate plus a gate put together
(a) NOT (b) NOR
(c) XNOR (d) NAND

15. Which of these are universal gates
(a) NOR (b) NAND
(c) NOR and NAND Both (d) None

16. A EX-OR gate has inputs A and B and output Y. Then the output equation is:
(a) $Y=A+B$ (b) $Y=AB+A'B$
(c) $Y=A'B+AB'$ (d) $Y=AB'+A'B'$

17. Which is correct?
(a) $A \cdot A = 0$ (b) $A + 1 = A$
(c) $A + A = A'$ (d) $A' \cdot A' = 0$

:: EXERCISE ::

1. Differentiate combinational circuits and sequential circuits.
2. Explain Half-Adder with truth table and logic diagram.
3. Write a note on Full-Adder.
4. Construct the full adder using two half adder.
5. Explain half subtractor with truth table and circuit.
6. Explain Full subtractor with truth table and circuit.
7. Explain JK flip-flop in detail.
8. What is flip-flop? Explain the characteristics of SR flip-flop using truth table and logic diagram.
9. What is sequential circuit? Discuss the master-slave flip-flop in detail.
10. Write short notes :
 - (a) Excitation table of FFs
 - (b) D flip-flop
 - (c) T flip-flop.

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1. Half adder circuit is _____?
 - (a) Half of an AND gate
 - (b) Half of a NAND gate
 - (c) Half of NOR gate
 - (d) A circuit to add two bits together
2. If one wants to design a binary counter, preferred type of flip-flop is
 - (a) D-type
 - (b) SR-type
 - (c) Latch
 - (d) JK-type
3. A flip-flop is a binary cell capable of storing _____ bit of information.
 - (a) three
 - (b) one
 - (c) two
 - (d) four
4. Which of the following flip-flops is free from race around problem?
 - (a) T flip-flop
 - (b) SR flip-flop
 - (c) Master-Slave Flip-flop
 - (d) none
5. S-R type flip-flop can be converted into D type flip-flop if S is connected to R through
 - (a) OR Gate
 - (b) Inverter
 - (c) AND Gate
 - (d) Full Adder

6. A particular Full Adder has
(a) 3 inputs and 2 output
(c) 2 inputs and 3 output
(b) 3 inputs and 3 output
(d) 2 inputs and 2 output
7. If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be
(a) Set
(c) Indeterminate
(b) Reset
(d) Complement
8. Which of the following is the Universal Flip-flop?
(a) SR Flip-flop
(c) Master slave Flip-flop
(b) JK Flip-flop
(d) D Flip-flop
9. How is the JK Flip-flop made to toggle?
(a) $J=0, K=0$
(c) $J=1, K=1$
(b) $J=1, K=0$
(d) $J=0, K=1$
10. Full adder is constructed by using
(a) Two OR gate & one HA
(c) One HA & two OR gate.
(b) Two Half Adder & one OR gate.
(d) One OR gate & one HA
11. A D flip-flop can be made from a
(a) JK flip-flop and an inverter
(c) RS flip-flop and an inverter
(b) RS flip-flop
(d) both (a) and (b).
12. How is a J-K flip-flop made to toggle?
(a) $J = 0, K = 0$
(c) $J = 0, K = 1$
(b) $J = 1, K = 0$
(d) $J = 1, K = 1$
13. A J-K flip-flop is in a "no change" condition when _____.
(a) $J = 1, K = 1$
(c) $J = 0, K = 1$
(b) $J = 1, K = 0$
(d) $J = 0, K = 0$
14. A set of flip flops integrated together is called _____.
(a) Counter
(c) Register
(b) Adder
(d) None of the above
15. Half-Adder Logic circuit contains ____ XOR Gates.
(a) 1
(c) 4
(b) 2
(d) 6

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- 1 Which of the following is not major part of CPU
(a) Register (b) C.U.
(c) ALU (d) IO

2 _____ is multi purpose register.
(a) AC (b) PC
(c) SP (d) DR

3 Stack works on _____ algorithm.
(a) FIFO (b) LIFO
(c) Both (c) None

4 Which of the following stack.
(a) PUSH (b) POP
(c) Both (d) None

5 In memory stack pointer is _____ at the time
(a) Increment (b) Decrement
(c) Divide (d) None

6 Polish notation of $A + (B * C)$ is
(a) ABC*+ (b) AB+C*
(c) AB*+C (d) AB+*C

7 Polish notation of $A * B + C * D + E * F$ is
(a) AB*CD*EF*++ (b) ABCDE
(c) ABCD*EF**++ (d) AB+CD-

8 Reverse polish notation is useful for
(a) Evaluation of Arithmetic Expression
(b) Evaluation of tree
(c) Evaluation of stack
(d) Evaluation of queue

9 Which of the following is not type of interrupt ?
(a) External (b) Internal
(c) Software (d) None

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- 1 Interface unit provide interface between _____ and peripheral device.
- Processor bus
 - CPU
 - Printer
 - Monitor
- 2 I/O Bus consist of
- Data Line
 - Address Line
 - Control Line
 - All
- 3 There are _____ types of command there interface may received
- 2
 - 3
 - 5
- 4 Data transfer to and from peripherals.
- Direct Memory Access
 - Programmed I/O
 - Interrupt initiated I/O
 - All of above
- 5 DMA stand for
- Dynamic Memory Address
 - Dynamic Memory Access
 - Direct Memory Access
 - Direct Memory Address
- 6 During the DMA transfer
- Ideal
 - Busy
 - Waiting
 - None
- 7 BR stands for
- Bud Rate
 - Bus Request
 - Bit Rate
 - Bus Rate
- 8 BG stand for
- Bus Grant
 - Bit Given
 - Bit Grant
 - None
- 9 DMA control bus _____ register
- 2
 - 3
 - 4
 - 5
- 10 Which of the following is DMA Register
- Address Register
 - Word Count Register
 - Control Register
 - All of above
- 11 DMA is useful for _____ the display in interactive display.
- Adding
 - Updating
 - Deleting
 - None
- 12 In IOP computer is divide into _____ module
- 2
 - 3
 - 4
 - 5
- 13 IOP can fetch and execute its own instruction that is not possible in _____
- DMA controller
 - I/O Device
 - CPU
 - None
- 14 In most of computer CPU is _____ and IOP is _____
- Master, Slave
 - Slave, master
 - Primary, Secondary
 - Secondary, Primary