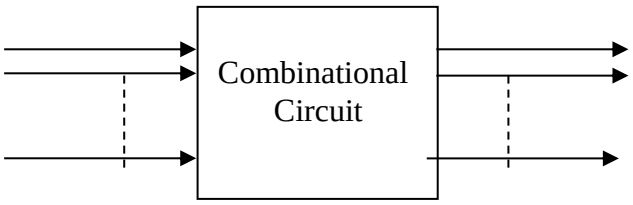
❖ COMBINATIONAL CIRCUIT:

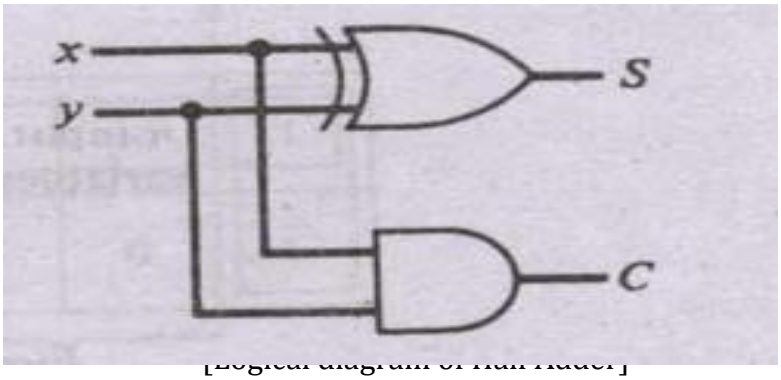
A combinational circuit is a connected arrangement of logic gates with set of inputs and outputs.
The following figure shows the block diagram of combinational circuit. it is consists of n inputs and m outputs. there is an interconnection of logical gates between inputs and outputs.



[Block diagram of a combinational circuit]

❖ HALF ADDER:-

Combinational circuit that performs the arithmetic addition of two bits is called half-adder. This circuit needs two binary input variables X and Y and two output variables S (sum) and C (carry). The input variables of a half-adder are called the **augends** and the **addend**. The output variables of a half-adder are called the sum and the carry.



[Logical diagram of Half Adder]

TRUTH TABLE FOR HALF ADDER

INPUTS		OUTPUTS	
X	**Y**	**S (Sum)**	**C (Carry)**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

As shown in truth table, we have two inputs variables X & Y, and two output variables S (Sum) And C(Cary). We can see that when both inputs are high, then the output generates carry-1. In remaining cases, the carry is not generated. S output represents the least significant bit of sum.
The Boolean functions for two outputs can be obtained directly from the truth table as follow:

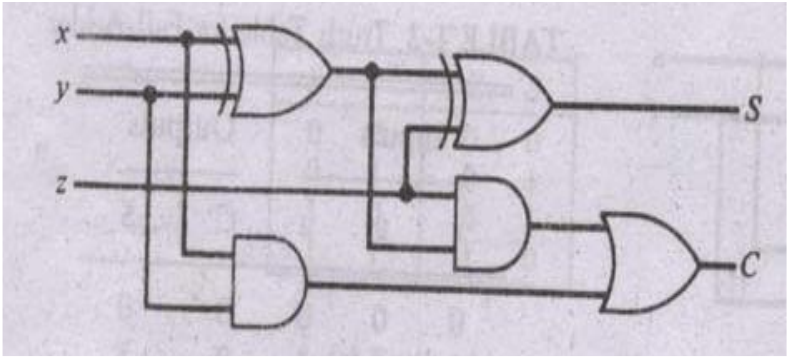
$S = X'Y + XY' = X \oplus Y$ (Ex-OR gate)
$C = XY$ (AND gate)

❖ FULL ADDER:-

A full adder is a combinational circuit that performs the arithmetic sum of three input bits (binary digits). It consists of three inputs (i.e. X,Y,Z) and two outputs S (sum) and C (carry).

A full adder is consists of two half adders. This is because when we want to add two binary numbers, each having two or more bits, the LSB(least significant bits) can be added by using half adder.

The following figure shows the three input variables, denoted by X, Y and Z, represent three significant bits to be added.



[Logical diagram of Full Adder]

TRUTH TABLE FOR FULL ADDER

INPUTS			OUTPUTS	
X	**Y**	**Z**	**S**	**C(Carry)**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The above truth table shows that the values of the output variables are determined from the arithmetic sum of the input bits. When all the inputs are 0, the output is 0. The output of S is 1 when odd numbers of inputs are 1. Hence, output of S represents EX-OR operation. The C (Carry) output has carry-1 if two or three inputs are equal to 1.

The Boolean functions for two outputs can be obtained directly from the truth table as follow:

$S = X \oplus Y \oplus Z$

$C = Z(X \oplus Y) + XY$

❖ FLIP-FLOPS:

A Flip-flop is a binary cell capable of storing one bit of information. It has two outputs, one for the normal value and one for the complement value of the bit stored in it. Flip-flops are storage elements utilized in synchronous sequential circuits.

Synchronous sequential circuits employ signals that effect storage elements only at discrete instances of time. A timing device called a clock pulse generator that produces a periodic train of clock pulses achieves synchronization.

Values maintained in the storage elements can only change at the clock pulses. Hence, a flip-flop maintains a binary state until directed by a clock pulse to switch states. The difference in the types of flip flops is in the number of inputs and the manner in which the inputs affect the binary state.

Flip-flops can be described by a characteristic table which performs all possible inputs (just like a truth table). The characteristic table of a flip-flop describes all possible outputs (called the next state) at time Q(t+1) over all possible inputs and the present state at time Q(t).

The most common types of flip flops are:

(1) SR Flip-Flop
(2) D Flip-Flop
(3) JK Flip-Flop
(4) T Flip-Flop

(1) **SR - Flip Flop (set reset):-**

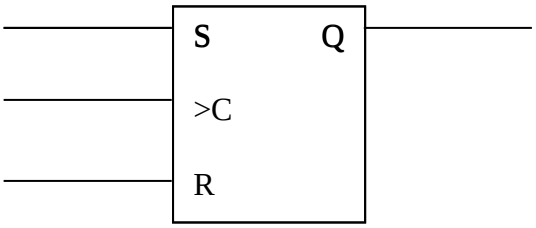
The operation of the SR flip-flop is as follow:

If there is no signal at the clock input C, the output of the circuit cannot change irrespective of the values at inputs S and R.

Only when the clock signals changes from 0 to 1 can the output be affected according to the values in inputs S and R.

If S =1 and R = 0 when C changes from 0 to 1, output Q is set to 1. If S = 0 and R =1 when C changes from 0 to 1, output Q is clear to 0.

If both S and R are 0 during the clock transition, output does not change. When both S and R are equal to 1, the output is unpredictable and may go to either 0 or 1, depending on internal timing that occur within the circuit.



[Graphical Symbol]

CHARACTERISTIC TABLE			
S	**R**	**Q(t+1)**	**Description**
0	0	Q(t)	No change
0	1	0	Clear to 0
1	0	1	Set to 1
1	1	?	Indeterminate

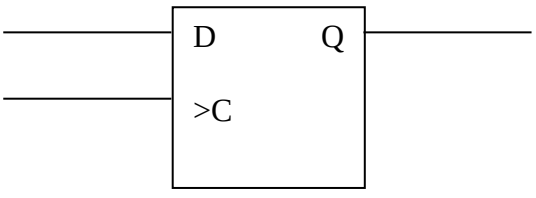
[Characteristic Table]

(2) D – Flip Flop (data):-

The D (data) Flip flop is a slight modification of the SR flip-flop. An SR flip flop is converted to a D flip flop by inserting an inverter between S and R and assigning the symbol D to the single input.

The D flip flop is operate when clock pulse changed from 0 to 1.

When D = 1, the output of flip flop will be 1. and when D = 0, the output will be 0. Hence, we can say that what ever we have input, it will be the output.



[Graphical Symbol]

CHARACTERISTIC TABLE		
D	**Q(t+1)**	**Description**
0	0	clear to 0
1	1	set to 1

[Characteristic Table]

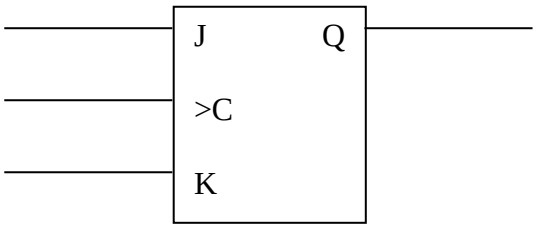
From the characteristic table, the relationship can be expressed by following equation:

Q(t+1) = D

Note that although, D flip flop has the advantage of having only one input, it has the disadvantage that its characteristic table does not have a "NO CHANGE" condition Q(t+1) = Q(t). This can be accomplished by feeding the output back into the input, so that clock pulses keep the state of the flip flop unchanged.

(3) **J-K Flip Flop (jump & kick):**

A JK flip flop is a refinement of the SR flip flop in that the indeterminate condition of the SR type is defined in the JK type. Inputs J & K behave like inputs S&R to set and clear the flip flop, respectively.



[Graphical Symbol]

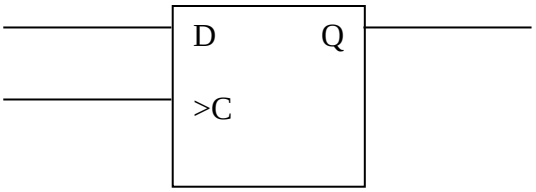
CHARACTERISTIC TABLE			
J	**K**	**Q(t+1)**	**Description**
0	0	Q(t)	No change
0	1	0	Clear to 0
1	0	1	Set to 1
1	1	Q'(t)	Complement

[Characteristic Table]

Here, J=S to set and K=R to reset. In characteristic table, when J=1 & K=0, it will set to 1. When J=0 & K=1, it will clear to 0. when J=K=0, there is "NO CHANGE". we can see that Instead of Indeterminate condition, the JK flip flop has complement condition Q(t+1)=Q'(t) when J=K=1.

(4) **T Flip Flop (Toggle):**

The T (Toggle) flip flop obtained from JK type when inputs J and K are connected to provide a single input designated by T. Hence, T Flip Flop has only two conditions.



[Graphical Symbol]

CHARACTERISTIC TABLE

T	Q(t+1)	Description
0	Q(t)	NO CHANGE
1	Q'(t)	COMPLEMENT

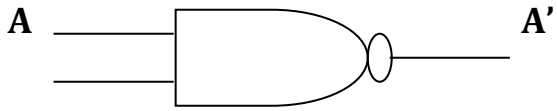
[Characteristic Table]

When T=0 (J=K=0) a clock transition does not change the state of the flip flop. When T=1(J=K=1) a clock transition complements the state of the flip flop.

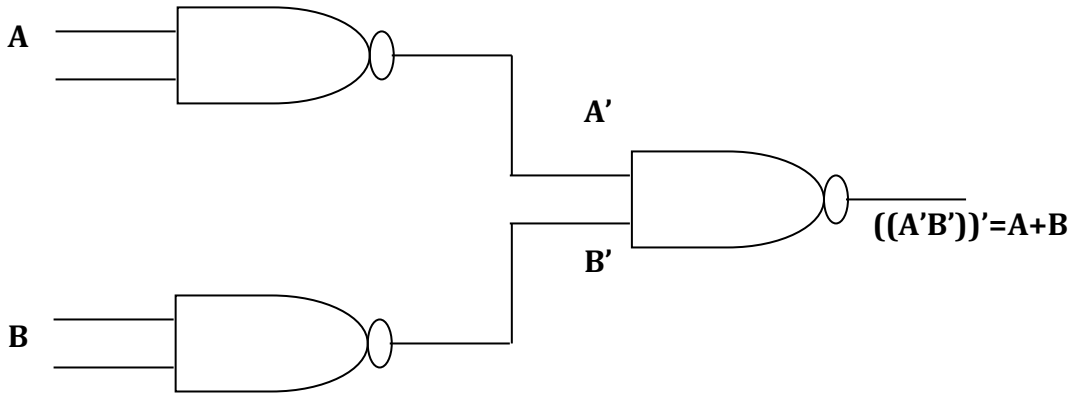
- UNIVERSALITY OF NAND & NOR GATES:
  A **universal gate** is as a gate through which we can create any basic gate.

Using NAND Gate

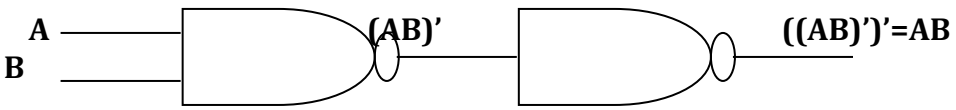
NOT:



OR:



AND:



COA MCQ CH-1

1 What is the output state of an OR gate if the inputs are 0 and 1?
a.0 **b.1**
c.3 d.2

2.What is the output state of an AND gate if the inputs are 0 and 1?
a.0 b.1
c.3 d.2

3.A NOT gate has...
a. Two inputs and one output
b. One input and one output
c. One input and two outputs
d. none of above

4.An OR gate has...
a. Two inputs and one output
b. One input and one output
c. One input and two outputs
d. none of above

5.The output of a logic gate can be one of two ____?
a. Inputs b. Gates
c.States d. none

6.The output of a ____ gate is only 1 when all of its inputs are 1
a. NOR b. XOR
c. AND d. NOT

7.A NAND gate is equivalent to an AND gate plus a .... gate put together.
a. NOR **b. NOT**
c. XOR d. none

8.Half adder circuit is _____?
a. Half of an AND gate
b. A circuit to add two bits together
c. Half of a NAND gate
d. none of above

9.Which are combinational gates
a. NAND & NOR b. NOT & AND
c. X-OR & X-NOR d. none of above

10. Which is correct:
a. A.A'=0 b. A+1=A
c. A+A=A' d. A'.A'=0

11.In a 4 input OR gate,the total number of High outputs for the 16 input states are
a.16 **b.15**

c. 13. d. none of above

12.In a 4 input AND gate,the total number of High outputs for the 16 input states are
a.16 b.8
c.4 **d.1**

13.a buffer is
a. always non-inverting b.always inverting
c. inverting or non-inverting d.none of above

14.In a 3 input NOR gate,the number of states in which output is 1 equals
a. 1 b. 2
c. 3 d. 4

15.Which of these are universal gates
a. only NOR b. only NAND
c. both NOR and NAND d. NOT,AND,OR

16. In a 3 input NAND gate,the number of gates in which output in 1equals
a.8 **b.7**
c.6 c.5

17.A.0=
a. 1 b. A
c. 0 d. A or 1

18.Demorgan's first theorem is
a. A.A'=0 b. A''=A
c. (A+B)'=A'.B' **d.** (AB)'=A'+B'

19. In which function is each term known as min term
a. SOP b. POS
c. Hybrid d. both SOP and POS

20. In which function is each term known as max term
a. SOP **b.** POS
c. Hybrid d. both SOP and Hybrid

21.The min term designation for ABCD is
a.m_0 b. m_{10}
c. m_{14} **d. m_{15}**

22.A karnaugh map with 4 variables has
a. 2 cells b. 4 cells
c. 8 cells **d.16 cells**

23.In a karnaugh map for an expression having 'don't care terms' the don't cares can be treated as
a. 0 b. 1

c. 1 or 0 d. none of above

24. A flip flop is a
a. combinational circuit **b. memory element**
c. arithmetic element d. memory or arithmetic

25. I n a D latch
a. data bit D is fed to S input and D' to R input
b. data bit D is fed to R input and D' to S input
c. data bit D is fed to both R and S inputs
d. data bit D' is not fed to any input

26. In a JK flip flop toggle means
a. set Q=1 and Q'=0
b. set Q=0 and Q'=1
c. change the output to the opposite state
d. no change in input

27. A+(B.C)=
a. A.B+C b. A.B+A.C
c. A **d.(A+B).(A+C)**

28. In which function is each term known as max term
a. SOP **b. POS**
c. Hybrid d. both SOP and Hybrid

29. A half adder can be used only for adding
a. 1s **b. 2s**
c. 4s d. 8s

30. A 3 bit binary adder should be
a. 3 full adders b. 2 full adders and 1 half adder
c. 1 full adder and 2 half adder d. 3 half adders

31. The number of inputs and outputs in a full adder are
a. 2 and 1 b. 2 and 2
c. 3 and 3 **d.** 3 and 2