CMOS DESIGN -ECL312

PROJECT REPORT

Submitted to

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Under the Guidance of

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CONTENTS

OBJECTIVE:

We have to design the CMOS layout for a 4-bit ripple counter and also Write the netlist and verify it using the NgSpice.

INTRODUCTION:

A 4-bit asynchronous UP counter with a D flip flop is shown in the above diagram. It is capable of counting numbers from 0 to 15. The clock inputs. of all flip flops are cascaded and the D input (DATA input) of each flip flop is connected to a state output of the flip flop.

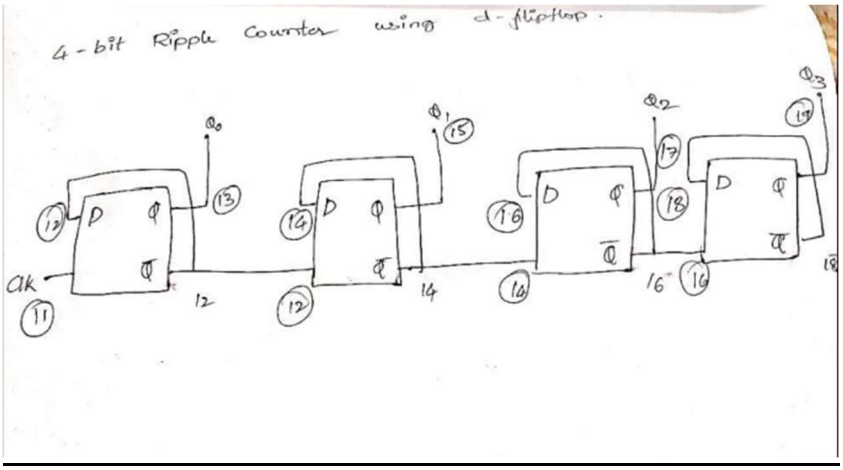
That means the flip-flops will toggle at each active edge or positive edge of the clock signals. The clock input is connected to the first flip-flop. The other flip flops in the counter receive the clock signal input from Q' output of the previous flip flop. The output of the first flip-flop will change when the positive edge on the clock signal occurs.

In the asynchronous 4-bit up counter, the flip flops are connected in toggle mode, so when the clock input is connected to the first flip flop FF0, then its output after one clock pulse will become 20.
The rising edge of the Q output of each flip-flop triggers the clock input of its next flip-flop. It triggers the next clock frequency to half of its applied input. The Q outputs of every individual flip flop (Q0, Q1, Q2, Q3) represents the count of the 4-bit UP counter.

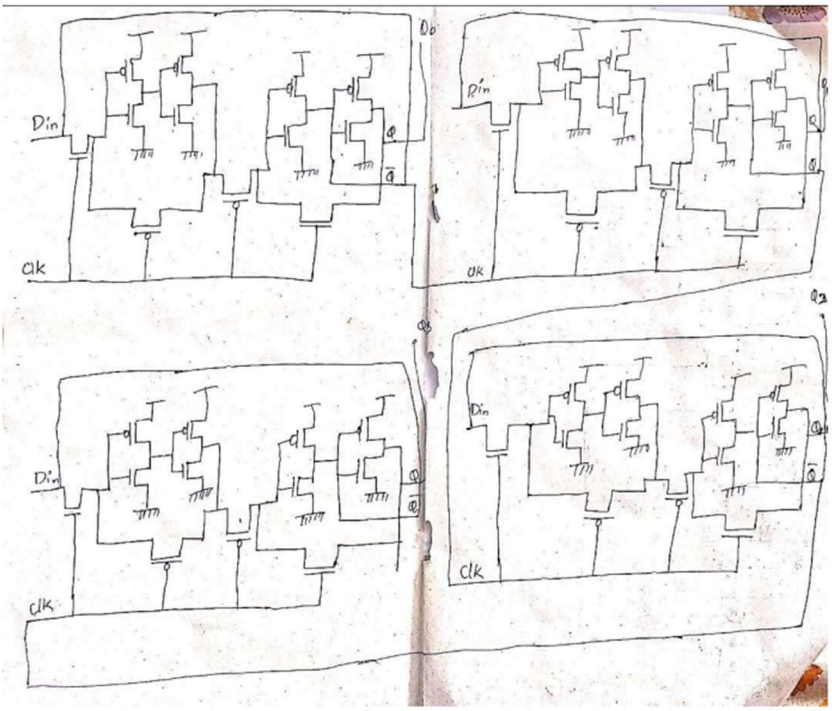
SOFTWARE USED:

Ngspice, Microwind

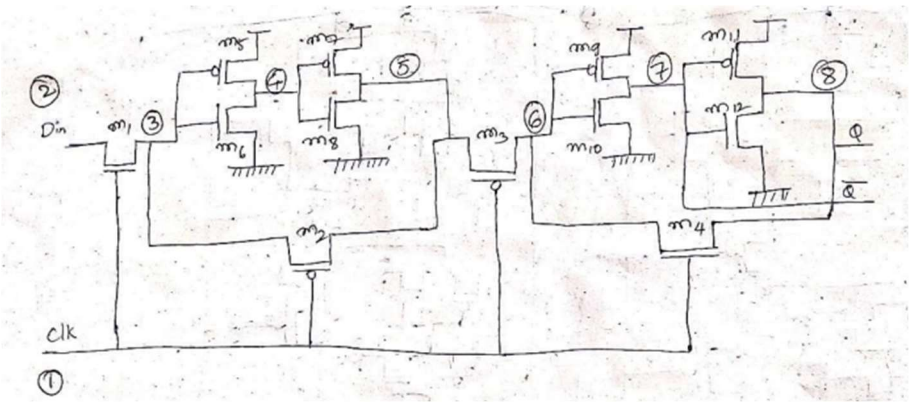
CIRCUIT DIAGRAM:



CIRCUIT DIAGRAM BY CMOS TECHNOLOGY:



SINGLE FLIP-FLOP:

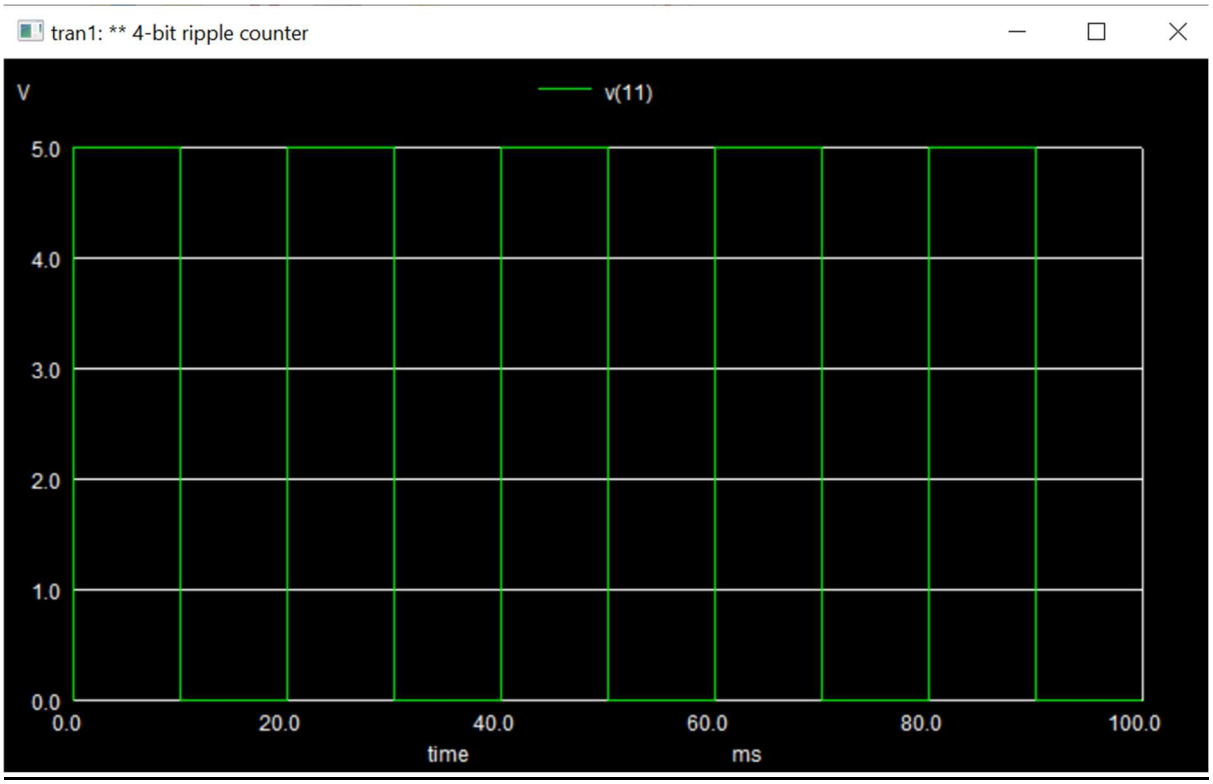


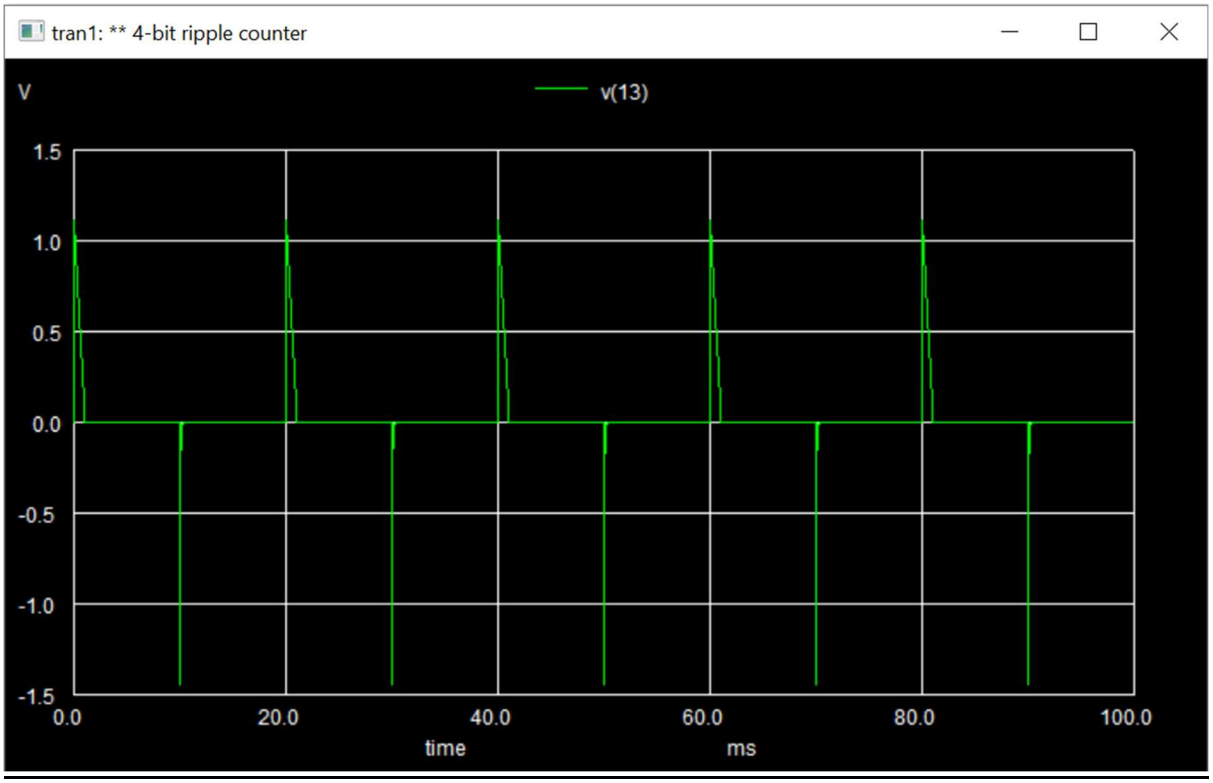
NETLIST:

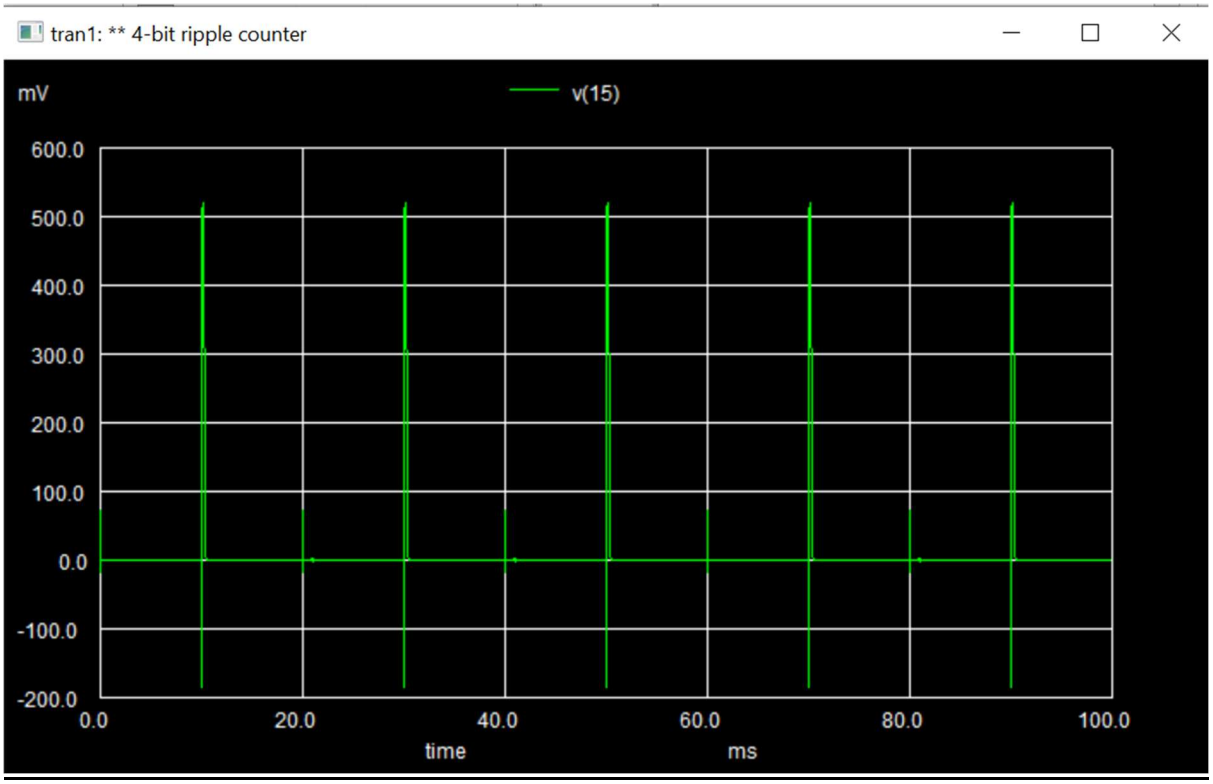
```
*** 4-bit ripple counter
.subckt inverter 1 2 3
.model pmod pmos level=54 version=4.7
.model nmod nmos level=54 version=4.7
mp 2 1 3 3 pmod w=100u l=10u
mn 2 1 0 0 nmod w=100u l=10u
.ends
.subckt dff 1 2 7 8
.model pmod pmos level=54 version=4.7
.model nmod nmos level=54 version=4.7
m1 2 1 3 3 nmod w=100u l=10u
m2 5 1 3 3 pmod w=100u l=10u
m3 6 1 5 5 pmod w=100u l=10u
m4 6 1 8 8 nmod w=100u l=10u
m5 4 3 9 9 pmod w=100u l=10u
m6 4 3 0 0 nmod w=100u l=10u
m7 5 4 9 9 pmod w=100u l=10u
m8 5 4 0 0 nmod w=100u l=10u
m9 7 6 9 9 pmod w=100u l=10u
m10 7 6 0 0 nmod w=100u l=10u
m11 8 7 9 9 pmod w=100u l=10u
m12 8 7 0 0 nmod w=100u l=10u
.ends
Vd 1 0 dc 5v
Vp 11 0 pulse(0 5 0 0 0 10m 20m)
```

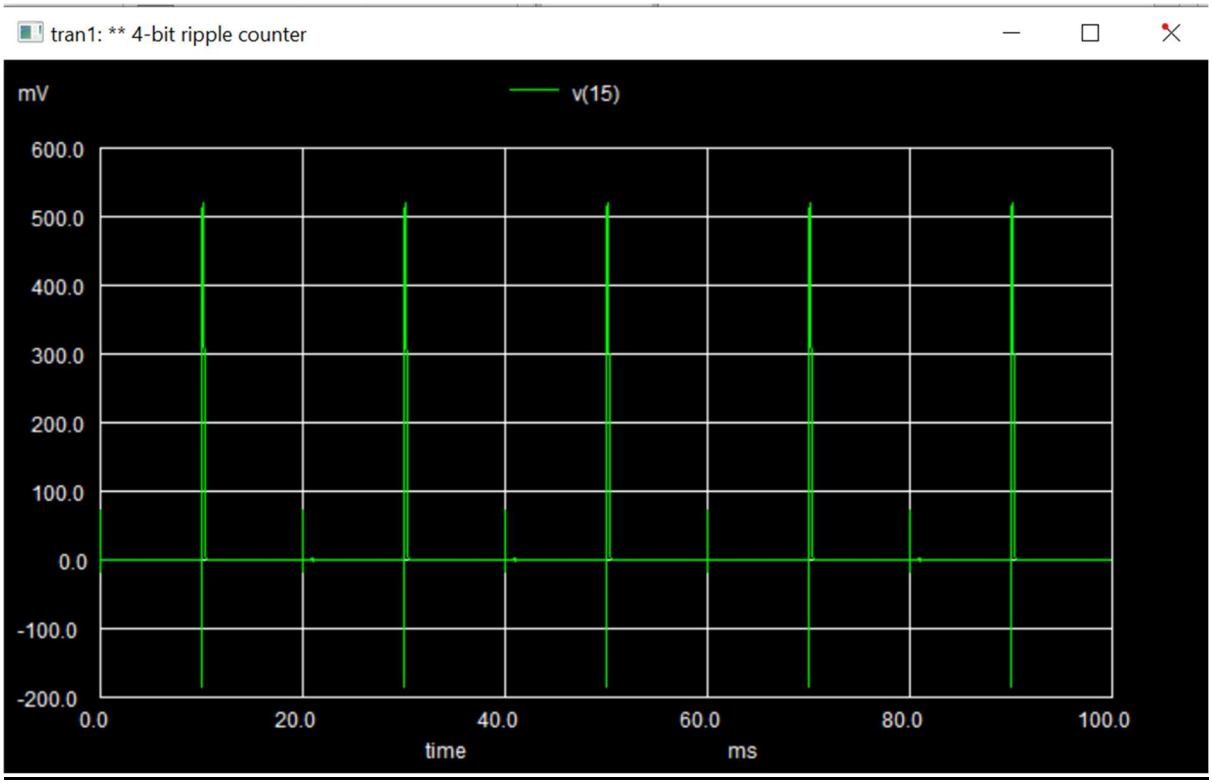
```
xd1 11 12 12 13 dff
xd2 12 14 14 15 dff
xd3 14 16 16 17 dff
xd4 16 18 18 19 dff
.tran 0.01ms 100ms
.control
run
plot V(11)
plot V(13)
plot V(15)
plot V(17)
plot V(19)
.endc
.end
```

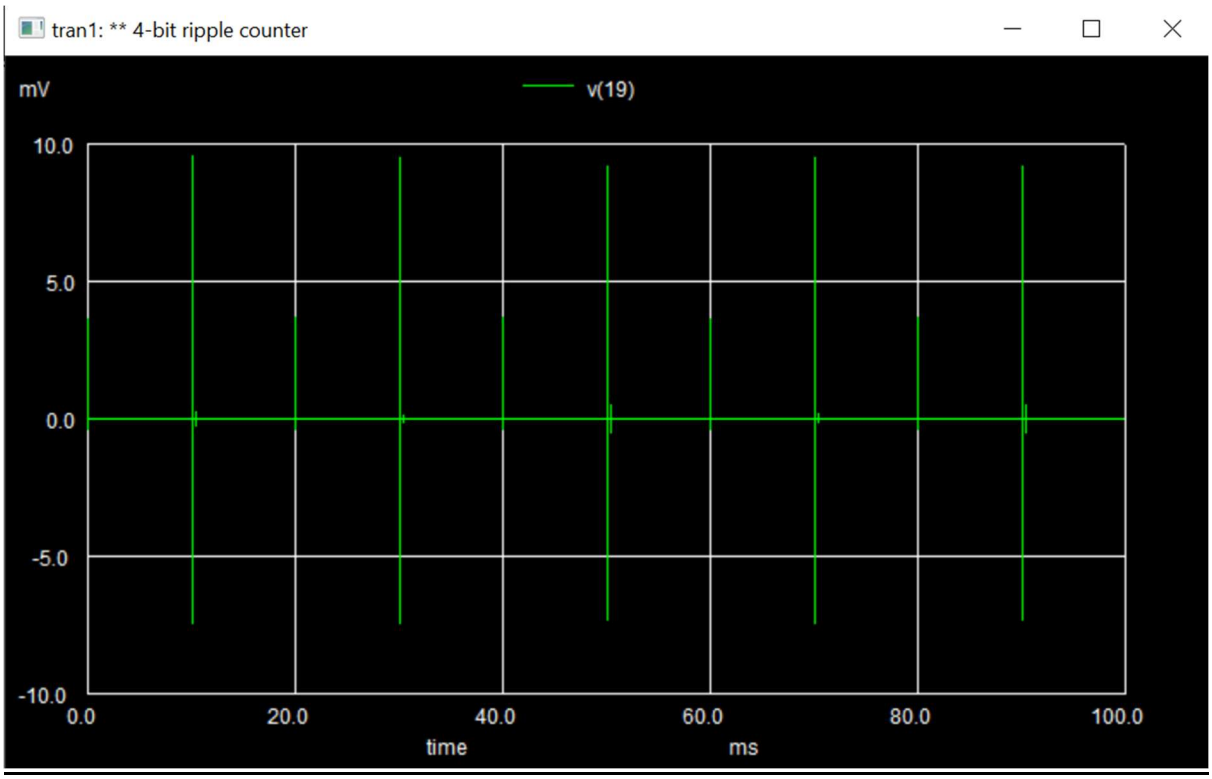
NGSPICE OUTPUT:



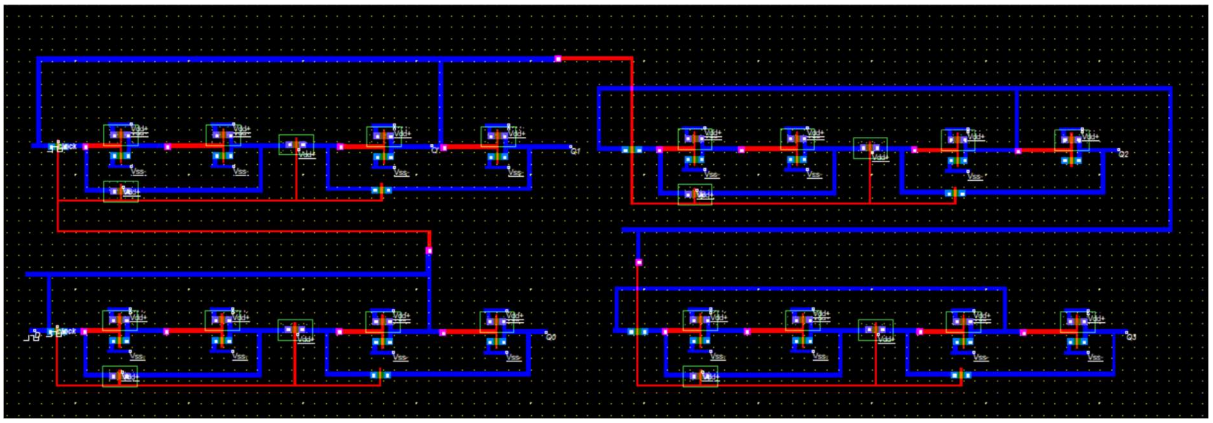

tran1: ** 4-bit ripple counter
V
v(13)
1.5
1.0
0.5
0.0
-0.5
-1.0
-1.5
0.0
20.0
40.0
60.0
80.0
100.0
time
ms


tran1: ** 4-bit ripple counter
mV
v(15)
600.0
500.0
400.0
300.0
200.0
100.0
0.0
-100.0
-200.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

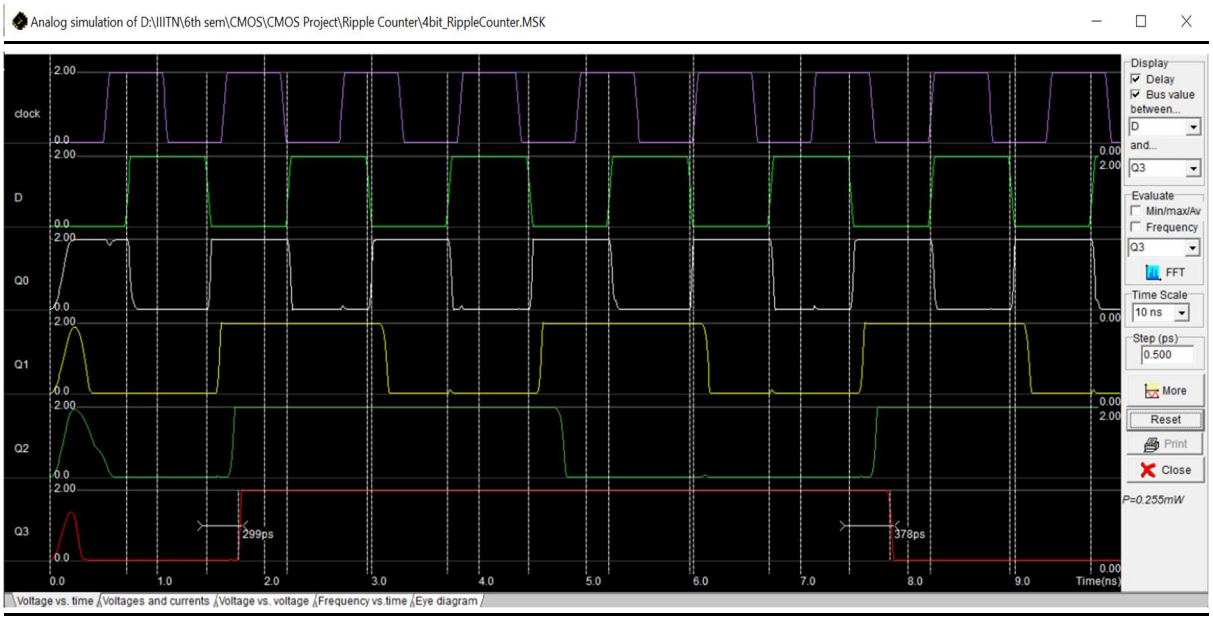

tran1: ** 4-bit ripple counter
mV
v(15)
600.0
500.0
400.0
300.0
200.0
100.0
0.0
-100.0
-200.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms


tran1: ** 4-bit ripple counter
mV
v(19)
10.0
5.0
0.0
-5.0
-10.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

CMOS LAYOUT:



OUTPUT:



CONCLUSION: I have completed the circuit design and verified it in NgSpice and also designed the layout for it in Microwind.