
| Tool Version : Vivado v.2021.2 (win64) Build 3367213 Tue Oct 19 02:48:09 MDT 2021
| Date : Fri Dec 23 14:58:33 2022
| Host : DESKTOP-KMETAO7 running 64-bit major release (build 9200)
| Command : report_utilization -file {D:/Y.Harsha vardhan ece20181/project files/project_review/utilization_report.txt} -name utilization_1
| Design : parking_system
| Device : xc7z020clg484-1
| Speed File : -1
| Design State : Routed

Utilization Design Information

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1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs	37	0	0	53200	0.07
LUT as Logic	37	0	0	53200	0.07
LUT as Memory	0	0	0	17400	0.00
Slice Registers	52	0	0	106400	0.05
Register as Flip Flop	52	0	0	106400	0.05
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-

0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
1	Yes	-	Set
36	Yes	-	Reset
0	Yes	Set	-
15	Yes	Reset	-

2. Slice Logic Distribution

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice	27	0	0	13300	0.20
SLICEL	10	0			
SLICEM	17	0			
LUT as Logic	37	0	0	53200	0.07
using O5 output only	0				
using O6 output only	18				
using O5 and O6	19				
LUT as Memory	0	0	0	17400	0.00
LUT as Distributed RAM	0	0			
LUT as Shift Register	0	0			
Slice Registers	52	0	0	106400	0.05
Register driven from within the Slice	42				
Register driven from outside the Slice	10				
LUT in front of the register is unused	10				
LUT in front of the register is used	0				
Unique Control Sets	3		0	13300	0.02

* * Note: Available Control Sets calculated as Slice * 1, Review the Control Sets Report for more informati on regarding control sets.

3. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accom modate a RAMB18E1

4. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	0	0	0	220	0.00

5. IO and GT Specific

Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB	24	0	0	200	12.00
IOB Master Pads	12				
IOB Slave Pads	11				
Bonded IPADs	0	0	0	2	0.00
Bonded IOPADs	0	0	0	130	0.00
PHY_CONTROL	0	0	0	4	0.00
PHASER_REF	0	0	0	4	0.00
OUT_FIFO	0	0	0	16	0.00
IN_FIFO	0	0	0	16	0.00
IDELAYCTRL	0	0	0	4	0.00
IBUFDS	0	0	0	192	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	0	16	0.00
PHASER_IN/PHASER_IN_PHY	0	0	0	16	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	0	200	0.00
ILOGIC	0	0	0	200	0.00
OLOGIC	0	0	0	200	0.00

6. Clocking

Site Type	Used	Fixed	Prohibited	Available	Util%
BUFGCTRL	1	0	0	32	3.13
BUFIO	0	0	0	16	0.00
MMCME2_ADV	0	0	0	4	0.00
PLLE2_ADV	0	0	0	4	0.00
BUFMRCE	0	0	0	8	0.00
BUFHCE	0	0	0	72	0.00
BUFR	0	0	0	16	0.00

7. Specific Feature

Site Type	Used	Fixed	Prohibited	Available	Util%

BSCANE2	0	0	0	4	0.00
CAPTUREE2	0	0	0	1	0.00
DNA_PORT	0	0	0	1	0.00
EFUSE_USR	0	0	0	1	0.00
FRAME_ECCE2	0	0	0	1	0.00
ICAPE2	0	0	0	2	0.00
STARTUPE2	0	0	0	1	0.00
XADC	0	0	0	1	0.00

8. Primitives

Ref Name	Used	Functional Category
FDCE	36	Flop & Latch
LUT2	35	LUT
OBUF	16	IO
FDRE	15	Flop & Latch
IBUF	8	IO
CARRY4	8	CarryLogic
LUT6	7	LUT
LUT5	5	LUT
LUT4	5	LUT
LUT3	3	LUT
LUT1	1	LUT
FDPE	1	Flop & Latch
BUFG	1	Clock

9. Black Boxes

Ref Name	Used

10. Instantiated Netlists

Ref Name	Used