Copyright 1986-2021 Xilinx, Inc. All Rights Reserved. | Tool Version : Vivado v.2021.2 (win64) Build 3367213 Tue Oct 19 02:48:09 MDT 2021 : Fri Dec 23 14:58:33 2022 Host : DESKTOP-KMETAO7 running 64-bit major release (build 9200) | Command : report_utilization -file {D:/Y.Harsha vardhan ece20181/project files/project_review/utilizati on_report.txt} -name utilization 1 | Design : parking_system Device : xc7z020clg484-1 Speed File : -1 Design State: Routed **Utilization Design Information** Table of Contents -----1. Slice Logic 1.1 Summary of Registers by Type 2. Slice Logic Distribution 3. Memory 4. DSP 5. IO and GT Specific 6. Clocking 7. Specific Feature 8. Primitives 9. Black Boxes 10. Instantiated Netlists 1. Slice Logic -----+ Site Type | Used | Fixed | Prohibited | Available | Util% | **+-----**| Slice LUTs | 37 | 0 | 0 | 53200 | 0.07 | | LUT as Logic | 37 | 0 | 0 | 53200 | 0.07 | | LUT as Memory | 0 | 0 | 0 | 17400 | 0.00 | | Slice Registers | 52 | 0 | 0 | 106400 | 0.05 | | Register as Flip Flop | 52 | 0 | 0 | 106400 | 0.05 | | Register as Latch | 0 | 0 | 0 | 106400 | 0.00 | | F7 Muxes | 0 | 0 | 0 | 26600 | 0.00 | | F8 Muxes | 0 | 0 | 0 | 13300 | 0.00 | |

1.1 Summary of Registers by Type

+-----+
| Total | Clock Enable | Synchronous | Asynchronous |
+-----+

0		_	-	Set
0		_	-	Reset
0		_	Set	-
0		_	Reset	-
0		Yes	-	-
1		Yes	-	Set
36		Yes	-	Reset
0		Yes	Set	-
15		Yes	Reset	-
+	+	+		++

2. Slice Logic Distribution

+	++++++
Site Type	Used Fixed Prohibited Available Util%
Olica	
Slice	27 0 0 13300 0.20
SLICEL	10 0
SLICEM	17 0
LUT as Logic	37 0 0 53200 0.07
using O5 output only	0
using O6 output only	18
using O5 and O6	19
LUT as Memory	0 0 0 17400 0.00
LUT as Distributed RAM	0 0
LUT as Shift Register	0 0
Slice Registers	52 0 0 106400 0.05
Register driven from within	n the Slice 42
Register driven from outsid	de the Slice 10
LUT in front of the registe	er is unused 10
LUT in front of the registe	er is used 0
Unique Control Sets	3
+	

<sup>+-----+

* *</sup> Note: Available Control Sets calculated as Slice * 1, Review the Control Sets Report for more informati on regarding control sets.

3. Memory

Site Type	+ Used Fixed F	Prohibited	l Available Uti	l%
Block RAM T RAMB36/FII RAMB18	++ ile	0 0	140 0.00 140 0.00 280 0.00	

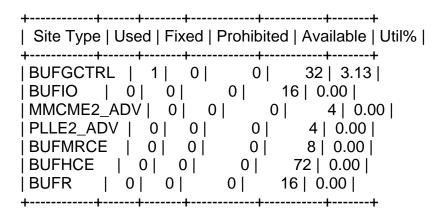
^{*} Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

Site Type	e Used	Fixed	d Prohib	+ ited Available Ut +	:il%
DSPs	0	0	0	220 0.00	

5. IO and GT Specific

Site Type Used Fixed Prohibited Available Util%
+
Bonded IOB 24 0 0 200 12.00
IOB Master Pads 12
IOB Slave Pads
Bonded IPADs
Bonded IOPADs
PHY_CONTROL
PHASER_REF
OUT_FIFO
IN_FIFO
IDELAYCTRL
IBUFDS
PHASER_IN/PHASER_IN_PHY
IDELAYE2/IDELAYE2_FINEDELAY 0 0 0 200 0.00
ILOGIC
OLOGIC
+

6. Clocking



7. Specific Feature



```
BSCANE2 | 0 | 0 |
                         0 |
                               4 | 0.00 |
CAPTUREE2 | 0 | 0 |
                                1 | 0.00 |
                          0 |
DNA_PORT | 0|
                   0 |
                          0 |
                                1 | 0.00 |
EFUSE_USR | 0 | 0 |
                                 1 | 0.00 |
                          0 |
FRAME_ECCE2 | 0 | 0 |
                          0 |
                                 1 | 0.00 |
                              2 | 0.00 |
ICAPE2
        | 0 | 0 |
STARTUPE2 | 0 | 0 |
                          0 |
                                 1 | 0.00 |
                              1 | 0.00 |
IXADC
       | 0| 0|
                       0 |
```

8. Primitives

```
+----+
| Ref Name | Used | Functional Category |
I FDCE
        | 36 |
                 Flop & Latch |
LUT2
       | 35 |
                     LUT |
                      10 |
OBUF
       | 16|
       | 15|
FDRE
                  Flop & Latch |
      | 8|
IBUF
                     10 |
CARRY4 | 8|
                   CarryLogic |
          7 |
LUT6
                     LUT |
LUT5
          5 |
                     LUT |
LUT4
          5 |
                     LUT |
LUT3
          3 |
                     LUT |
LUT1
          1 |
                     LUT |
FDPE
          1 |
                 Flop & Latch |
                     Clock |
BUFG
         1 |
```

9. Black Boxes

+----+ | Ref Name | Used | +-----

10. Instantiated Netlists

+-----+ | Ref Name | Used | +-----