

DC Amplifier

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A DC amplifier has an open loop gain of 1000 and two poles, a dominant one at 1kHz and a high frequency one whose location can be controlled. It is required to connect this amplifier in a negative feedback loop that provides a DC closed loop gain of 10 and a maximally flat response.

1. Find the required value of H .

Solution: Table ?? summarises the given information. The open loop gain can be expressed as

$$G(s) = \frac{G_0}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)} \quad (1.1)$$

$$\Rightarrow G(0) = G_0 \quad (1.2)$$

The closed loop gain

$$T(s) = \frac{G(s)}{1 + G(s)H} \quad (1.3)$$

$$\Rightarrow T(0) = \frac{G_0}{1 + G_0H} \quad (1.4)$$

Substituting from Table ??,

$$\frac{1000}{1 + 1000H} = 10 \quad (1.5)$$

$$\Rightarrow H = 0.099 \quad (1.6)$$

| Parameter | Value |
|---------------------|--------|
| dc open loop gain | 1000 |
| dominant pole | 1000Hz |
| insignificant pole | $-p_2$ |
| dc closed loop gain | 10 |

TABLE 1: 1

$$G_0 = 1000 \quad (1.7)$$

$$\text{Therefore, } G(s) = \frac{1000}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)} \quad (1.8)$$

2. Find p_2 .

Solution: From (??) and (??),

$$T(s) = \frac{p_1 p_2 G_0}{s^2 + (p_1 + p_2)s + (HG_0 + 1)p_1 p_2} \quad (2.1)$$

$$= \frac{K\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (2.2)$$

$$\omega_n = \sqrt{(HG_0 + 1)p_1 p_2}$$

$$\Rightarrow \zeta = \frac{p_1 + p_2}{2\sqrt{(HG_0 + 1)p_1 p_2}} \quad (2.3)$$

using the standard formulation for a second order system. Also, for maximally flat response, the quality factor

$$Q = \frac{1}{2\zeta} = \frac{1}{\sqrt{2}} \quad (2.4)$$

$$\Rightarrow \zeta = \frac{1}{\sqrt{2}} \quad (2.5)$$

$$\Rightarrow \frac{p_1 + p_2}{2\sqrt{(HG_0 + 1)p_1 p_2}} = \frac{1}{\sqrt{2}} \quad (2.6)$$

$$\Rightarrow \sqrt{\frac{p_1}{p_2}} + \sqrt{\frac{p_2}{p_1}} = \sqrt{2(HG_0 + 1)} \quad (2.7)$$

The above equation is of the form

$$x + \frac{1}{x} = a \quad (2.8)$$

$$\Rightarrow x = \frac{a \pm \sqrt{a^2 - 4}}{2} \quad (2.9)$$

where

$$x = \sqrt{\frac{p_2}{p_1}} \quad (2.10)$$

$$a = \sqrt{2(HG_0 + 1)}, \quad (2.11)$$

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Thus, from (??), (??) and (??),

$$p_2 = p_1 \left[\frac{\sqrt{2(HG_0 + 1)} \pm \sqrt{2(HG_0 + 1) - 4}}{2} \right]^2 \quad (2.12)$$

From the following code,

```
codes/ee18btech11005/ee18btech11005_1.py
```

$$p_2 = 1244038.9567529503$$

and 31.734068607786863 (2.13)

3. Draw the equivalent circuit system diagram.

Solution: The equivalent circuit system is shown in the figure.??

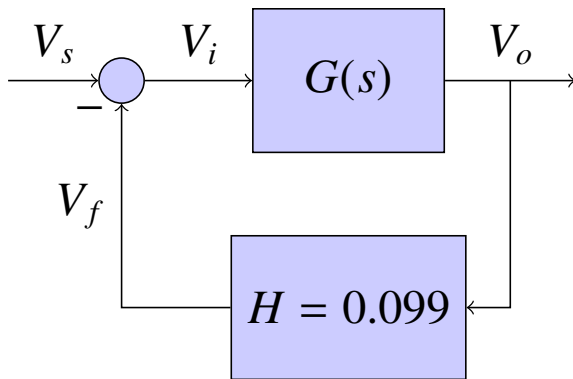


Fig. 3: 1

4. Obtain $G(s)$ and $T(s)$

Solution: Substituting the value of p_2 in (??) and (??),

$$G(s) = \frac{1000}{(1 + \frac{s}{2\pi 10^3})(1 + \frac{s}{1.244 \times 10^6})} \quad (4.1)$$

$$T(s) = \frac{10}{0.128 \times 10^{-11} s^2 + 1.599 \times 10^{-6} s + 1} \quad (4.2)$$

5. Verify from the Bode plot of above closed loop transfer function that it has maximally flat response.

Solution: The following code generates the bode plot of the transfer function in Fig. ??.

```
codes/ee18btech11005/ee18btech11005_2.py
```

6. Find the step response of $T(s)$

Solution: The following code generates the desired response of in Fig. ??.

```
codes/ee18btech11005/ee18btech11005_3.py
```

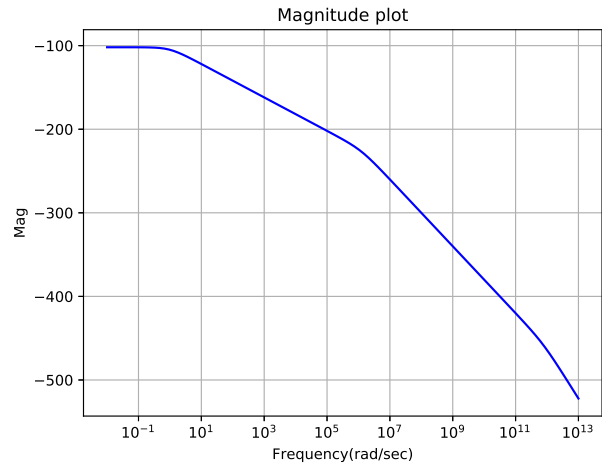


Fig. 5

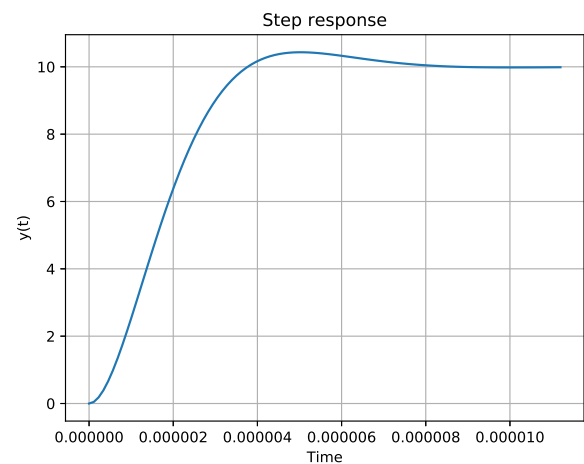


Fig. 6

7. Design a circuit that represents the above transfer function.

Solution: The circuit can be designed using an operational amplifiers having negative feedback. Consider the circuit shown in figure.??:1. Assume the gain of all the amplifiers are large. And assume no zero state response. Take the parameters in s-domain.

For the first amplifier., Applying KCL at

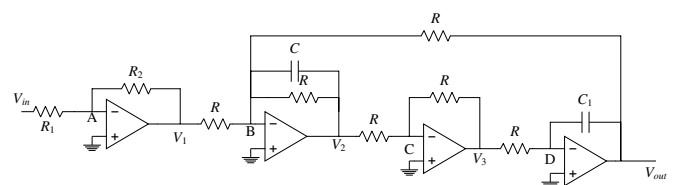


Fig. 7: 1

node A., Since, the opamp has large gain, potential at node A is assumed to be zero due to virtual short at node A.

$$\frac{0 - V_{in}(s)}{R_1} + \frac{0 - V_1(s)}{R_2} = 0 \quad (7.1)$$

$$\frac{V_{in}(s)}{R_1} = \frac{V_1(s)}{R_2} \quad (7.2)$$

$$\Rightarrow V_{in} = -\frac{V_1(s)R_1}{R_2} \quad (7.3)$$

For the second amplifier., Applying KCL at node B., Similarly potential at node B is zero.

$$\frac{-V_1(s)}{R} + \frac{-V_2(s)}{R} - sCV_2(s) + \frac{-V_{out}(s)}{R} = 0 \quad (7.4)$$

$$\frac{-V_1(s)}{R} + \frac{-V_2(s)}{R} - sCV_2(s) = \frac{V_{out}(s)}{R} \quad (7.5)$$

$$\frac{-V_1(s)}{R} = V_2(s) \left[sC + \frac{1}{R} \right] + \frac{V_{out}(s)}{R} \quad (7.6)$$

For the third amplifier., Potential at node C is zero(Due to high gain of amplifier).Applying KCL at node C.

$$\frac{-V_2(s)}{R} + \frac{-V_3(s)}{R} = 0 \quad (7.7)$$

$$\Rightarrow V_2(s) = -V_3(s) \quad (7.8)$$

For the Fourth amplifier., Potential at node D is zero.Applying KCL at node D.

$$\frac{-V_3(s)}{R} + sC_1(-V_{out}(s)) = 0 \quad (7.9)$$

$$V_3(s) = -sC_1RV_{out}(s) \quad (7.10)$$

From equation.?? and equation. ??...,

$$V_2(s) = sC_1RV_{out}(s) \quad (7.11)$$

Substituting the equation.?? and equation.??,

$$\frac{-V_1(s)}{R} = (s^2C_1CR + sC_1)V_{out}(s) + \frac{V_{out}(s)}{R} \quad (7.12)$$

$$V_1(s) = -(s^2C_1CR^2 + sC_1R + 1)V_{out}(s) \quad (7.13)$$

from equation.?? and equation.??.

$$V_1(s) = \frac{R_1}{R_2}(s^2C_1CR^2 + sC_1R + 1)V_{out}(s) \quad (7.14)$$

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{R_2}{R_1(s^2C_1CR^2 + sC_1R + 1)} \quad (7.15)$$

Comparing equation.?? and equation.??

$$\frac{R_2}{R_1} = 10 \quad (7.16)$$

$$C_1CR^2 = 0.128 \times 10^{-11} \quad (7.17)$$

$$C_1R = 1.599 \times 10^{-6} F \quad (7.18)$$

$$\text{Let., } R = 1000 \Omega \quad (7.19)$$

$$\Rightarrow C_1 = 1.599 \times 10^{-9} \quad (7.20)$$

$$\text{and., } C_1CR^2 = 0.128 \times 10^{-11} \quad (7.21)$$

$$\Rightarrow C = 0.8005 \times 10^{-9} F \quad (7.22)$$

$$\text{Let., } R_1 = 100 \Omega \quad (7.23)$$

$$\Rightarrow R_2 = 1000 \Omega \quad (7.24)$$

From Table.?:1. The Final circuit is shown

| Parameter | Value |
|-----------|---------------|
| R_1 | 100 Ω |
| R_2 | 1000 Ω |
| R | 1000 Ω |
| C | 0.8005 nF |
| C_1 | 1.599 nF |

TABLE 7: 1

in figure.??

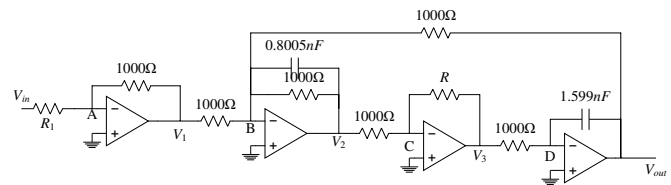


Fig. 7: 1

8. Draw the equivalent block diagram of the above circuit.

Solution: The equivalent block diagram is shown in the Fig.?.?.The block diagram can be computed similarly from the above circuit diagram. Where each opamp is reduced into a block. And the last three blocks having a negative feedback.

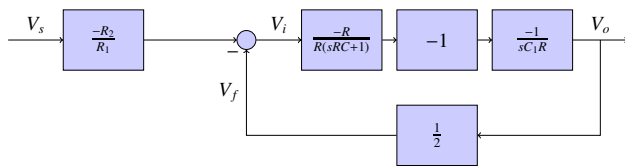


Fig. 8

9. Verify the closed loop DC gain using NGSPICE simulator.

Solution: The following README file gives the procedure to be followed.

```
codes/ee18btech11005/spice/README
```

From equation.???. The DC closed loop gain is 10.

The following netlist file, gives the DC gain of the closed loop function.

```
codes/ee18btech11005/spice/gvv_ngspice.net
```

We can observe from simulation that the value of DC closed loop gain is 9.997.

Error analysis:-

ERROR in DC GAIN = $10 - 9.993 = 0.007$
Thus, the predicted value in ngspice is almost accurate. Therefore, the value is verified using ngspice.

10. Verify the step response of the output from ngspice simulation.

Solution: The following netlist file does the transient analysis and store the Vout values with respect to time in a dat file.

```
codes/ee18btech11005/spice/gvv_ngspice2.net
```

Following python code is to plot the step response.

```
codes/ee18btech11005/spice/ee18btech11005_spice.py
```

The step response obtained is shown in the figure.???.The graph has steady state value equal to 10.

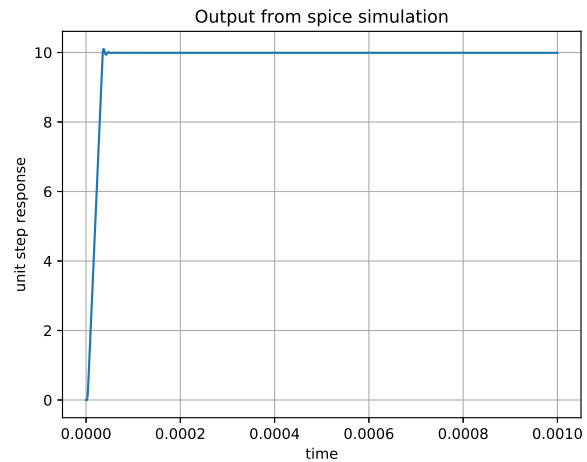


Fig. 10