Design and Development of STM32-Based CubeSat OBC

ABSTRACT:

This project presents the design and dvelopment of a Cubesat-Level OBC prototype based on the STM32 MCU.

The objective of this work is to design a compact, reliable and power-efficient Embedded Hardware system capable of managing the Power Regultion , Sensor Telementry acquisition, data logging, and subsystem monitoring.

The complete system was designed using KiCad from Schematic to PCB Layout and 3D verification.

The design consists of a Li-ion battery charging stage using a TP4056 linear charger, followed by a Boost conv. For 5V rail generation and used an LDO regulatr for stable 3V3 logic supply.STM32 MCU serves as the central unit, interfacing , interfacing with peripheral devices including SPI Flash Memory, SD card storage, an Inertial Measurement Unit(IMU), Current Sensor, Thermistor-based temparature Monitoring, and an ADC-based battery Voltage measurement. A SWD interface is incoroporated for debugging and Frimware programming, while status LEDs provide visual system diagnostics.

The design Workflow followed a schematic apprach: requirement definition, block level schematic design, component selection based on datasheet analysis, footprint assignment, PCB planning, controlled routing, ground plane implementation, DRC verification.

The final result is a 2-layer PCB implementation demonstrating a structured power distribution strattegy, modular subsytem integration , and adherence to embedded hardware design best practices.

SYSTEM ARCHITECTURE:

Overall Architecture Overview-

The purposed CubeSat On-Board Computer (OBC) is designed as a modular embedded system integrating Power regulation, Data acquisition, Storage and Subsystem monitoring within a compact 2-layer PCB architecture. The system architecture is derived directly from the schematic design and is organised into functional blocks to ensure clarity,maintainability and electrical reliability.

The architecture is divided into the fllowing subsystems -

1. Power Input and Charging block
2. Battery and Energy Storage block
3. Voltage Regulation Block

4. Microcontroller Core block
5. Memory and Data storage block
6. Sensor Telemetry block
7. ADC & Voltage monitoring block
8. Debug & Programming Interface
9. Grounding and Power distribution network

I. Power Input and Charging block

The power input stage is implemented using a USB-C interface configured for 5V default operation. This stage provides external power for battery charging and initial system startup.

The charging functionality is implemented using the TP4056 linear Li-ion battery charger. The TP4056 operates using a constant-current/constant-voltage(CC/CV) charging algorithm, terminating charge at ~4.2V . The exposed thermal pad is connected to ground with thermal vias to improve heat dissipation, as observed in the schematic and PCB layout.

This block ensures:

- Controlled charging current
- Thermal regultion
- Safe battery voltage limiting
- Stable transition between external power and battery operation

The Schematic flow shows a direct path from USB_5V to the TP4056 input, followed by the battery output connection to the system power rail.

II. Battery & Energy Stroage Block

The Li-ion battery serves as the primary energy storage elemnt. It supplies the system during standalone operation and acts as an energy buffer during load transients.

A bulk capacitor is placed across the battery rail to stabilize voltage flucuations . The battery output feeds the boost converter input stage, forming the next level of power conditioning.

Trace width considerations and placement strategy in the schematic ensure that high-current battery paths remain short and low impedance.

III. Voltage Regulation Block

The regulation stage consists of two sub-blocks:

- **Boost Converter:** A DC-DC boost converter is implemented to step-up the battery voltage (3-4.2V) to a regulated 5V rail. The boost topology includes

- Switching controller
- Inductor
- Schottky diode

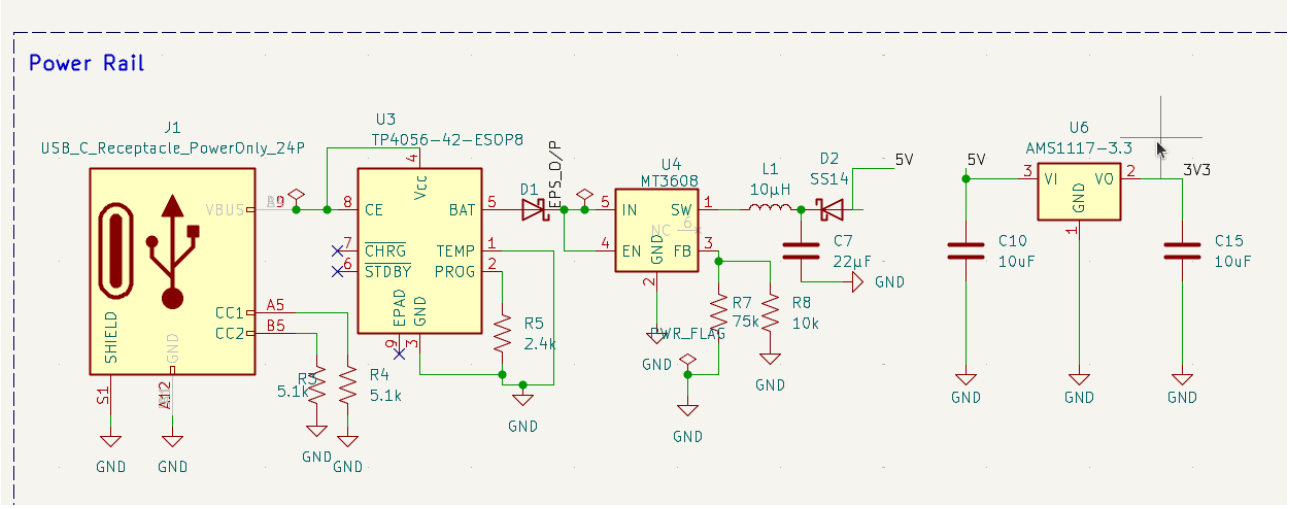
- Input and output capacitors

Special layout emphasis was placed on minimizing the high-di/dt switching loop. The schematic arrangement ensures that the inductor,diode,and capacitors from a compact loop to reduce EMI and switching noise.

- **LDO Regulator:** The 5V output from the boost stage feeds a low-droupot regulator (LDO) t generate a stable 3.3V rail for digital logic and sensors. The LDO ensures:

- Low ripple output
- Noise suppression
- Stable supply for MCU and peripherals

This dual-stage regulation(Boost+LDO) improves power integrity by siolating switching noise from sensitive digital circuits.



IV. Microcontroller Core block

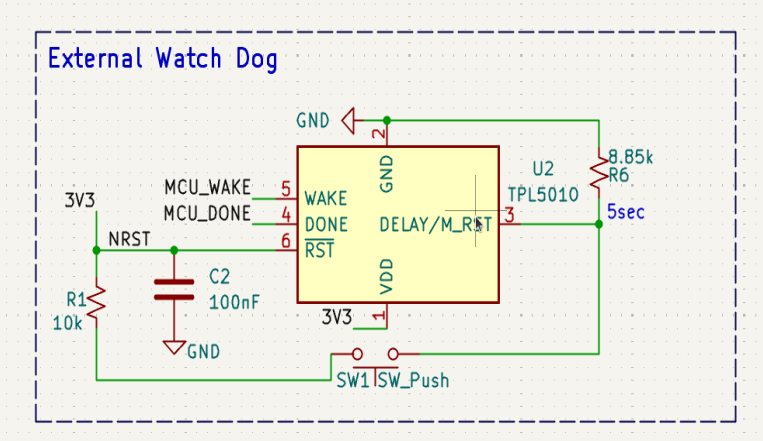
The central processing unit is an STM32 microcontroller selected for its:

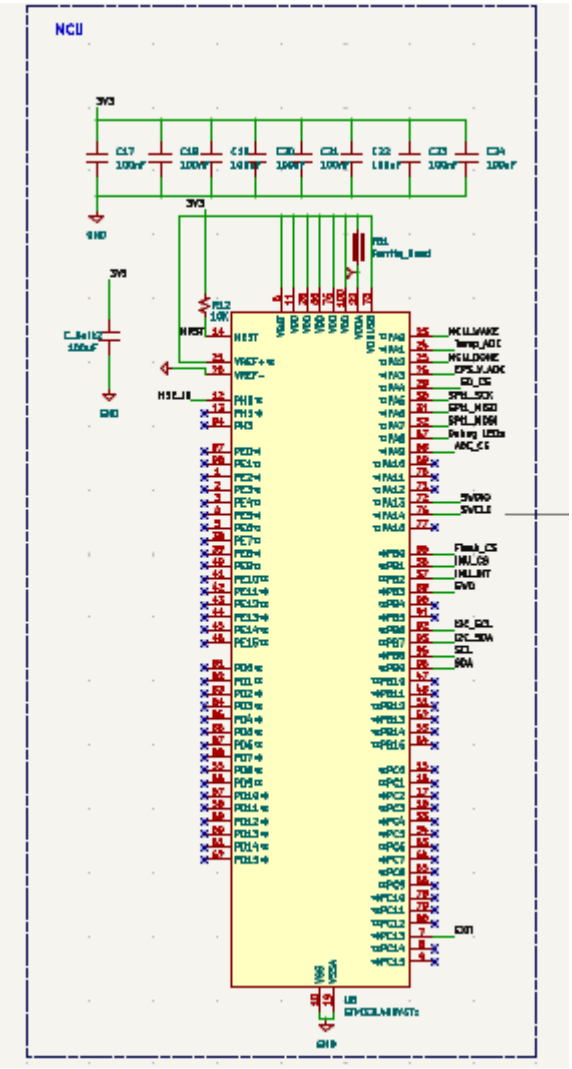
- Sufficient GPIO availability
- Multiple SPI and I2C interfaces
- ADC capability
- Low-power operation

The MCU handles:

- Sensor data acquisition
- Memory management
- SPI and I2C communication
- ADC sampling

- Current monitoring
- SD card logging
- System diagnostics



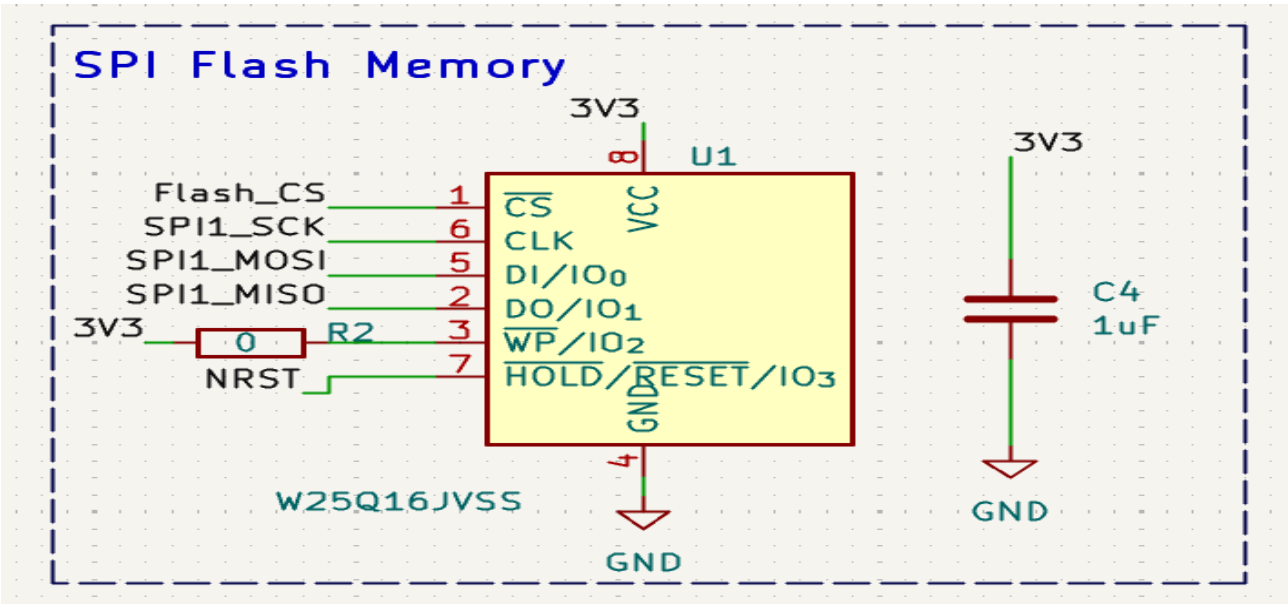


An external watchdog circuit is integrated to enhance reliability by resetting the MCU in case of software malfunction.

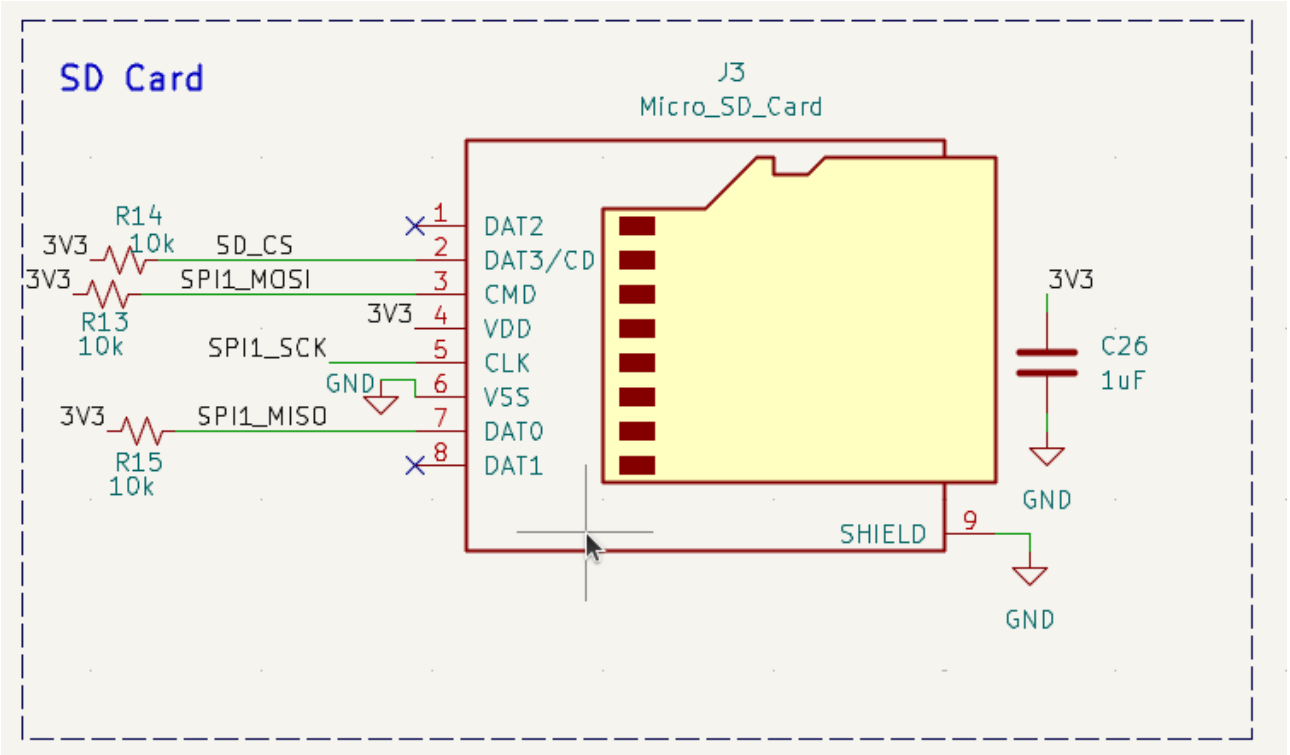
V. Memory and Data Storage Block

The system integrates two storage mechanisms:

- **SPI Flash Memory:** Used for firmware backup and non-volatile storage. Connected via SPI interface to the MCU. Short trace routing and controlled layout minimize signal degradation.



- **SD Card Interface:** Used for high-capacity telemetry data logging. Connected using SPI mode for simplicity. The connector is positioned near the board edge for accessibility. Proper pull-ups and short routing maintain signal integrity.



VI. Sensor Telemetry Block

The telemetry subsystem integrates sensors for system monitoring and data acquisition:

- IMU (Inertial Measurement Unit) for motion sensing
- Thermistor for temperature measurement
- Current sensor with shunt resistor
- Battery voltage monitoring using resistor divider + ADC

Telemetry Data Flow:

Sensors → Analog/Digital Interface → STM32 MCU → Data Processing → Storage (SPI Flash / SD Card)

The MCU periodically samples telemetry data and stores or transmits it depending on mission logic.

- **IMU (Inertial Measurement Unit):**

Purpose

The IMU measures acceleration and angular motion of the satellite. In CubeSat systems, IMU data is used for:

- Attitude determination

- Motion tracking
- Stabilization algorithms
- Event detection

Interface

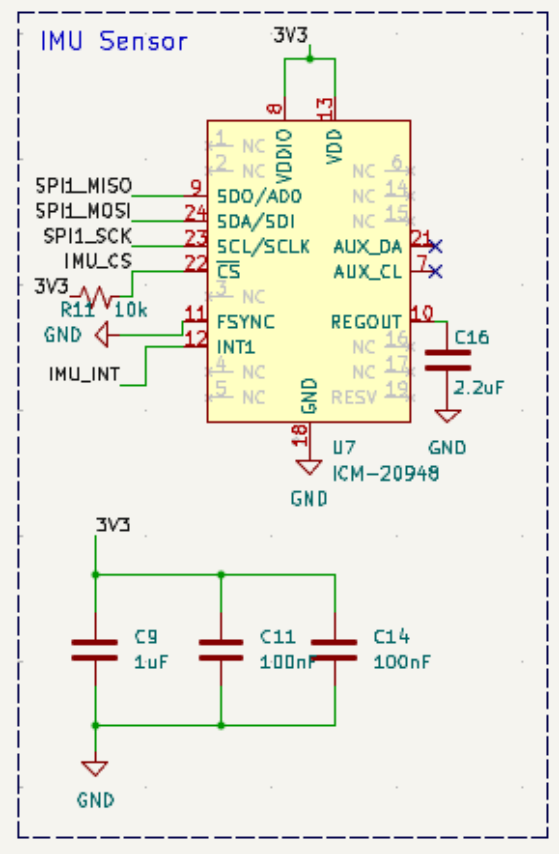
The IMU is connected to the STM32 via SPI (preferred for reliability and noise immunity). SPI was selected due to:

- Higher data throughput
- Better noise resistance compared to I2C
- Dedicated chip-select control

Design Considerations

- Short SPI traces between MCU and IMU
- Dedicated ground stitching around IMU
- Placement away from boost converter inductor
- Decoupling capacitor placed close to sensor supply pin

Magnetic interference from switching inductors can affect IMU readings; therefore, placement was optimized to isolate it from noisy power sections.



- **Current Sensor Block**

Purpose

The current sensor monitors system load current and provides telemetry for:

- Power budgeting
- Load profiling
- Fault detection
- Efficiency estimation

Implementation

The design uses:

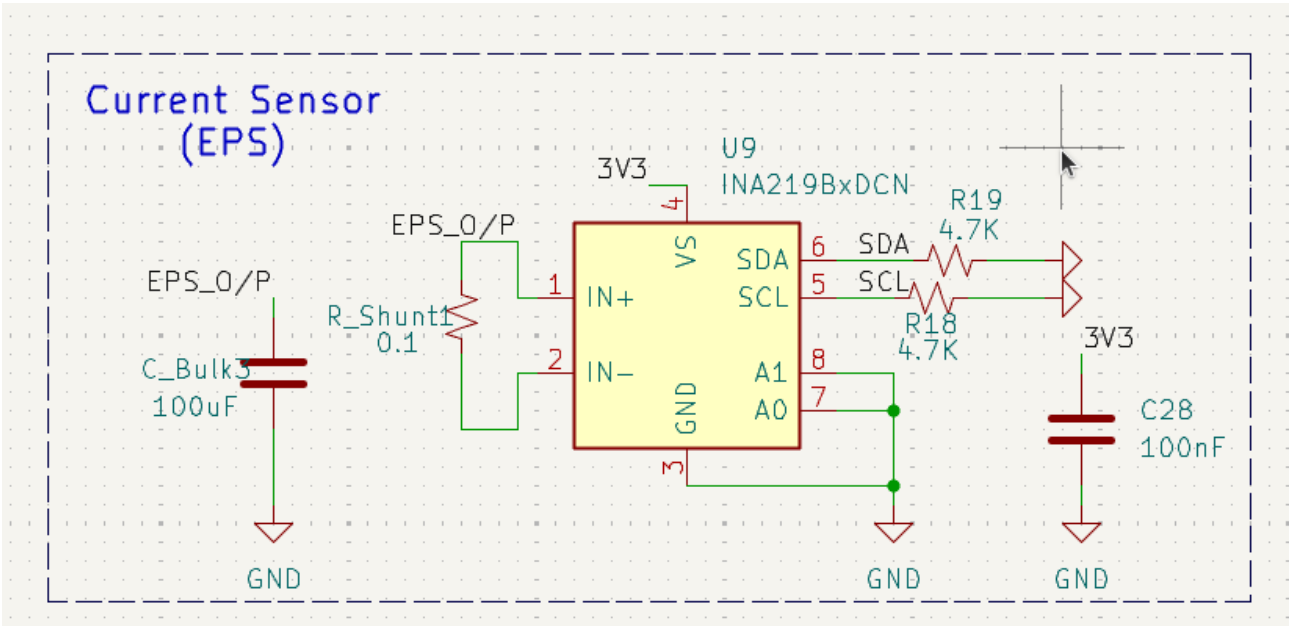
- Low-value shunt resistor
- Current sensing IC (or amplifier)
- Kelvin routing for accurate measurement

The shunt resistor is placed in series with the battery or regulated output. The voltage drop across the shunt is amplified and fed to the MCU through an analog input or digital interface.

Layout Strategy

- High-current path kept short and wide
- Sense lines routed separately (Kelvin connection)
- Analog trace kept away from switching node
- Ground reference stable and low impedance

This ensures accurate current measurement without switching noise interference.



VII. Battery Voltage Monitoring (ADC Block)

Purpose

Battery voltage monitoring allows the MCU to:

- Estimate battery state of charge
- Detect undervoltage conditions
- Trigger safe shutdown
- Log battery health over time

Implementation

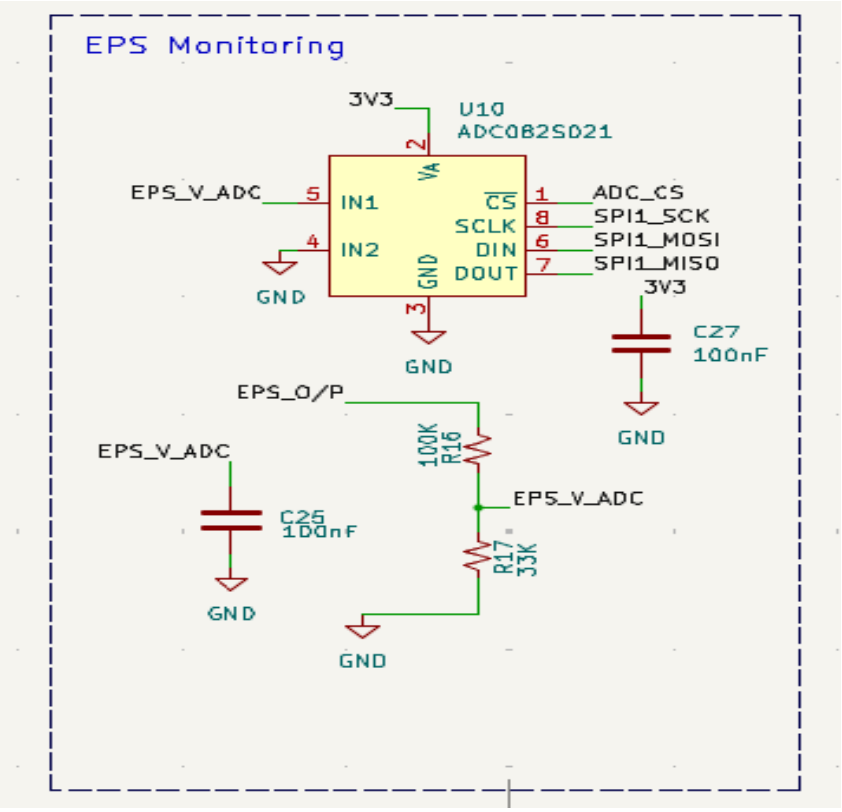
A resistive voltage divider is connected between battery positive terminal and ground. The midpoint of the divider feeds an ADC input of the STM32.

Since the battery voltage can reach 4.2V, the divider scales it down to a safe 0–3.3V range compatible with MCU ADC

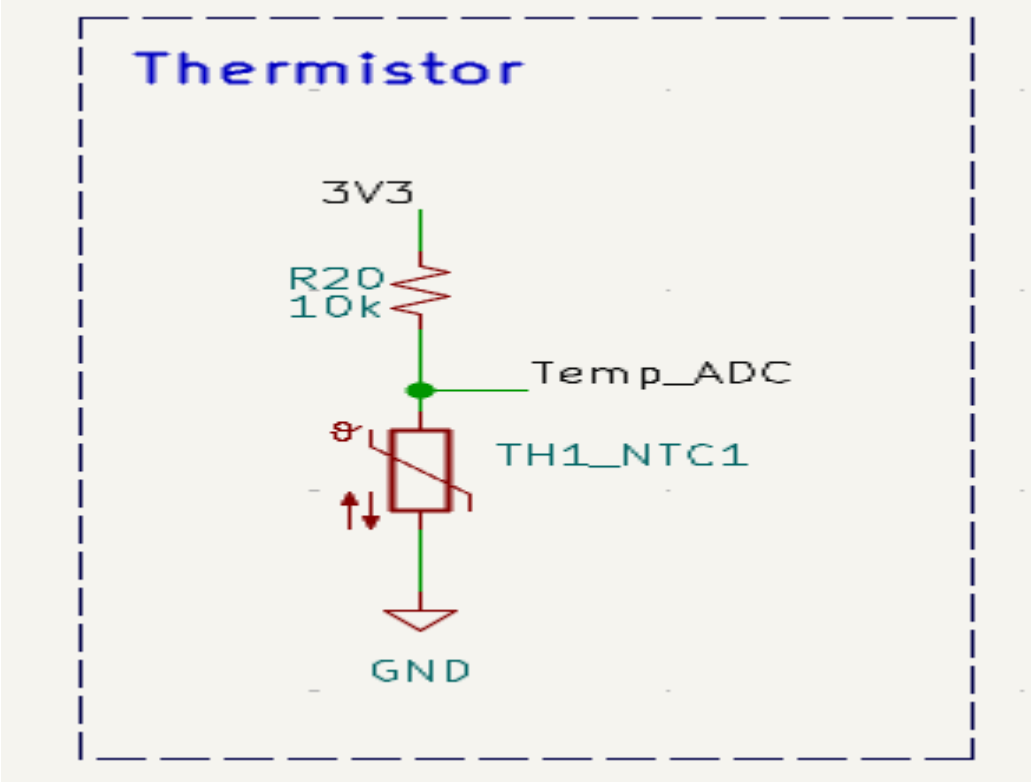
Additional Considerations

- RC filtering added before ADC input
- Divider resistor values selected to minimize power loss
- Analog ground used as reference

The ADC sampling provides digital representation of battery voltage for firmware processing.



The thermistor forms part of a voltage divider circuit connected to the ADC for temperature estimation.

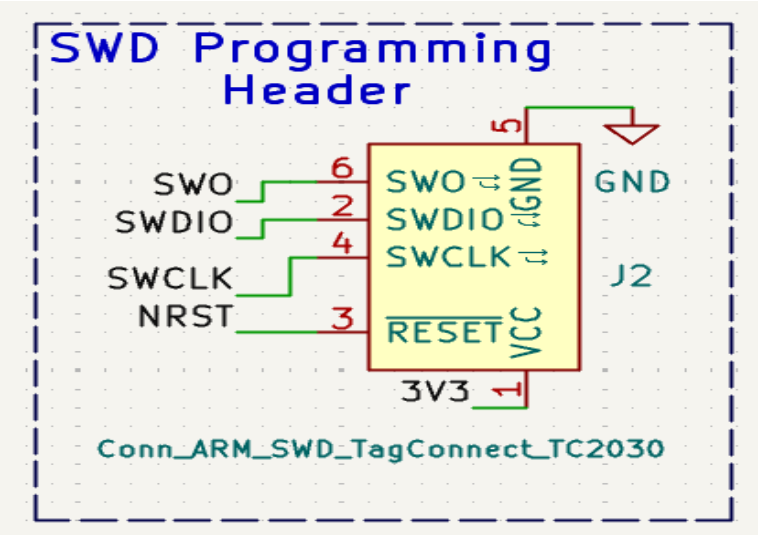


VIII. Debug and Programming Interface

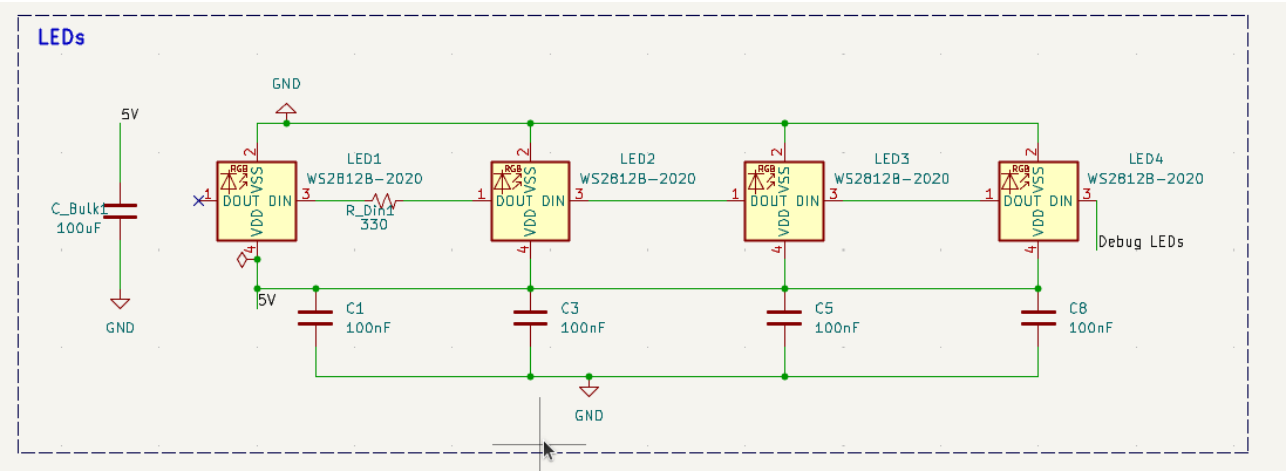
A Serial Wire Debug (SWD) interface is provided for:

- Firmware upload
- Real-time debugging
- System diagnostics

The SWD connector is placed at an accessible location on the PCB. Signal traces are short and directly routed to MCU debug pins.



Status LEDs are incorporated to indicate power presence, charging state, and MCU activity.



IX. Grounding and Power Distribution Strategy

The architecture follows a 2-layer PCB configuration with:

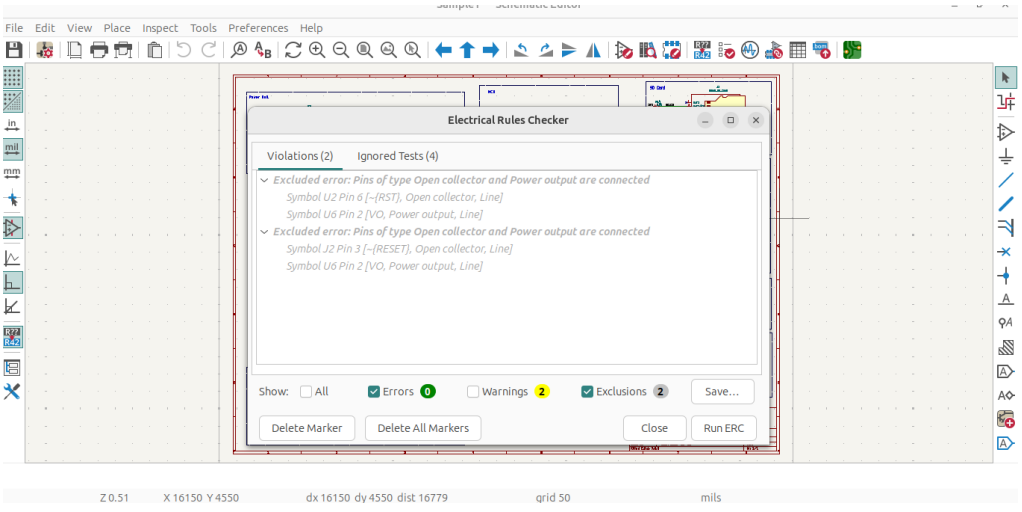
- Bottom layer: Solid ground plane
- Bottom layer: Solid ground plane

Ground stitching vias are placed:

- Low impedance return path
- Reduced EMI
- Improved signal integrity
- Thermal distribution

X. ERC

Electrical Rule Check:



PCB LAYOUT METHODOLOGY

Overview -

The PCB layout of the CubeSat OBC was implemented using a structured and rule-driven approach to ensure electrical reliability, signal integrity, thermal stability, and manufacturability compliance. The design was implemented as a two-layer PCB, balancing performance and cost while maintaining a clean ground return path.

The layout methodology followed a systematic sequence:

I. Mechanical definition

II. Layer stack planning

III. Component placement strategy

IV. Power routing

V. Signal routing

VI. Ground plane implementation

VII. Design Rule Check (DRC) validation

VIII. 3D verification

I. Mechanical Planning and Board Outline

Before placement, the board outline was defined considering:

- Compact footprint
- Connector accessibility (USB-C, SD card)
- Mounting hole positioning
- Clearance from board edges (≥ 1 mm copper clearance)

All copper features were maintained at a minimum 1 mm distance from the board edge to prevent exposed copper during fabrication.

II. Layer stack planning

The PCB was implemented as a 2-layer board with the following configuration:

- Top Layer (F.Cu): Component placement and signal routing
- Bottom Layer (B.Cu): Continuous ground plane

The bottom layer was primarily reserved for ground to:

- Provide a low-impedance return path
- Reduce EMI
- Improve signal integrity

- Enhance thermal spreading

This configuration ensures stable reference for digital and analog signals.

III. Component placement strategy

Component placement followed a functional zoning approach.

1. Power Section Placement

The power section (USB input, TP4056 charger, boost converter, LDO) was placed on one side of the board to isolate switching noise from digital and sensor sections.

Key principles followed:

- Inductor placed immediately next to SW pin
- Input and output capacitors placed as close as possible to regulator pins
- Short high-current loops
- Minimal switching node copper area

This reduces switching loop area and EMI radiation.

2. MCU Placement

The STM32 microcontroller was placed near the center of the board to minimize trace length to:

- SPI Flash
- SD card
- IMU
- ADC monitoring circuits

Decoupling capacitors were placed within 2–3 mm of each VDD pin to ensure stable supply filtering.

3. Sensor and Analog Placement

Sensitive analog components (thermistor, ADC divider, current sensing circuitry) were placed:

- Away from switching regulator
- In a relatively quiet ground region
- With short signal routing

The IMU was positioned away from the boost inductor to prevent magnetic interference.

4. Memory and Storage Placement

SPI Flash was placed close to the MCU to maintain short SPI trace lengths.

The SD card connector was positioned at the board edge for user accessibility and mechanical stability.

IV. Routing Strategy

Routing followed a strict priority-based order:

1. Step 1: High-Current Power Routing

- Battery traces routed first
- Boost converter high-current path routed with wide traces
- 3.3V main rail routed with sufficient width

Trace width was selected based on expected current.

2. Step 2: Switching Loop Optimization

For the boost converter:

- Minimized loop area between switch, inductor, diode, and capacitor
- Kept feedback trace short and isolated
- Avoided routing signals under the switching node

This is critical for reducing EMI and ripple.

3. Step 3: MCU Power Routing

- Routed VDD traces short
- Connected each decoupling capacitor directly to ground plane via short via
- Avoided shared return paths with switching current

4. Step 4: Digital Signal Routing

SPI and communication lines were routed:

- As short as possible
- Avoiding sharp 90° bends
- With consistent spacing
- Without crossing split ground areas

Where necessary, vias were used to escape tight pin spacing.

5. Step 5: Analog Routing

Analog signals (ADC inputs, current sense signals) were routed:

- Away from switching nodes
- With minimal crossing of digital traces
- With RC filtering where required

Kelvin routing principles were applied for current sense lines.

V. Ground Plane Implementation

The bottom layer was filled with a continuous GND copper zone.

Key grounding techniques:

- Solid ground reference under MCU
- Thermal vias under exposed pads
- Stitching vias around switching regulator
- Stitching vias near decoupling capacitors
- Perimeter stitching along board edges

Ground stitching improves:

- Return current continuity
- EMI suppression
- Thermal dissipation

Care was taken not to split the ground plane with unnecessary signal routing.

VI. Thermal Management

Thermal vias were added under:

- TP4056 exposed pad
- High-power regulator components

This improves heat transfer from top copper to bottom ground plane.

Component spacing was also considered to allow heat spreading.

VII. Design Rule Verification

Design Rule Checks (DRC) were performed iteratively to ensure manufacturability.

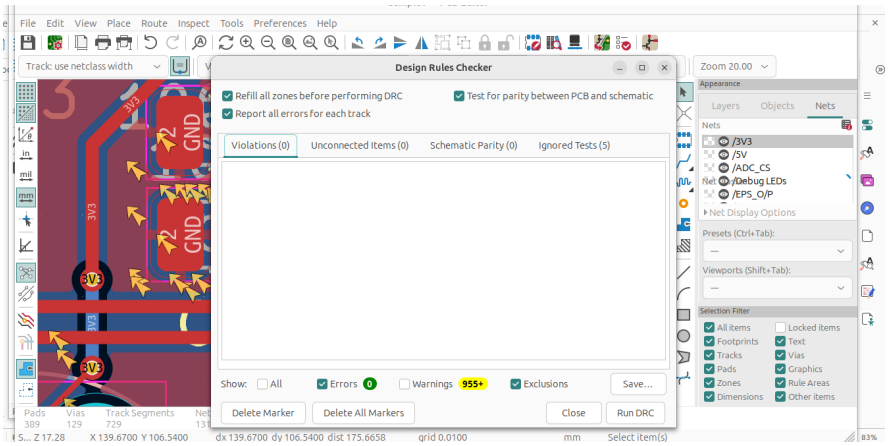
Key constraints enforced:

- Minimum clearance: 0.15–0.2 mm
- Minimum via drill: 0.3 mm
- Minimum annular ring: 0.15 mm
- Minimum hole clearance: 0.25 mm

Several DRC violations were encountered during layout, including:

- Thermal spoke clearance issues
- Annular width violations
- Via diameter mismatches
- Hole clearance violations

These were resolved through rule tuning and footprint adjustments, ensuring fabrication compatibility.

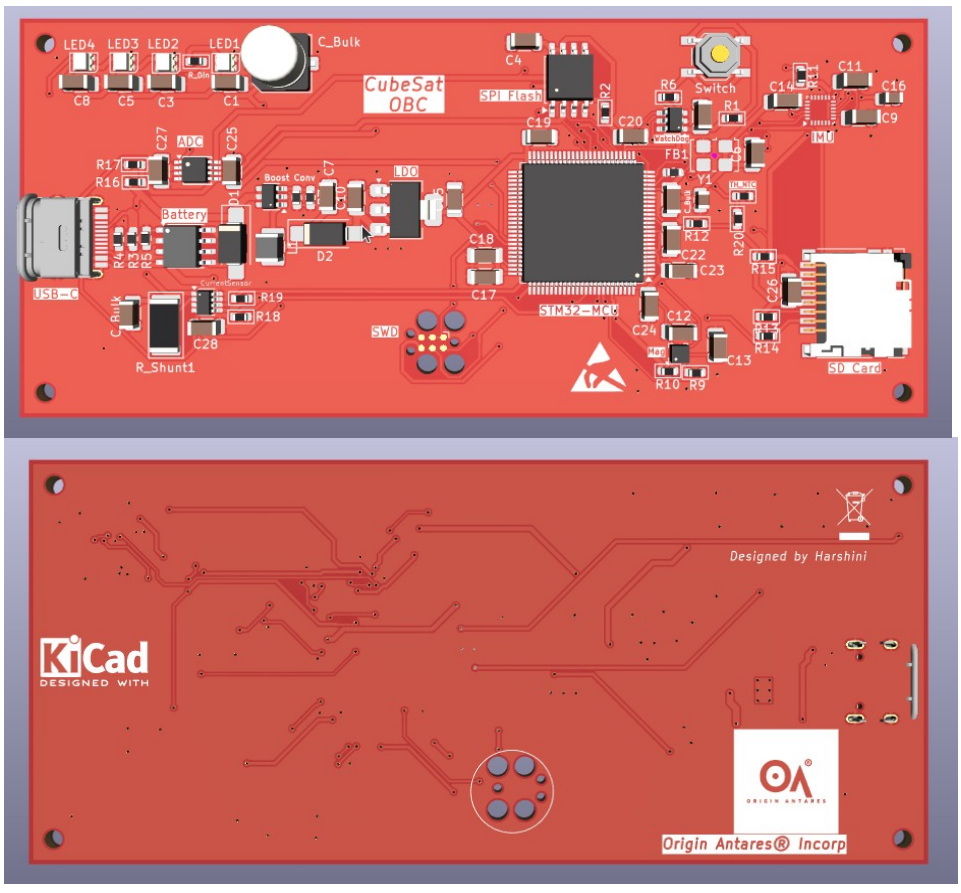


VIII. 3D Verification

The 3D viewer was used to:

- Verify connector orientation
- Confirm SD card alignment
- Check component spacing
- Validate mechanical clearances

Solder mask color and 3D rendering were also used for presentation verification.



IX. Manufacturability Considerations

The layout was finalized only after:

- Eliminating all DRC errors
- Ensuring adequate copper-edge clearance
- Verifying drill sizes within fabrication limits
- Confirming proper silkscreen placement

The final design is compatible with standard PCB fabrication processes using 2-layer FR4 material.