1. Question 1

/ 1

Which of the following is/are false?
a. Processor can directly access data from secondary memory.
b. Primary memory is used as backup memory.
c. Primary memory stores the active instructions and data for the program being executed on the processor.
d. Primary memory can store only instructions.

Hide answer choices

1. **a , b, c**
2. **a and b**
3. **a**
4. **a and d**

2. Question 2

/ 1

Program counter:

Hide answer choices

1. **Counts the total number of instructions present in a program**
2. **Points to the next instruction that is to be executed.**
3.

Points to the current instruction that is being executed

4. ☐

Stores the data of the current instruction that is being executed.

3. Question 3

/ 1

Which of the following contains circuitry to carry out operations such as addition, multiplication etc?

Hide answer choices

1. ☐

Control Unit

2. ☐

Memory Unit

3. ☐

ALU

4. ☐

Input/Output Unit

4. Question 4

/ 1

Which of the following statements are true?
a. The ENIAC computer was built using mechanical relays.
b. Harvard Mark1 computer was built using mechanical relays.
c. PASCALINE computer could multiply and divide numbers by repeated addition and subtraction.
d. Charles Babbage built his automatic computing engine in the 19th century.

Hide answer choices

1. ☐

a and b

2. ☐

a, b, d

3. ☐

b and c

4. ☐

d and c

5. Question 5

/ 1

Which of the following generates the necessary signals required to execute an instruction in a computer?

Hide answer choices

1. ☐

Arithmetic and Logic Unit

2. ☐

Memory Unit

3. ☐

Input/Output Unit

4. ☐

Control Unit

6. Question 6

/ 1

An instruction ADD R1, A is stored at memory location 4004H. R1 is a processor register and A is a memory location with address 400CH. Each instruction is 32-

bit long. What will be the values of PC, IR and MAR during execution of the instruction?

Hide answer choices

1. **PC=4004H; IR= ADD R1, A; MAR 400CH**
2. **PC=4008H; IR= ADD; MA= 400CH**
3. **PC=4008H; IR=ADD R1, A; MAR= 400CH**
4. **None of the above**

7. Question 7

/ 1

Consider a 1 MB (Megabyte) byte-addressable memory system, with a word size of 32 bits. The number of bits in MAR and MDR will be:

Hide answer choices

1. **23,32**
2. **20, 8**
3. **23, 32**
4. **20, 32**

8. Question 8

/ 1

A computer has 2GB (Gigabytes) of byte-addressable memory. The number of address lines will be 32

1. **T**

   True

2. **F**

   False

9. Question 9

/ 1

Which of the following statements are false for Harvard architecture?

Hide answer choices

1. **The program and data are stored in separate memory units.**

2. **The program and data are stored in the same memory.**

3. **The processor fetches instructions from program memory and accesses data from data memory.**

4. **The program memory and data memory can be built using different memory technologies.**

10. Question 10

/ 1

For a 512 X 32 bit memory that contains 512 locations each with 32-bit data, what will be the address (in binary) of the 389th location? (Assume the first location as 0).

Hide answer choices

1. ☐

   110000100

2. ☐

   110000101

3. ☐

   011000100

4. ☐

   011000101

11. Question 11

/ 1

Consider a 32-bit machine where an instruction (SUB R1, LOCA) is stored at location 2004H. LOCA is a memory location whose value is 1024H. The number of memory access required to execute this instruction will be?

Hide answer choices

1. ☐

   4

2. ☐

   2

3. ☐

   8

4. ☐

   16

12. Question 12

/ 1

Which of the following statements are true for Moore's law?

Hide answer choices

1. **Moore's law predicts that power dissipation will double every 18 months.**

2. **Moore's law predicts that the number of transistors per chip will double every 18 months**

3. **Moore's law predicts that the speed of VLSI circuits will double every 18 months**

4. **None of the above**

1. Question 1

/ 1

Consider the following statement for representing signed numbers using sign-magnitude, 1's complement, and 2's complement format:
(i) Sign of the number can be identified using MSB.
(ii) By flipping the sign bit we can obtain the number of its opposite sign.
Which of the following is correct?

Hide answer choices

1. **Only (i) is true**

2. **Only (ii) is true**

3. **Both (i) and (ii) are true**

4. ☐

   Both (i) and (ii) are false

2. Question 2

/ 1

The decimal number (35.5) base 10 in binary notation is?

Hide answer choices

1. ☐

   100011.101

2. ☐

   100011.1

3. ☐

   00110101.0101

4. ☐

   110101.101

3. Question 3

/ 1

The number (110.101001) base 2 in hexadecimal notation is?

Hide answer choices

1. ☐

   6.A4

2. ☐

   C.A4

3. ☐

   6.29

4. ☐

C.29

4. Question 4

/ 1

The addressing mode that adds the displacement and the index register to get the effective address of the operand is called

Hide answer choices

1. ☐

Indexed addressing

2. ☐

Base-Indexed addressing

3. ☐

Register Indirect Addressing

4. ☐

Relative addressing

5. Question 5

/ 1

Registers R1 and R2 contain data values 600 and 800 respectively in decimal, and the word length of the processor is 4 bytes. The effective address of the memory operand for the instruction “LOAD R5,10(R1,R2)” will be 1410 .

1. T

○ True

2. **F**

○ False

6. Question 6

/ 1

Which of the following statements are false for MIPS 32 register set?
a. Register R0 always contains the value 0.
b. Any register other than R0 can be used for register indirect addressing.
c. Any register other than R0 can be used to hold the return address for function calls.
d. R31 is a special register used as a stack pointer.

Hide answer choices

1. **a, c and d**
2. **c and d**
3. **d**
4. **a and b**

7. Question 7

/ 1

The MIPS code for A = B+C where B is loaded in register $S2 and C is loaded in register $S3 is?

Hide answer choices

1. **ADD $S1, $S2, $S3**
2. **ADDI $S3, $S2, $S1**
3. **ADD $S3, $S2, $S1**
4.

None of the above

8. Question 8

/ 1

In MIPS32, to fetch a 32-bit word from memory in a single cycle, the word has to be stored from memory location?

Hide answer choices

1. **0019H**
2. **001BH**
3. **001AH**
4. **0018H**

9. Question 9

/ 1

For the instruction STORE R1,35(R2) what will be the effective address of the memory operand if R2 is 200 (in decimal)?

Hide answer choices

1. **35**
2. **165**
3. **235**

4. ☐

200

10. Question 10

/ 1

How do you represent -10 using 16-bit, 2's complement representation?

Hide answer choices

1. ☐

1000 0000 0001 0110

2. ☐

0000 0000 0000 1010

3. ☐

1111 1111 1111 0110

4. ☐

0000 0000 0001 0110

1. Question 1

/ 1

What kind of processor is x86?

Hide answer choices

1. ☐

RISC

2. ☐

CISC

3. ☐

DISC

4. ☐

None of the above

2. Question 2

/ 1

A processor having a clock cycle time of 5ns will have a clock rate of _____ MHz.

Hide answer choices

1. ☐

200

2. ☐

245

3. ☐

257

4. ☐

303

3. Question 3

/ 1

Which of the following statements is/are true with respect to Amdahl's law?
a. It expresses the law of diminishing returns.
b. It expresses the maximum speedup that can be achieved.
c. It provides a measure to compare the execution times of two machines.
d. All of these

Hide answer choices

1. ☐

a and c

2. ☐

b and c

3. ☐

d only

4. ☐

a and b

4. Question 4

/ 1

The total execution time of a typical program is made up of 60% of CPU time and 40% of I/O time. Which of the following alternatives is better? Assume that there is no overlap between CPU and I/O operations.

Hide answer choices

1. ☐

Increase the CPU speed by 50%.

2. ☐

Reduce the I/O time by half

3. ☐

Both alternatives give the same speedup

4. ☐

None of these

5. Question 5

/ 1

Consider a program with 50 million instructions, a machine requires 25 milliseconds to execute
this program. What will be the MIPS rating of the machine?

Hide answer choices

1. ☐

20

2. ☐

200

3. ☐

2000

4. ☐

20000

6. Question 6

/ 1

A program is running on a machine that has a total of 1000 instructions, the average cycles per instruction for the program are 1.5, and the execution time of the program is 1 μsec. The clock rate of the machine is _____ GHz.

Hide answer choices

1. ☐

1.5

2. ☐

2

3. ☐

1

4. ☐

1.75

7. Question 7

/ 1

Suppose that a machine A executes a program with an average CPI of 3. Consider another machine B (with the same instruction set and a better compiler) that executes the same program with 10% less instructions and with a CPI of 1.5 at 1.5 GHz. The clock rate of A so that the two machines have the same performance is 3.30,3.40 GHz.

1. T

- True

2. **F**

- False

8. Question 8

/ 1

Suppose that a machine X executes a program with an average CPI of 2.5. Consider another machine Y (with the same instruction set and a little better compiler) that executes the same program with 10% fewer instructions and with the CPI of 1.5 at 4GHz. What should be the clock
frequency of X so that both the machines have the same performance?

Hide answer choices

1. **7.40GHz**
2. **7.40MHz**
3. **7.40KHz**
4. **7.40Hz**

9. Question 9

/ 1

On which of the following does CPI depend on?

Hide answer choices

1. **Instruction Set Architecture**
2.

CPU organization

3. ☐

Complier

4. ☐

All of these

10. Question 10

/ 1

Consider a program whose instruction count is 1,500, average CPI is 2, and clock cycle time is 1
nanosecond. Suppose we use a new compiler on the same program for which the new instruction count is 2,500, and the new CPI is 1.5, which is running on a faster machine with a clock
cycle time of 0.5 nanoseconds. The speedup achieved will be?

Hide answer choices

1. ☐

1.66

2. ☐

0.63

3. ☐

1.63

4. ☐

None of these

1. Question 1

/ 1

Which of the following statement is/are correct?

Hide answer choices

1. ☐

MIPS instructions are 32 bits long.

2. ☐

All instructions are stored in memory with address having the last two bits 00.

3. ☐

Program Counter is decremented to 4 to point to the next instruction

4. ☐

All of these

2. Question 2

/ 1

The correct sequence in Fetch-Execute cycle is:

Hide answer choices

1. ☐

Decode, Fetch, Execute

2. ☐

Fetch, Execute, Decode

3. ☐

Fetch, Decode, Execute

4. ☐

None of the above

3. Question 3

/ 1

Which instruction does the following set of micro-operations refer to:
Steps Action
1 PCout, MARin, Read, Select4, Add, Zin
2 Zout, PCin, Yin, WMFC
3 MDRout, IRin
4 R1out, Yin

5 R2out, SelectY, Add, Zin
6 Zout, R1in, End

Hide answer choices

1. ☐

ADD R2, R1

2. ☐

ADD R1, R2

3. ☐

MOVE R1, R2

4. ☐

MOVE R2, R1

4. Question 4

/ 1

The Instruction Register (IR)

Hide answer choices

1. ☐

Holds the memory address of the next instruction

2. ☐

Holds the memory address of the current instruction

3. ☐

Holds the executed or decoded instruction.

4. ☐

Holds the encoded instruction that is currently being executed or decoded.

5. Question 5

/ 1

Which of the following statements are true for vertical micro-instruction encoding?

Hide answer choices

1. **If there are control signals, every control word stored in control memory (CM) consists of k bits, one bit for every control signal.**
2. **Sequential activation of at most one control signal in a single time step.**
3. **Low cost of implementation.**
4. **None of these**

6. Question 6

/ 1

Which of the following statements is/are false?

Hide answer choices

1. **Diagonal micro-instructions encoding requires multiple decoders.**
2. **In vertical micro-instructions encoding, more than one control signals cannot be activated at a time**
3. **Horizontal micro-instructions encoding has a lower cost of implementation.**
4. **None of these.**

7. Question 7

/ 1

Which of the following is true for MIPS32 register bank?

Hide answer choices

1. **There is one read port and one write port.**
2. **There is one read port and two write ports.**
3. **There are two read ports and one write port.**
4. **None of these**

8. Question 8

/ 1

Consider a single bus system, how many steps will be required to complete the instruction MOVE R1,R2

Hide answer choices

1. **2**
2. **3**
3. **4**
4.

5

9. Question 9

/ 1

Which of the following is not true for a branch instruction in MIPS32?

Hide answer choices

1. **The branch condition is computed in EX stage.**
2. **The new PC value is loaded in the MEM stage.**
3. **The target address is computed in ID stage.**
4. **The WB stage is not required.**

10. Question 10

/ 1

Consider a hardwired control unit where each instruction of the machine requires maximum of
50 steps to complete its execution. If the total number of such instructions are 129, what should be the size of step decoder and instruction decoder respectively?

a.

Hide answer choices

1. **6x64; 7x128**
2. **50x1; 129x1**
3.

64x1, 256x1

4. 6x64, 8x256

1. Question 1

/ 1

How many address and data lines will be there for a 16M x 32 memory system?

Hide answer choices

1. 24 and 5
2. 20 and 32
3. 24 and 32
4. None of the above

2. Question 2

/ 1

Assume that a 1G x 1 DRAM memory cell array is organized as 1M rows and 1K columns. The number of address bits required to select a row and a column will be?

Hide answer choices

1. 20 and 10
2. 30 and 1
3.

220 and 210

4. ☐

None of the above

3. Question 3

/ 1

What is the function of the chip select line (CS') in a memory chip?

Hide answer choices

1. ☐

Power supply is applied to the chip when CS' is activated.

2. ☐

The data bus is put in the high impedance state when CS' is deactivated.

3. ☐

It prevents two or more subsystems from using the memory simultaneously.

4. ☐

None of the above

4. Question 4

/ 1

Which of the following statement(s) is/are true?

Hide answer choices

1. ☐

In memory, data are stored in the form of 0's and 1's.

2. ☐

Memory system stores data and instruction.

3. ☐

Every bit of memory has a unique address.

4. ☐

All of these

5. Question 5

/ 1

Which of the following are true for Static RAM (SRAM)?

Hide answer choices

1. ☐

Power consumption is higher than Dynamic RAM (DRAM).

2. ☐

Packing density is higher than Dynamic RAM (DRAM).

3. ☐

It is faster than Dynamic RAM (DRAM).

4. ☐

It is non-volatile.

6. Question 6

/ 1

Which of the following statement(s) is/are false?

Hide answer choices

1. ☐

In volatile memory data is lost when power is switched off.

2. ☐

Dynamic memory requires periodic refreshing.

3. ☐

Magnetic tape does not allow random access of data.

4. ☐

None of these.

7. Question 7

/ 1

Which of the following is/are true for virtual memory systems?

Hide answer choices

1. ☐

It increases the size of the program that can be run

2. ☐

It increases the size of the physical memory

3. ☐

It increases the size of the secondary memory

4. ☐

It improves the processor-memory bandwidth

8. Question 8

/ 1

What is/are false for cache memory?

Hide answer choices

1. ☐

It consumes low power as compared to main memory.

2. ☐

It is a type of non-volatile memory.

3. ☐

It decreases the effective speed of the memory system.

4. ☐

All of these.

9. Question 9

/ 1

The total number of external connections required by an 8 x 8 memory will be 15

1. **T**

○ True

2. **F**

○ False

10. Question 10

/ 1

Which of the following statement is true for writing 1 in SRAM chip?

Hide answer choices

1. ☐

The bit line b is set with 1, and bit line b' is set with 0.

2. ☐

The bit line b is set with 0, and bit line b' is set with 1.

3. ☐

The bit line b is set with 1, and bit line b' is set with 1.

4. ☐

The bit line b is set with 0, and bit line b' is set with 0.

Question 1

.

/ 1

For a Hard disk rotating at a speed of 3600 rpm, Find the value of maximum delay

Hide answer choices

6.31 millisec

8.30 millisec

16.60 millisec

Question 2

/ 1

For a hard disk rotating at a speed of 9500 rpm, Find the value of average delay

---

Hide answer choices

6.31 millisec

4.15 millisec

3.152 millisec

2.8 millisec

Question 3

/ 1

The smallest unit of data transfer is__

Hide answer choices

sector

track

platters

Question 4

/ 1

The important factors listed are:

1.The time required to move the head to the desired track.

2.Average seek times are in the range 8 – 20 msec.

3.The total time to transfer a block of data (typically, a sector).

Out of these factors which are related to Seek time

Hide answer choices

1 only

1 and 2

2 and 3

all 1,2,3

Question 5

/ 1

The data from a CPU need to be stored in a backup memory. Which is the best possible solution for the same

Hide answer choices

SRAM

DRAM

Hard Disk

Volatile memory

Question 6

/ 1

To read a bit from a FG transistor the necessary action to be performed is

Hide answer choices

Apply a voltage on the control gate

Apply a voltage on the floating gate

Apply a voltage on the drain

Apply a voltage on the source

Question 7

/ 1

The material in between control gate and floating gate is a

Hide answer choices

Conductor

semi-conductor

Insulator

metal

Question 8

/ 1

The start and stop bits are characterised for

Hide answer choices

synchronous transmission

asynchronous transmission

clock driven transmission

Question 9

/ 1

Separate decoders for memory and IO are required in

Hide answer choices

IO mapped interfacing

Memory mapped Interfacing

direct interfacing

Question 1

/ 1

Several program instructions have to be executed for each data word transferred

between the I/O device and memory.

The above statement corresponds to which mode of data transfer?

Hide answer choices

DMA

Programmed I/O

Fixed I/O interfacing

Question 2

/ 1

Consider a programmed I/O system where 20 instructions are required to be executed for the

transfer of each word of data. The cycles-per-instruction (CPI) of the machine is 1.5 and the

processor clock frequency is 2 GHz. The maximum data transfer rate will be _____

million words per second. (Assume 1 million = 10^6)

Hide answer choices

66.67

23.46

22.67

87.54

Question 3

/ 1

Which of the following statement(s) is/are true for DMA data transfer?

Hide answer choices

Data transfer requires very less CPU intervention.

Not Suitable for transferring large blocks of data

No direct data transfer between I/O and memory.

Question 4

/ 1

Which of the following registers needs to be initialized before transfer of any data in DMA mode?

Hide answer choices

Memory Address

Word Count

Address of data on disk

All of the above

Question 5

/ 1

How many total keys are supported by a 4*4 MATRIX KEYBOARD

Hide answer choices

4

8

16

24

Question 6

/ 1

If a key is pressed in a a keyboard, the corresponding row and column are

Hide answer choices

grounded

raised to high voltage

raised to high impedance

Question 7

/ 1

Suppose that it is required to transfer 20K bytes in interrupt-driven mode of data transfer.

Every time an interrupt occurs, it involves the transfer of 64 bytes of data that takes 20

microseconds for the processor to service. The time required to transfer 40K bytes of data will

be ..... milliseconds? (Assume 1K = 1024)

Hide answer choices

5.25

6.25

12.5

32.56

Question 8

/ 1

Which of the following bus is more cheaper to implement?

Hide answer choices

Parallel Bus

Serial Bus

High bus

Question 9

/ 1

The maximum data transfer rates supported by USB 2.0 and USB 3.0 standards are respectively:

Hide answer choices

480Mbps and 5Gbps

2 Gbps and 10 Gbps

12 Mbps and 5 Gbps

5 Gbps and 10 Gbps

Question 10

/ 1

With Bridge-Based Bus Architectures

Hide answer choices

Intel follows this kind of architecture.

different buses

can operate in parallel.

System includes a lot of buses that are

segregated by bridges.

All of these

Question 1

/ 10

In the non-pipelined version, the execution time of an instruction is equal to

Hide answer choices

the combined delay of all stages

individual delay

multiplied delay

Question 2

/ 1

Consider a 5-stage instruction pipeline with stage delays of 20 nsec, 25 nsec, 35 nsec, 30 nsec,

and 22 nsec respectively. The delay of an inter-stage register stage of the pipeline is 2 nsec. The

total time required for the execution of 1000 instructions will be ..... microseconds.

Hide answer choices

59.14 microsec

37.14 microsec

220.19microsec

322.14 microsec

Question 3

/ 1

Consider a 3-stage instruction pipeline with stage delays of 25 nsec, 30 nsec and 15 nsec

respectively, and the delay of an inter-stage register stage of 5 nsec. Suppose the pipeline is

.

modified by splitting the 1st stage into two simpler stages with delays 10 nsec and 15 nsec, and

.

2nd stage into two simpler stages with delays 15 nsec and 15 nsec. For the execution of 1000

.

instructions, the speedup of the new 5-stage pipeline over the previous 3-stage pipeline will be

.

_____.

.

Hide answer choices

.

.

1.746

.

.

20.08

.

.

35.07

.

.

25.67

.

.

Question 4

.

/ 1

.

Since a new instrucEon is fetched every clock cycle, it is required to

.

_____ the ____ on each clock.

.

Hide answer choices

.

increment, PC

decrement,PC

increment,IP

DECREMENT,IP

Question 5

/ 1

Identify the statement related to pipeline hazard

Hide answer choices

operation occurs at full speed

prevent a pipeline from operating at its maximum

possible clock speed.

operation suspends

Question 6

/ 1

For the following MIPS32 program segment, how many stall cycles will be required .....?

1: LW R5, 200(R2)

2: ADD R1, R6, R8

3: SUB R3, R5, R8

Hide answer choices

2

1

0

4

Question 7

/ 1

Which of the following data hazards can cause performance degradation in the MIPS32 integer pipeline?

a. WAR data hazard.

b. WAW data hazard.

c. RAW data hazard.

Hide answer choices

a

b

c

Question 8

/ 1

Consider the MIPS32 pipeline with ideal CPI of 1.5. Assume that 30% of all instructions executed

are branch, out of which 90% are taken branches. The pipeline speedup for (i) predict taken and

(ii) predict not taken approaches to reduce branch penalties will be approximately:

a. 3.94, 3.85

b. 4.34, 4.29

c. 3.85, 4.34

d. 3.85, 3.94

Hide answer choices

a

b

c

d

Question 9

/ 1

Which of the following require additional hardware?

Hide answer choices

Bypassing

Concurrent access

splitting

Question 10

/ 1

In Bypassing which of the following is not required?

a) Requires multiplexers to select these additional paths.

b) The control unit identifies data dependencies and selects the multiplexers in a

suitable way.

c) Additional data transfer paths are to be added in the data path.

d) Splitting a clock cycle into two halves,

Hide answer choices

a

b

c

d

Question 1

/ 1

Loop unrolling requires significantly greater number of registers

True

F

False

Question 2

/ 1

Floating point will require more than one cycles in ____ stage

Hide answer choices

EX

FETCH

DEC

Question 3

/ 1

The number of cycles between an instruction producing a result and another instruction using it is known as

Hide answer choices

.

.

Hazard

.

.

Latency

.

.

delay

.

.

Interval

.

.

Question 4

.

/ 1

.

S.D F4, 40(R5) is used for

.

Hide answer choices

.

.

Storing from a floating-point register pair:

.

.

Loading into a floating-point register pair

.

.

Question 5

.

/ 1

In the floating-point extension of MIPS32, there are __ floating-point

registers

Hide answer choices

4

8

16

32

Question 6

/ 1

There is no limit to the number of instructions that can be fetched and issued in every

clock cycle.

T

True

F

False

Question 7

/ 1

Suppose the start-up time of vector multiply operation is 12 clock cycles.After start-up, the initiation rate is one per clock cycle. What will be the number of clock cycles required per result for a 64-element vector?

Hide answer choices

2.13

1.19

3.21

7.56

Question 8

/ 1

The start-up time (in clock cycles) will be equal to the

Hide answer choices

pipeline stalls once per vector

deeply parallel access.

depth of the functional unit pipeline.

processor-memory speed gap

Question 9

/ 1

Hyperthreading is

Hide answer choices

Single processor appears to be two logical processors.

processor can be considered to be using micro-programming.

RISC architecture supposedly execute instructions faster than CISC.

Question 10

/ 1

What is not true about Rapid Execution Engine?

a) ALUs run at twice the processor frequency.

b) Basic integer operations execute in 1⁄2 processor clock tick.

c) Provides higher throughput and reduced latency of execution.

d) Each logical processor has its own set of registers.

Hide answer choices

a

b

.

c

.

.

d

.

……

.

Question 1

.

/ 1

.

Decimal equivalent of 11101000 represented in 2’s complement format will be_____?

.

Hide answer choices

.

.

-18

.

.

18

.

.

21

.

.

-21

.

.

Question 2

.

/ 1

.

Largest number that can be represented using 8-bit 1’s complement representation will

.

be_____

.

Hide answer choices

.

.
127
.
.
256
.
.
128
.
.
212
.

.

Question 3

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/ 1

.

The minimum number of NAND gates required to design half adder is

.

Hide answer choices

.

.

3

.

.

4

.

.

5

.

.

6

.

.

Question 4

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/ 1

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For a Full adder Delay for Carry = _____ and Delay for Sum = ___

.

Hide answer choices

.

.

2 δ and 2 δ

.

.

2 δ and 3 δ

.

.

3 δ and 2 δ

.

.

3 δ and 3 δ

.

.

Question 5

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/ 1

.

Carry Look Ahead Adder is

.

Hide answer choices

.

.
Serial Adder

.
.
Parallel Adder

.
.
Spontaneous adder

.

.

Question 6

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/ 1

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In a 5-bit carry look-ahead adder, suppose we are adding two numbers A = (1, 0, 1, 1, 0) and B =

.

(1, 0, 1, 1, 1). The carry generate and carry propagate signals will be:

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Hide answer choices

.

.

G = (1, 0, 1, 1, 0) and P = (1, 0, 1, 1, 1)

.

.

G = (1, 0, 1, 1, 0) and P = (0, 0, 1, 0, 1)

.

.

G = (1, 0, 1, 1, 0) and P = (0, 0, 0, 0, 1)

.

.

G = (1, 0, 1, 1, 0) and P = (1, 0, 0, 0, 1)

.

.

Question 7

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/ 1

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Carry Select adder consists of __-

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Hide answer choices

.

.

two parallel adders

.

.

two serial adders

.

.

two selection adders

.

.

Question 8

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/ 1

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Suppose we are multiplying (-9) x (12) using Booth’s multiplier, where each number is

.

represented in 5 bits. What will be the values of A (temporary register), and Q (multiplier) after

.

third step?

.

Hide answer choices

.

.
00100, 00011

.
.
01001, 00011

.
.
00100, 10001

.

.

Question 9

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/ 1

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For n bit multiplication , number of additions=___ and shift operations=___

.

Hide answer choices

.

.

n and n

.

.

2n and n

.

.

2n and 2n

.

.

Question 10

.

/ 1

.

Booth’s multiplier inspects three bits of the multiplier at every step

.

.

T

. True

.

F

. False

.

Question 1

.

/ 1

.

Shift left by 1 bit means _____ by 2

Hide answer choices

Multiply

Divide

Add

Subtract

Question 2

/ 1

The number of significant digits depends on the number of bits in___

Hide answer choices

Mantissa

Exponent

Question 3

/ 1

IEEE-754 format supports __ rounding modes

Hide answer choices

3

4

5

6

Question 4

/ 1

For multiplying F1 = 270.75 and F2 = -2.375, result will include 2^ ___

Hide answer choices

8

9

7

Question 5

/ 1

The range of the number depends on the number of bits in __

Hide answer choices

Exponent

Mantissa

Question 6

/ 1

F = (-1)^s M x 2^E represents a __

Hide answer choices

Floating point number

Fixed point number

Question 7

/ 1

For addition of 2 numbers, We add the _____values after shifting one of them right for exponent

alignment.

Hide answer choices

Mantissa

Exponent

Sign bit

Question 8

/ 1

If the process of rounding generates a result that is not in normalized form, then

we need to____ the result.

Hide answer choices

discard

retain

re-normalize

Question 9

/ 1

For subtracting F2 = 234 from F1 = 210.75,Shift the mantissa of F2 ____ position,

Hide answer choices

right by 1

left by 1

right by 2

left by 2

Question 10

/ 1

The number of columns in a reservation table represents__

Hide answer choices

evaluation time

generation time

delay time

Question 1

/ 1

Which of the following statement is true in regards to memory?

Hide answer choices

The faster, smaller memory are always closer to processor

The memory, that is farthest away is the costliest.

As we move away from the processor, speed increases.

None of the above

Question 2

/ 1

Which of the following statements are false?

Hide answer choices

Temporal locality arises because of loops in a program.

Spatial locality arises because of loops in a program.

Temporal locality arises because of sequential instruction execution.

Spatial locality arises because of sequential instruction execution.

Question 3

/ 1

In a two-level cache system, the access times of L1 and L2 caches are 1 and 8 clock cycles respectively. The miss penalty from L2 cache to main memory is 18 clock cycles. The miss rate of L1 cache is twice that of L2. The average memory access time of the cache system is 2 cycles. The miss rates of L1 and L2 caches respectively are?

Hide answer choices

0.130 and 0.065

0.056 and 0.111

0.0892 and 0.1784

0.1784 and 0.0892

Question 4

/ 1

The memory access time is 1 nsec for a read operation with a hit in cache, 5 nsec for a read operation with a miss in cache, 2 nsec for a write operation with a hit in cache, and 10 nsec for a write operation with a miss in cache. The execution of a sequence of instructions involves 100 instruction fetch operations, 60 memory operand read operations, and 40 memory operand write operations. The cache hit ratio is 0.9. The average memory access time (in nanoseconds) in executing the sequence of instructions is?

Hide answer choices

1.26

1.68

2.46

4.52

Question 5

/ 1

Assume that a read request takes 50 nsec on a cache miss and 5 nsec on a cache hit. While running a program, it is observed that 80% of the processor's read requests result in a cache hit. The average read access time is **14**nsec

Question 6

/ 1

A cache memory system with capacity of N words and block size of B words is to be designed. If it is designed as a direct mapped cache, the length of the TAG field is 10 bits. If it is designed as a 16-way set associative cache, the length of the TAG field will be how many bits?

Hide answer choices

19

17

16

13

Question 7

/ 1

Which of the following statements is true?

Hide answer choices

The implementation of direct mapping technique for cache requires expensive hardware to carry out division.

The set associative mapping requires associative memory for implementation.

A main memory block can be placed in any of the sets in set associative mapping.

None of the above.

Question 8

/ 1

7. Consider a direct-mapped cache with 64 blocks and a block size of 16 bytes. Byte address 1200 will map to block number 11 of the cache.

T

True

F

False

Question 9

/ 1

How can the cache miss rate be reduced?

Hide answer choices

By using larger block size

By using larger cache size

By reducing the cache associativity

None of the above

Question 10

/ 1

Consider a two-level memory hierarchy with separate instruction and data caches in level 1, and main memory in level 2. The clock cycle time in 1 ns. The miss penalty is 20 clock cycles for both read and write. 2% of the instructions are not found in I-cache, and 10% of data references not found in D-cache. 25% of the total memory accesses are for data, and cache access time (including hit detection) is 1 clock cycle. The average access time of the memory hierarchy will be which of the following nanoseconds?

Hide answer choices

1.76 ns

1.68 ns

1.88 ns

1.86 ns