NPTEL Online Certification Courses

Indian Institute of Technology Kharagpur

Course Name: Computer Architecture and Organization

Questions Solutions

TYPE OF QUESTION: MCQ/MSQ/SA

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- https://www.linkedin.com/in/aarish-ejaz-22b158200
- https://www.linkedin.com/in/piyush-rawat-a38335200
- https://www.linkedin.com/in/akash-bulla-211843204/

Instagram Handles :

- https://www.instagram.com/piyush_rawat.09/
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Course Name: Computer Architecture and Organization

Assignment- Week 1

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 12 **Total mark: 12 x 1 = 12**

QUESTION 1:

Which of the following is/are false?

a. Processor can directly access data from secondary memory.
b. Primary memory are used as backup memory.
c. Primary memory stores the active instructions and data for the program being executed on the processor.
d. Primary memory can store only instructions.

Correct Answer: a, b and d

Detailed Solution:

Processor have access to primary memory which stores data and instructions for the program being executed. The secondary memory is used as a backup memory. Primary memory can store both instructions and data.

Thus option (a), (b) and (c) are false.

QUESTION 2:

Program counter:

a. Counts the total number of instructions present in a program.
b. Points to the current instruction that is being executed.
c. Points to the next instruction that is to be executed.
d. Stores the data of the current instruction that is being executed.

Correct Answer: c

Detailed Solution:

Program counter is used to point to the next instruction that is to be executed by the processor.

Thus option (c) is correct.

QUESTION 3:

Which of the following is/are false?

a. Central Processing Unit (CPU) consists of Control Unit, Arithmetic Logic Unit (ALU) and Primary Memory.
b. There are broadly two types of memory, primary memory and secondary memory.
c. The arithmetic and logic operations are performed in the control unit.
d. Control Unit is a part of main memory.

Correct Answer: a, c, d

Detailed Solution:

CPU consists of ALU and Control unit. Control unit is responsible for generating the required control signals for execution of instructions and ALU performs arithmetic and logic operations.

Thus option (a),(c) and (d) are false.

QUESTION 4:

Which of the following contains circuitry to carry out operations such as addition, multiplication etc?

a. Control Unit
b. Memory Unit
c. Input/output Unit
d. None of these.

Correct Answer: d

Detailed Solution:

In computer system the computations are performed in Arithmetic and Logical unit, thus none of the options are true.

QUESTION 5:

Tow registers are initialized as R1=30 and R2 = 25. The instruction ADD R1, R2 is in memory location 2018H. If the size of an instruction is 4 byte, then after the execution of the instruction the value of PC, R1 and R2 will be.

a. PC = 2018H, R1 = 55, R2 =25
b. PC = 2018H, R1 = 55, R2 =00
c. PC = 201CH, R1 = 55, R2 =00
d. PC = 201CH, R1 = 55, R2 =25

Correct Answer: d

Detailed Solution:

ADD R1, R2 is equivalent to R1 = R1 + R2, after executing the instruction R1 will contain 55 and value of R2 will remain unchanged. PC will point the next instruction as the instruction size is 4 byte thus PC = 201CH.

Thus option (d) is correct.

QUESTION 6:

Consider a 32-bit machine where an instruction (SUB R1, LOCA) is stored at location 2004H. LOCA is a memory location whose value is 1024H. The number of memory access required to execute this instruction will be …………….?

Correct Answer: 2

Detailed Solution:

Initially, instruction is stored at location 2004H and hence, PC contains 2004H. After the instruction is fetched the PC points to next memory location. As this is a 32-bit machine PC will be incremented by 4. The steps carried out for executing this instruction is given below:

MAR	**←**	**PC / (2004H)**		
PC	**←**	**PC + 4**	**// PC = 2004 + 4 = 2008H**	
MDR	**←**	**Mem[MAR]**	**// (ADD R1, LOCA)**	**#Memory Access 1**
IR	**←**	**MDR**	**// (ADD R1, LOCA)**	
MAR	**←**	**IR[Operand]**	**// (LOCA)**	
MDR	**←**	**Mem[MAR]**	**// (Content of LOCA)**	**#Memory Access 2**
R1	**←**	**R1 + MDR**		

Therefore, we have two memory accesses.

The correct answer will be 2.

QUESTION 7:

Consider a 32-bit machine where an instruction (ADD R1, R2) is stored at memory location 2004H (in hexadecimal). What will be the value of IR and PC while the instruction is fetched and executed? Consider Individual instruction is 32-bit.

a. IR = ADD R1, R2, PC = 2004H
b. IR = 2004H, PC = ADD R1, R2
c. IR = ADD R1, R2, PC = 2008H
d. IR = 2008H, PC = ADD R1, R2

Correct Answer: c

Detailed Solution: **Initially, instruction is stored at location 2004H and hence, PC contains 2004H. The steps carried out to execution this instruction is given below:**

MAR	**←**	**PC**	**// MAR = 2004**
PC	**←**	**PC + 4**	**// PC = 2004 + 4 = 2008**

MDR ← Mem[MAR] // MDR = ADD R1, R2 which is the content of location 2004.
IR ← MDR //IR = ADD R1, R2
R1 ← R1 + R2
Therefore IR = ADD R1, R2, and PC = 2008H

Thus correct option will be (c).

QUESTION 8:

For a 512 X 32 bit memory that contains 512 locations each with 32-bit data, what will be the address (in binary) of the 389^{th} location? (Assume first location as 0)

a. 110000100
b. 110000101
c. 011000100
d. 011000101

Correct Answer: a

Detailed Solution: The first location in memory has address 0, second location has address 1, and so on. Thus,
the 389^{th} location has address 388, which is 110000100 in binary.

The correct option is (a).

QUESTION 9:

Consider the instruction XOR R3, R2. If register R1 and R2 contains value 09H and 47H respectively. What will be the value R3 after executing the instruction?

a. 4E
b. 2E
c. 3E
d. 5E

Correct Answer: a

Detailed Solution:

XOR R3, R2

R3: 0000 1001 (09)
R2: 0100 0111 (47)
R3: 0100 1110 (4E)

The correct option is (a).

QUESTION 10:

For a byte addressable computer which has 4Gigabytes of memory. If each word in the computer is 64bit. Then how many bits are needed to address a single word.

a. 29
b. 30
c. 31
d. 32

Correct Answer: a

Detailed Solution:
Address Space = 4GB = 4 x 2^{30} B = 2^{32} B
1 word = 64 bits = 8 B
We have $2^{32}/8 = 2^{29}$ words
Thus, we require 29 bits to address each word.

The correct option is (a).

QUESTION 11:

Consider the following statement and answer:

(i) In Von-Neumann architecture, instruction and data are stored in same memory module.

(ii) In Von-Neumann architecture, instruction and data access can be performed parallelly.

a. Only (i) is true.
b. Only (ii) is true.
c. Both (i) and (ii) are true.
d. Both (i) and (ii) are false.

Correct Answer: a

Detailed Solution:

In Von-Neumann architecture instructions and data are stored in same memory thus it is not possible to access both at the same time, hence only statement (i) is true.

The correct options is (a).

QUESTION 12:

Which of the following statement(s) is/are true?

a. Nibble: A collection of 4 bits
b. Word: Byte/Multiple of Bytes
c. Byte: A collection of 8-bit
d. All of these

Correct Answer: d

Detailed Solution:

Bit is a binary digit all other options are true.
Thus correct option is (d).

************END*******

Course Name: Computer Architecture and Organization

Assignment- Week 2

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 10 **Total mark: 10 x 1 = 10**

QUESTION 1:

Which of the following statement(s) is/are true for **radix** of a positional number system.

a. It represents number of unique digits, used to represent numbers.
b. It represents number of binary digits, used to represent single digit of any number system.
c. Radix of Hexadecimal number system is 4.
d. Radix of Hexadecimal number system is 16.

Correct Answer: a, d

Detailed Solution:

Radix or base represents the number of unique digits available in the number system. Hexadecimal number system have 16 unique digits (0-9) and (A-F).

The correct options are (a) and (d).

QUESTION 2:

What will be binary representation of $(3.6E)_{16}$?

a. 0011 . 0110 1111
b. 0011 . 0110 1110
c. 11 . 0110 111
d. None of these

Correct Answer: b, c

Detailed Solution:

The conversion can be done as follows:

3.6E

3 = 0011

.6E = 0110 1110

Hence, $(3.6E)_{16}$ = $(0011.0110\ 1110)_2$. However we can remove the trailing 0's and leading 0's thus one more representation will be $(11.0110\ 111)_2$.

The correct options are (b) and (c).

QUESTION 3:

What is the largest number that can be represented using 10-bit 2's complement representation ------?

Correct Answer: 511

Detailed Solution:

The range of n-bit 2's complement representation is given by $-(2^{n-1})$ to $+(2^{n-1} - 1)$. So, for n = 10 the largest number that can be represented will be $+(2^{10-1} - 1) = 511$.

QUESTION 4:

Consider the following statement for representing signed numbers using sign magnitude, 1's complement and 2's complement format:
(i) Sign of the number can be identified using MSB.
(ii) By flipping the sign bit we can obtain the number of its opposite sign.
Which of the following is correct?

a. Only (i) is true
b. Only (ii) is true
c. Both (i) and (ii) are true
d. Both (i) and (ii) are false

Correct Answer: a

Detailed Solution:

In all representation we can identify sign of the number using MSB. But by flipping the sign bit we cannot obtain the number of its opposite sign for 1's and 2's complement representation.

Thus option (a) is correct.

QUESTION 5:

Which of the following addressing modes does not require any memory access for fetching the operands?

a. Direct Addressing
b. Immediate Addressing
c. Register Indirect
d. Register Addressing
e. None of these

Correct Answer: b and d

Detailed Solution:

Immediate addressing does not require any memory access as the data is available as an operand in the instruction itself. Register addressing mode also not require any memory access as the registers are used as an operands.

Thus option (b) and (d) are correct.

QUESTION 6:

How do you represent -10 using 16-bit, 2's complement representation?

a. 1000 0000 0001 0110
b. 0000 0000 0000 1010
c. 1111 1111 1111 0110
d. 0000 0000 0001 0110

Correct Answer: c

Detailed Solution:

Firstly, the representation of +10 will be 01010.

In 16 bit +10 will be 0000 0000 0000 1010

Now, -10 = 1's Complement of 0000 0000 0000 1010 + 1

= 1111 1111 1111 0101

+ 1

= 1111 1111 1111 0110

The correct option is (c).

QUESTION 7:

For the instruction `STORE R1,35(R2)` what will be effective address of the memory operand if R2 is 200 (in decimal)?

a. 35
b. 165
c. 200
d. None of these

Correct Answer: d

Detailed Solution:

For this instruction indexed addressing mode is used, the operand 35 specifies an offset of displacement, which is added to the index register (R2) to get the effective address. The effective address will be 200 + 35 = 235. None of the options are correct.

Thus correct option is (d).

QUESTION 8:

Which of the following statement(s) is/are true for CISC architecture?

a. Supports large number of addressing modes.
b. It does not support variable-length instruction.
c. Pipeline implementation of CISC architecture is complex.
d. Only load and store instruction can access memory

Correct Answer: a, c

Detailed Solution:

Refer lecture 8: slide number 2-5 for property of CISC and RISC.

Both option (a) and (c) are true for CISC architecture.

QUESTION 9:

Which of the following instruction is/are invalid for MIPS32 processor if $s0 and $s1 contains address of some variables (say A and B).

a. add $t0, $t1, 20($s0)
b. lw $t0, 40($s0)
c. add $t0, $t0, $t1
d. None of these

Correct Answer: a

Detailed Answer:

The instruction add $t0, $t1, 20($s0) is using indirect addressing and trying to access memory location which is not valid in MIPS.

The correct option is (a).

QUESTION 10:

Consider the following MIPS instruction:

```
slt $t0, $s0, $s1
```

What does the instruction do if $s0 and $s1 is loaded with some data?

a. Set $t0 = 1 if $s0<$s1
b. Set $t0 = 0 if $s0>$s1
c. Set $t0 = 1 if $s0>$s1
d. Set $t0 = 0 if $s0<$s1

Correct Answer: a, b

Detailed Solution:

The instruction will set $t0=1 if $s0<$s1 else it will set $t0=0.

Hence, the correct options are (a) and (b).

**************END*******

Course Name: Computer Architecture and Organization

Assignment- Week 3

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 10 **Total mark: 10 x 1 = 10**

QUESTION 1:

A processor having clock cycle time of 5ns, will have a clock rate of ________ MHz.

Correct Answer: 200

Detailed Answer:

Frequency is given by the formula f = 1 / (Cycle time).

Hence, frequency = 1 / 5ns = 1 / (5×10^{-9}) = 2×10^8 Hz = 200 MHz

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QUESTION 2:

Suppose a program requires 1000 instructions to execute. The average number of cycles per instruction (CPI) is 1.5. The clock frequency of the machine is 2.0 GHz. Time required to execute the program will be _________ nanoseconds.

Correct Answer: 750

Detailed Answer:
Execution time = IC x CPI x T
IC = Instruction Count = 1000
CPI = Cycles Per Instructions = 1.5
T = Clock cycle time = 1/f = $1/2 \times 10^9$ = $.5 \times 10^{-9}$s = .5 ns

Execution Time = IC x CPI x C = 1000 x 1.5 x .5 = 750 nanoseconds.

QUESTION 3:

Consider a program whose instruction count is 1,500, average CPI is 2, and clock cycle time is 1 nanosecond. Suppose we use a new compiler on the same program for which the new instruction count is 2,500, and new CPI is 1.5, which is running on a faster machine with clock cycle time of 0.5 nanosecond. The speedup achieved will be:

a. 1.66
b. 0.63
c. 1.60
d. 1.33

Correct Answer: c

Detailed Answer:

XT for compiler_1 = 1500 x 2 x 1 = 3000ns

XT for compiler_2 = 2500 x 1.5 * 0.5 = 1875ns

Speedup = XT for compiler_1 / XT for compiler_2 = 3000 / 1875 = 1.60

The correct option is (c).

QUESTION 4:

On which of the following does CPI depend on?

a. Instruction Set Architecture
b. Complier
c. CPU organization
d. All of these

Correct Answer: d

Detailed Answer:

CPI depends on ISA, compiler as well as the CPU organization.

The correct option is (d).

QUESTION 5:

Consider the following statements:

(i) RISC architecture increases number of instructions per program.

(ii) RISC architecture increases CPI and clock cycle time.

Which of the following is correct?

a. Only (i) is true
b. Only (ii) is true
c. Both (i) and (ii) are true
d. Both (i) and (ii) are false

Correct Answer: a

Detailed Answer:
RISC architecture uses simple instructions which can lead to larger number of instructions per program, however RISC provides execution of instruction mostly in single cycle thus reduces CPI.

The correct option is (a).

QUESTION 6:

Suppose that a machine X executes a program with an average CPI of 2.5. Consider another machine Y (with same instruction set and a little better compiler) that executes the same program with 10% less instructions and with the CPI of 1.5 at 4GHz. What should be the clock frequency of X so that both the machines have same performance?

a. 7.40GHz
b. 7.40MHz
c. 7.40KHz
d. 7.40Hz

Correct Answer: a

Detailed Solution:
Given, $CPI_X = 2.5$,

$CPI_Y = 1.5$, $f_Y = 4GHz$, $T_Y = 1 / f_Y = 0.25ns$

$IC_Y = IC_X - IC_X \times 0.1 = 0.9\ IC_X$

If both machine have same performance, then we must have

$XT_X = XT_Y$

$IC_X \times CPI_X \times T_X = IC_Y \times CPI_Y \times T_Y$

$IC_X \times 2.5 \times T_X = 0.9\ IC_X \times 1.5 \times 0.25ns$

$T_X = .3375 / 2.5 = 0.135ns$

$f_X = 1 / T_X = 1 / 0.135ns = 7.40\ GHz$

The correct option is (a).

QUESTION 7:

Suppose for a CISC ISA implementation, there are four instruction types LOAD, STORE, ALU and BRANCH with relative frequencies of 25%, 25%, 40% and 10% respectively, and CPI values of 3, 2.5, 1 and 6 respectively. The overall CPI will be ____. (Provide answer up-to 2 decimal places)

Correct Answer: 2.37 to 2.38

Detailed Solution:

$CPI = \sum(F_i \times CPI_i) = 0.25x3 + 0.25x2.5 + 0.40x1 + 0.10x6 = 0.75 + 0.625 + .40 + .60 = 2.375.$

QUESTION 8:

Consider the following statements:

(i) MIPS rating is used to compare performance of two processors.

(ii) Higher MIPS rating indicates better performance.

Which of the following is correct?

a. Only (i) is true
b. Only (ii) is true
c. Both (i) and (ii) are true
d. Both (i) and (ii) are false

Correct Answer: a

Detailed Solution:

MIPS is used to compare performance of two processors; however, it is not always true that higher MIPS rating mean higher performance. Some computer may call other software routine for computation which might not be considered for evaluating MIPS rating.

The correct option is (a).

QUESTION 9:

Consider a program with 50 million instructions, a machine requires 25 milliseconds to execute this program. What will be the MIPS rating of the machine?

a. 20
b. 200
c. 2000
d. 20000

Correct Answer: c

Detailed Solution:

MIPS rating = (Instruction Count / Execution time x10^6)

= (50 x 10^6 / 25 x 10^{-3} x 10^6) = 50000/25 = 2000

The correct option is (c).

QUESTION 10:

Which of the following statements is/are true with respect to Amdahl's law?

a. It express the law of diminishing returns.
b. It provides a measure to compare execution time of two machines.
c. It expresses the maximum speedup that can be achieved.
d. All of these

Correct Answer: a, c

Detailed Solution:

Amdahl's law expresses the law of diminishing returns, which identifies maximum speedup that can be achieved if we are want to improve some part of the program.

The correct options are (a) and (c).

************END*******

Course Name: Computer Architecture and Organization

Assignment- Week 4

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 10 **Total mark: 10 x 1 = 10**

QUESTION 1:

If the instruction size of a machines is 64 bit long, which has a byte addressable memory then to point to the next instruction the PC value should be incremented by _____?

Correct Answer: 8

Detailed Solution:

In byte addressable memory each byte will have unique address, so if the instructions are 64-bit long then PC should be incremented by 8 to point to the next instruction to be executed.

The correct answer will be 8.

QUESTION 2:

During fetch operation of an instruction does CPU knows what kind of instruction is getting fetched?

a. Yes
b. No

Correct Answer: b
Detailed Solution:
The type of instruction is known at the decoding stage.
Thus option (b) is correct.

QUESTION 3:

Consider the following statement:
(i) Program Counter holds address of the memory location containing the next instruction to be executed.

(ii) Instruction Register contains the next instruction to be executed.
Which of the following is correct?

a. Only (i) is true
b. Only (ii) is true
c. Both (i) and (ii) are true
d. Both (i) and (ii) are false

Correct Answer: a
Detailed Solution:
Program counter contains the address of the next instruction to be executed and Instruction register contains the current instruction being executed.

Thus option (a) is correct.

QUESTION 4:

For single bus architecture, register Y and Z can be used only to store intermediate value?

a. True
b. False

Correct Answer: a
Detailed Solution:
In single bus architecture register Y and Z are temporary registers which cannot be used by instruction explicitly. It can only be used to store intermediate value during computation.

Thus option (a) is correct.

QUESTION 5:

Consider the following set of micro-operations for a single bus architecture machine:

Step **Action**
T1: PCout, MARin, Read, Select4, Add, Zin

T2: Zout, PCin, Yin, WMFC

T3: MDRout, IRin

T4: R3out, Yin, SelectY

T5: R4out, ADD, Zin

T6: Zout, R3in, End

The micro-operation corresponds to which instruction?

a. ADD Y, R4
b. ADD R3, Y
c. ADD R3, R4
d. MOVE R3, R4

Correct Answer: c

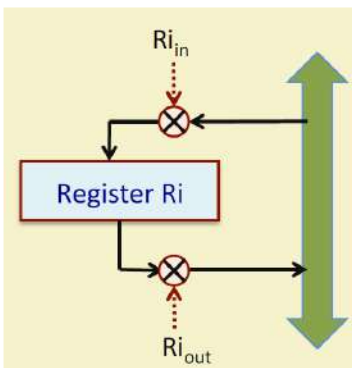
Detailed Solution:

In the first three basic steps loading instruction address to MAR, incrementing PC and loading instruction to register IR takes place. In fourth step Y is loaded with the content of R3, and in the next step ALU operation is performed which adds Y (content of R3) and content of R4. At step 6 the content of Z (result) is again stored back to register R3.

Thus option (c)is correct.

<u>QUESTION 6:</u>

Consider the following scenario where registers Ri is connected through a bus. Assume that Ri is initially loaded with data X. And in bus we have data Y.



What will happen if $Ri_{in} = 1$ is applied?

a. The content of R1 will become Y
b. Data X will be placed on the bus.

c. R1 will be loaded with Y and, bus will be loaded with X.
d. The content of R1 and Bus will be unchanged.

Correct Answer: a
Detailed Solution:
The control signal Ri_{in} indicates the input control of register Ri is activated thus content of Ri will be loaded with new value Y which is available in the BUS.

The correct option is (a).

QUESTION 7:

Which of the following statement(s) is/are true for fetching a word from memory?

a. The word can be directly loaded to general purpose registers from memory.
b. The information to be fetched, must be an instruction/operand.
c. The word can be directly transferred to ALU for further operation.
d. All of these.

Correct Answer: b

Detailed Solution:
During fetching of a word, the word is first loaded into register MDR.

The correct option is (b).

QUESTION 8:

Consider a single bus system, how many steps will be required to complete the instruction MOVE R1, R2

a. 2
b. 3
c. 4
d. 5

Correct Answer: c

Detailed Solution:

The steps to complete the operation will be as follows:

T1: PC_{out}, MAR_{in}, Read, Select4, Add, Z_{in}

T2: Z_{out}, PC_{in}, Y_{in}, WMFC

T3: MDR_{out}, IR_{in}

T4: $R2_{out}$, $R1_{in}$, END

Thus correct answer will be (c)

QUESTION 9:

Consider a hardwired control unit where each instruction of the machine requires maximum of 50 steps to complete its execution. If the total number of such instructions are 129, what should be the size of step decoder and instruction decoder respectively?

a. 6x64; 7x128
b. 50x1; 129x1
c. 64x1, 256x1
d. 6x64, 8x256

Correct Answer: d

Detailed Solution:

A decoder with n-select line can have 2^n outputs thus option b, and c, are incorrect. Option a is also incorrect as first decoder can fulfill the requirement of maximum time steps to be generated by controller; however, with second decoder we can only decode 128 instructions. Thus option (d) is correct.

QUESTION 10:

Which of the following statement(s) is/are true for micro-programed control unit?

a. The control signals are generated by circuits such as encoder, decoder etc.
b. It is flexible for modification.
c. It is used in CISC architecture.
d. All of these

Correct Answer: b, c

Detailed Solution:

In micro-programed control unit control signals are stored in memory and loaded sequentially based on instruction. It is slow as compared to hardwired control unit but provides flexibility as control signals are stored in memory that can be modified as per requirement. It is used in CISC architecture.

The correct options are (b) and (c).

**************END*******

Course Name: Computer Architecture and Organization

Assignment- Week 5

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 10 **Total mark: 10 x 1 = 10**

QUESTION 1:

Which of the following statement(s) is/are true?

a. In memory, data are stored in the form of 0's and 1's.
b. Memory system stores data and instruction.
c. Every bit of memory has a unique address.
d. All of these

Correct Answer: a, b

Detailed Solution:

Memory are used to store data and instruction. Every memory location has a unique address, however each location may allow access of multiple bit/byte/word.

The correct options are (a) and (b).

QUESTION 2:

Consider a memory with "n" address line and "m" data lines what will be the total number of bits in the memory.

a. 2^m x n
b. 2^n x m
c. 2^{n+m}
d. m^2 x n

Correct Answer: b

Detailed Solution:

The total number of bits in the memory with n address line and m data lines will be given by 2^n x m.

The correct option is (b).

QUESTION 3:

Which of the following statement(s) is/are false?

a. In volatile memory data is lost when power is switched off.
b. Dynamic memory requires periodic refreshing.
c. Magnetic tape does not allow random access of data.
d. None of these.

Correct Answer: d

Detailed Solution:

All statements are true, refer lecture 23, and slide no (5-6).

The correct option is (d).

QUESTION 4:

What is/are false for cache memory?

a. It consumes low power as compared to main memory.
b. It is a type of non-volatile memory.
c. It decrease the effective speed of the memory system.
d. All of these.

Correct Answer: d

Detailed Solution:

Cache memory is a fast memory which is used to increase the effective speed of memory system. Cache memory consumes high power as compared to main memory thus use of larger size cache is not recommended.

The correct option is (d).

QUESTION 5:

The total number of external connection required by an 8 x 8 memory will be _______?

Correct Answer: 15

Detailed Solution:

Address decoder of size 3 x 8 → 3 external connection

Data outputs 8 bit → 8 external connection

2 external connection for R/W and CS.

2 external connection for power supply and ground.

Total external connection: 3+8+2+2 = 15.

QUESTION 6:

Which of the following is/are true for virtual memory system?

a. It increases the size of the program that can be run
b. It increases the size of the physical memory
c. It increases the size of the secondary memory
d. It improves the processor-memory bandwidth

Correct Answer: a

Detailed Solution:

Virtual memory only increases the size of the program that can be run. But it does not allow by any emans to increase the size of the memory (physical or secondary). It does not have any impact on processor memory bandwidth.

The correct options is (a).

QUESTION 7:

Which of the following statement is true for writing 1 in SRAM chip?

a. The bit line b is set with 1, and bit line b’ is set with 0.
b. The bit line b is set with 0, and bit line b’ is set with 1.
c. The bit line b is set with 1, and bit line b’ is set with 1.
d. The bit line b is set with 0, and bit line b’ is set with 0.

Correct Answer: a

Detailed Solution:

To write 1 in SRAM cell, bit line b is set with 1, and bit line b' is set with 0 and to write 0 in SRAM cell bit line b is set with 0, and bit line b' is set with 1.

The correct options is (a).

QUESTION 8:

Consider a 1Mbit memory organized as 1024 (rows) and 1024 (columns). If the data bus is 16-bit wide, total number of address lines required will be:

a. 16
b. 14
c. 15
d. 20

Correct Answer: a

Detailed Solution:

The 1Mbit memory is organized as 2^{10} = 1024 rows and 2^{10} = 1024 columns, with a 16-bit wide data bus. So, the memory can be organized as (2^{10}) x (2^6 x 2^4). Therefore, total number of address lines will be 10 + 6 = 16. The correct option is (a).

QUESTION 9:

For a DDR2 SDRAM if the internal clock is 140MHz and bus clock is 350MHz, what will be the maximum data transfer rate?

a. 4.48 KB/s
b. 4.48 MB/s
c. 4.48 GB/s
d. 4.48 TB/s

Correct Answer: c

Detailed Solution:

Maximum data transfer rate for the given internal clock and bus clock will be

$(2 \times 280 \times 10^6 \times 64) / 8 = 4.48$ GB/s

The correct option is (c).

QUESTION 10:

Consider a memory chip with size 1 Gbyte. Four such chips are connected together to build a larger byte-oriented memory system using memory interleaving, where the processor data lines are 32-bits wide. If we name the four chips as M0, M1, M2 and M3, to which memory modules will the memory addresses **0542364AH** and **1A54200CH** map to?

a. M2 and M3
b. M2 and M0
c. M0 and M0
d. M0 and M1

Correct Answer: b

Detailed Solution:

The 1Gbyte memory chip will have 30 address lines, as 2^{30} = 1G.

The memory system will contain 4 such chips, and hence will have 32 address lines.

The high-order address lines A_{31}, A_{30} … A_2 will be connected to the address lines of the four chips, while the low-order two address lines will be selecting one of the four chips:

M0: $A_1 = 0, A_0 = 0$

M1: $A_1 = 0, A_0 = 1$

M2: $A_1 = 1, A_0 = 0$

M3: $A_1 = 1, A_0 = 1$

For the memory address 0542364AH, $A_1 = 1, A_0 = 0$ → M2

For the memory address 0A54200CH, $A_1 = 0, A_0 = 0$ → M0

The correct option is (b).

***********END*******

Course Name: Computer Architecture and Organization

Assignment- Week 6

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 10 **Total mark: 10 x 1 = 10**

QUESTION 1:

Which of the following statement(s) is/are true?

a. Organizing memory in multiple levels may result in faster data access.
b. As we move away from the processor the speed of memory increase.
c. By keeping commonly used data in the memory that is near to processor, memory access time may increase.
d. None of these.

Correct Answer: a

Detailed Solution:

Memory hierarchy can result in faster access time on average. As we move away from processor the speed of memory decreases, and by keeping commonly used data near to processor we can access those data quickly, and thus overall access time can be improved.

The correct options is (a).

QUESTION 2:

Consider a three-level memory hierarchy (cache - main memory - magnetic disk). Which of the following interfaces of the memory hierarchy is/are managed by operating system?

a. Cache – magnetic disk
b. Cache - Main memory
c. Main memory - magnetic disk
d. None of these.

Correct Answer: c

Detailed Solution:

For multi-level hierarchy, the interfaces between the cache and main memory are managed by hardware, whereas the interface between main memory and magnetic disk/HDD/SSD is managed by software (operating system).

The correct options is (c).

QUESTION 3:

Consider a machine which takes 2 nanosecond to fulfill a read request for cache hit and 45 nanoseconds to fulfill a read request for cache miss. If a program results in 90% of cache hit then the average read access time will be _________ nanoseconds.

Correct Answer: 2.25

Detailed Solution:

Average Access Time => Hit. T_{hit} + (1-Hit).T_{miss}

= .90 x 2 + .10 x 45 = 1.80 + .45 = 2.25 nanoseconds.

QUESTION 4:

Consider a 2-level memory hierarchy consisting of a single-level cache memory and the main memory. The access times for the cache memory and main memory are 10 nanoseconds and 100 nanoseconds respectively. If a program is using cache for 85% of the time. The speedup gain by using cache will be __________.

Correct Answer: 4.25 to 4.26

Detailed Solution:

This can be solved by Amdahl's law

The memory access time of cache is 10 (r=10) time faster than main memory and can be used for 85% (H=.85) of the time.

Speedup = 1/[(H/r) + (1-H)] = 1/[(.85/10 + .15)] = 1/(0.085 + .15) = 4.255

QUESTION 5:

Consider a main memory with 1024 blocks with block size of 32-bit each and a cache memory which consist of 128 blocks. If we use direct mapping then block 128 and 256 will be mapped to which blocks of cache memory?

a. 128,256
b. 0, 0
c. 1, 1
d. 0, 1

Correct Answer: b

Detailed Solution:

Mapping will be done as: main memory block % total cache block;

For 128^{th} block: 128 % 128 = 0^{th} block

For 256^{th} block: 256 % 128 = 0^{th} block

The correct option is (b).

QUESTION 6:

Consider a set-associative cache that consists of 256 blocks divided into 16-block sets and a byte addressable main memory of size 512Kbytes, with block size of 32 bytes each. How many bits will be there in the TAG, SET and WORD fields respectively?

a. 10, 4, 5
b. 10, 5, 4
c. 10, 5, 5
d. 10, 4, 4

Correct Answer: a

Detailed Solution:

Number of blocks in main memory: total size / block size = 512K/32 = 16K blocks.
Number of sets in cache = 256 / 16 = 16.
Since each block has 32 bytes, number of bits in WORD field = 5 bits (as 2^5 = 32)
Since there are 16 sets, number of bits in SET field = 4 (as 2^4 = 16)
Total number of bits in the address = 19 (as 2^{19} = 512K)
Hence, number of bits in TAG field = 19 – (5 + 4) = 10
The correct option is (a).

QUESTION 7:

A computer has 4 Gbyte memory with 32-bit words, where the computer uses word-level addressing. Each block of memory stores 64 words. The computer has a direct-mapped cache of 128 blocks. How many bits will be there in the TAG field?

a. 16
b. 17
c. 18
d. 19

Correct Answer: b

Detailed Solution:

Main memory size = 4GB = 4G / 4 = 1G words (as 1 word = 4 bytes).
So, total number of address lines = 30 (as 2^{30} = 1G)
Since each block is 64 words, number of bits in WORD field = 6 (as 2^6 = 64)
As there are 128 blocks in cache, number of bits in BLOCK field = 7 (as 2^7 = 128)
Hence, number of bits in TAG field = 30 – (7 + 6) = 17
The correct option is (b).

QUESTION 8:

Consider an N-way set associative memory? What will happen if we increase value of N?

a. Search time in cache will increase.
b. Freedom of mapping main memory block into cache will increase.
c. Size of set will increase.

Correct Answer: a, b, c

Detailed Solution:

Increasing the value of N means we move towards N-way set associative which will increase search time, but allow more freedom to map blocks of main memory into cache. Also the size of set will increase and the number of sets will decrease.

Thus all the options are correct.

QUESTION 9:

Consider a processor with an average CPI of 1.5, which runs a program with the following instruction mix: ALU instructions – 50%, LOAD – 25%, STORE – 10%, BRANCH – 15%. Assume that the cache miss rate is 5%, and the miss penalty is 33 cycles. What will be the effective CPI for a unified L1-cache, using write back and write allocate, assuming that the probability that the cache is dirty is 10%.

a. 1.35
b. 1.85
c. 2.45
d. 3.95

Correct Answer: d

Detailed Solution:

Average CPI = 1.5

ALU = 0.5, LOAD = 0.25, STORE = 0.10, BRANCH = 0.15, Cache Miss Rate = 0.05, Miss Penalty (t_{MM}) = 33 cycles, Cache Dirty Rate = 0.10, Cache Clean Rate = 1 – 0.10 = 0.90

Number of memory accesses per instruction = 1 + 0.25 + 0.10 = 1.35

(1 for instruction fetch, 0.25 for load, 0.10 for store)

Memory stalls / access = $(1 - H_{L1})$ (t_{MM} x % clean + 2 t_{MM} x % dirty)
= 0.05 (33 x 0.90 + 66 x 0.10)
= 1.815

Memory stalls / instruction = 1.35 x 1.815 = 2.450 cycles

Thus, effective CPI = 1.5 + 2.45 = 3.95

The correct option is (c).

QUESTION 10:

Which of the following approaches can be used for reducing cache miss rate?

a. Use larger block size
b. Use larger cache
c. Use higher associativity

Correct Answer: a, b, c

Detailed Solution:

Refer lecture 32, slide-8.

**************END*******

Course Name: Computer Architecture and Organization

Assignment- Week 7

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 10 **Total mark: 10 x 1 = 10**

QUESTION 1:

Decimal equivalent of 11101011 represented in 2's complement format will be______?

Correct Answer: -21

Detailed Solution:

Decimal equivalent of number 11101011 will be:

$-1x2^7 + 1x2^6 + 1x2^5 + 1x2^3 + 1x2^1 + 1x2^0$ ➔ -128+64+32+8+2+1 ➔-21

QUESTION 2:

Largest number that can be represented using 8-bit 1's complement representation will be_______

Correct Answer: 127

Detailed Solution:

Range of 1's complement representation is : $-(2^{n-1}-1)$ to $+(2^{n-1}-1)$, for n=8 the largest number which can be represented will be $+(2^{8-1}-1) = 127$.

QUESTION 3:

If we implement a half adder only with basic gates (AND, OR, NOT), then how many basic gates will be required?

a. 6
b. 5
c. 4
d. 3

Correct Answer: a

Detailed Solution:

The SUM and CARRY outputs of a half-adder are given by:

S = A XOR B = A'.B + A.B'

C = A.B

For SUM, 5 gates (2 AND gate, 2 NOT gate, 1 OR gate) are needed and for CARRY, 1 AND gate is needed.

The correct option is (a).

QUESTION 4:

If the delay of each basic gates is "δ", and the inputs are available in both complemented and uncomplemented forms, the total delay required by SUM and CARRY outputs of a full adder is:

a. 2 δ and 2 δ
b. 2 δ and 3 δ
c. 3 δ and 2 δ
d. 3 δ and 3 δ

Correct Answer: a

Detailed Solution: The CARRY generator circuit will take 2 δ time to produce output.

The SUM circuit will also take 2 δ time (time required for AND-OR circuit as the inputs are already available in complemented form).

Hence, the correct option is (a).

QUESTION 5:

Which of the following statement(s) is/are true for carry lookahead adder?

a. Addition can be carried out in constant time.
b. All carries can be generated in parallel.
c. The cost of carry lookahead circuit increase rapidly with increase in number of bits.
d. None of these

Correct Answer: a, b, c

Detailed Solution:

In a carry look-ahead adder, all the carries are generated in parallel, and addition can be carried out in constant time. However, carry look-ahead requires lot of extra hardware in the carry generation logic, which increases rapidly with n.

The correct options are (a), (b), and (c).

QUESTION 6:

Carry save adder consist of?

a. Cascaded full adders.
b. Independent full adders.
c. Parallel adder in the last stage.
d. Carry select adders.
e. None of these.

Correct Answer: b, c

Detailed Solution:

A carry save adder consist of independent full adders which perform addition, and a parallel adder which add the results computed by independent full adders.

The correct options are (b) and (c).

QUESTION 7:

In a 5-bit carry look-ahead adder, suppose we are adding two numbers A = (1, 0, 1, 1, 0) and B = (1, 0, 1, 1, 1). The carry generate and carry propagate signals will be:

a. G = (1, 0, 1, 1, 0) and P = (1, 0, 1, 1, 1)
b. G = (1, 0, 1, 1, 0) and P = (0, 0, 1, 0, 1)
c. G = (1, 0, 1, 1, 0) and P = (0, 0, 0, 0, 1)
d. G = (1, 0, 1, 1, 0) and P = (1, 0, 0, 0, 1)

Correct Answer: c

Detailed Solution:

The carry generate and carry propagate signals are defined as $G_i = A_iB_i$, and $P_i = A_i$ xor B_i. Hence, G = (1, 0, 1, 1, 0) and P = (0, 0, 0, 0, 1).

The correct option is (c).

QUESTION 8:

Suppose we are multiplying (-9) x (12) using Booth's multiplier, where each number is represented in 5 bits. What will be the values of A (temporary register), and Q (multiplier) after third step?

a. 00100, 00011
b. 01001, 00011
c. 00100, 10001
d. None of these.

Correct Answer: c

Detailed Solution:

Step	A	Q	Q_{-1}	M	Operation
0	00000	01100	0	10111	Initialization
1	00000	00110	0	10111	Shift A-Q-Q_{-1} right
2	00000	00011	0	10111	Shift A-Q-Q_{-1} right
3	01001	00011	0	10111	A = A-M
	00100	10001	1	10111	Shift A-Q-Q_{-1} right

QUESTION 9:

Which of the following statement(s) is/are true?

a. Booth's multiplier is faster as compared to shift and add multiplication approach
b. Booth's multiplier inspects two bits of the multiplier at every step
c. Arithmetic right shift operation is used in Booth's multiplier.
d. None of these

Correct Answer: a, b, c

Detailed Solution:

Due to inspecting two bits, Booth's multiplier makes multiplication process faster by reducing number of add/subtract operations. It uses arithmetic right shift operation for shifting temporary register and multiplicand.

The correct options are (a), (b), and (c).

QUESTION 10:

Suppose we are dividing 37/6 using restoring division method, where A and M are represented in 4 bits. What will be the value of A after the third step?

a. 0000
b. 0100
c. 1011
d. 1110

Correct Answer: b

Detailed Solution:

Step	A	Q	M	Operation
0	0000	100101	0110	Initialization
1	0001	001010	0110	Shift A-Q left
	1011	001010	0110	A = A-M
	0001	001010	0110	A = A+M, Q0=0
2	0010	010100	0110	Shift A-Q left
	1100	010100	0110	A = A-M
	0010	010100	0110	A = A+M, Q0=0

3	**0100**	**101000**	**0110**	**Shift A-Q left**
	1110	**101000**	**0110**	**A=A-M**
	0100	**101000**	**0110**	**A=A+M, Q0=0**

************END*******

Course Name: Computer Architecture and Organization

Assignment- Week 8

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 10 **Total mark: 10 x 1 = 10**

QUESTION 1:

Which of the following fractions can be represented exactly in binary?

a. 0.75
b. 0.50
c. 0.33
d. 0.66
e. 0.99
f. 0.25

Correct Answer: a, b, f

Detailed Solution:

The necessary condition that a fractional number can be represented exactly in binary is that, we should be able to express the number in the form $x/2^k$, where x is some integer. Options (c), (d) and (e) cannot be represented in the form $x/2^k$.

The correct options are (a), (b), and (f).

QUESTION 2:

For any binary number shifting the fraction point left by 2 position is equivalent to?

a. Dividing value by 4
b. Multiplying value by 4
c. Adding 2
d. Subtracting 2
e. None of these.

Correct Answer: a

Detailed Solution:

Shifting the fraction point left by two position is equivalent to division by 4.

QUESTION 3:

For a single precision floating point number representation in IEEE-754 format, how many bits are used to represent mantissa?

a. 23
b. 24
c. 8
d. 127
e. None of these

Correct Answer: a

Detailed Solution:

In a single-precision floating-point number representation, 23 bits are used to represent mantissa.

The correct option is (a).

QUESTION 4:

Consider a floating point representation with 39-bit mantissa (including the implied bit), the number of significant digit in decimal will be__________

Correct Answer: 11 or 12

Detailed Solution:

For 39-bit mantissa, let y denotes the number of equivalent digits in decimal.

We can write, $2^{39} = 10^{y}$

Or, $39 \log_{10} 2 = y \log_{10} 10$

Or, $y = 11.74$ → 11 to 12 significant digits in decimal.

QUESTION 5:

The interpretation of the single precision floating point number 1000 0000 0001 1111 0000 0000 0000 1111 represented in IEEE-754 format will be:

a. 0
b. Very close to 0

c. Not a number
d. Infinity

Correct Answer: b

Detailed Solution:

As the E is all 0 and M is not equal to 0 the number will be close to 0.
The correct option is (b)

QUESTION 6:

Consider the following statements:
(i) IEEE-754 floating point representation requires shifting of mantissa for multiplication and division operation.
(ii) Shifting of mantissa affects exponent value of the number.

Which of the following statement is correct?

a. Only (i) is true
b. Only (ii) is true
c. Both (i) and (ii) are true
d. Both (i) and (ii) are false.

Correct Answer: b

Detailed Solution:

Alignment of mantissa is required only for addition and subtraction operation.
When we shift the mantissa, the exponent has to be modified at the same time to keep the value of the number as same.
The correct option is (b).

QUESTION 7:

What is required if we shift the mantissa left by 3 positions to normalize a number represented in IEEE754 format?

a. We have to decrement Exponent by 3
b. We have to increment Exponent by 3
c. We have to decrement Exponent by 2^3

d. We have to increment Exponent by 2^3

Correct Answer: a

Detailed Solution:

For normalization shifting of mantissa is done, shifting of mantissa is directly related to exponent value. For 3 left shift we require to decrease the value of E by 3.

The correct options is (a).

QUESTION 8:

Consider a 6-stage pipeline with stage delays of 45, 20, 15, 42, 23 and 20 nanoseconds respectively. Ignoring the delay of the latches between stages, the total time required to process 1500 sets of data in the pipeline will be ………. microseconds. (Provide your answer up-to two decimal places)

Correct Answer: 67.72 to 67.73

Detailed Solution:

The minimum clock period T = (delay of slowest stage) = 45 nsec.

Total time required to process 1500 data sets is given by

((6 – 1) + 1500) x 45 nsec = 67725 nsec = 67.725 microseconds.

QUESTION 9:

Consider the following reservation table:

	1	2	3	4	5	6	7	8
S_1	X				X			X
S_2		X				X		X
S_3			X			X		

In the reservation table multiple X in a row represents:

a. Repeated use of the same stage in different cycles
b. Extended use of a stage for more than one cycle
c. Parallel use of stage in same cycle

d. None of these.

Correct Answer: a

Detailed Solution:

In reservation table rows represents time step and column represents stages of function.

Thus, multiple X in rows shows use of same stage in different cycles.

The correct options is (a).

QUESTION 10:

For the following reservation table of an 8-stage pipeline, what will be the minimum average latency?

	1	2	3	4	5	6	7	8
S_1	X				X			X
S_2		X				X		X
S_3			X			X		

a. 5.0 clock cycles
b. 4.5 clock cycles
c. 8.0 clock cycles
d. 1.0 clock cycles

Correct Answer: b

Detailed Solution:

The forbidden latencies are 2, 3, 4, 6, and 7.

The possible latency cycles are:

(1, 8) = (1, 8, 1, 8, ...) ➔ average latency = (1+8)/2 = 4.5
(5) = (5, 5, 5, ...) ➔ average latency = (5+5)/2 = 5.0

The minimum average latency = 4.5

The same result can be obtained by constructing the state diagram of permissible latencies, and determining the cycle with minimum average latency.

The correct option is (b).

**************END********

Course Name: Computer Architecture and Organization

Assignment- Week 9

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 10 **Total mark: 10 x 1 = 10**

QUESTION 1:

Consider a hard disk that is rotating with a speed of 9500 rpm. The maximum rotational delay or latency will be ………… milliseconds? (Give answer correct up-to two decimal places).

Correct Answer: 6.31 to 6.32

Detailed Solution:

The disk makes 9500 revolutions in 1 minute = 60 sec
So, it will make 1 revolution in 60 / 9500 sec = 60 x 1000 / 9500 msec = 6.315 msec

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QUESTION 2:

Which of the following memory devices cannot be used for backup (or as a secondary storage device)?

a. DRAM
b. SRAM
c. Floppy Disk
d. Hard Disk
e. Flash Memory

Correct Answer: a, b

Detailed Solution:

DRAM and SRAM are volatile memories which retains data until power supply thus cannot be used as secondary storage.

The correct options are (a) and (b).

QUESTION 3:

Which of the following statement(s) is/are true for hard disk?

a. It is faster than Solid-state drives.
b. Sector is the smallest unit of data transfer.
c. It does not have any moving parts.
d. It is volatile in nature.
e. None of these.

Correct Answer: b

Detailed Solution:

Hard drives are slower as compared to soli- state drive; there is the moving part (viz. head) which is used for reading and writing data. The hard disk surface is divided into tracks, and tracks are further divided into sectors, which is the smallest unit of data transfer. Also, as it is a secondary storage device it holds non-volatile property.

The correct options is (b).

QUESTION 4:

Consider a hard disk with 2 double sided platters, 2500 tracks per surface, 200 sectors per track, and sector size of 1024 bytes. The total capacity of the disk will be ………………. Giga bytes. (Assume 1024 = 1K)

Correct Answer: 1.90 to 1.91

Detailed Solution:

Bytes/Track = 200*1024 = 200K
Bytes/Surface = 200K * 2500 = 500000K
Total Capacity = 4*500000K = 2000000K → 1.907 GB

QUESTION 5:

Which of the following operation is used to read a bit from floating gate transistor?

a. Apply read voltage at control gate and measure drain current.
b. Apply read voltage at control gate and measure source current.
c. Apply read voltage at floating gate and measure drain current.
d. Apply read voltage at floating gate and measure source current.

Correct Answer: a

Detailed Solution:

Drain is used to read value in floating point transistor, for which first a voltage Vread is applied at control gate and the current value at drain is measured.

The correct options is (a).

QUESTION 6:

Which of the following statement(s) is/are true for I/O device interfacing?

a. An input port is implemented using a tri-state bus driver.
b. An input port is implemented using a parallel-in parallel-out register.
c. An output port is implemented using a tri-state bus driver.
d. An output port is implemented using a parallel-in parallel-out register.

Correct Answer: a, d

Detailed Solution:

For I/O device interfacing, an input port is implemented using a tri-state bus driver, whereas an output port is implemented using a parallel-in parallel-out register. An output port is used to interface output devices.

The correct options are (a) and (d).

QUESTION 7:

Which of the following is/are true for I/O mapped device interfacing?

a. Separate address decoder is used to select memory and I/O ports.
b. Some of the memory address space is occupied by I/O devices.
c. Same instructions for memory and I/O operations.
d. All of these,

Correct Answer: a

Detailed Solution:

In I/O mapped device interfacing, we make distinction between memory locations and I/O ports, and separate processor instructions are used for read/write operations in memory and I/O device. Also, the separate address decoder is used to select memory modules and I/O ports.

The correct options is (a).

QUESTION 8:

Assume that we are executing some program P1, during the execution some interrupts are generated which are listed. Mark the interrupt types which allow the instruction being executed to be completed before handling it.

a. Timer interrupt
b. Page fault interrupt
c. I/O interrupt
d. All of these.

Correct Answer: a, c

Detailed Solution:

I/O interrupt and Timer interrupt can be handled after finishing the execution of the current instruction. However, page fault occurs when some requested data is not found in memory, which makes it necessary to re-execute the instruction after handling the interrupt.

The correct options are (a) and (c).

QUESTION 9:

Which of the following statement(s) is/are true for data transfer techniques?

a. Interrupt-driven technique transfers data faster than DMA mode of data transfer.
b. Asynchronous data transfer can be used for high-speed devices.
c. Interrupt-driven data transfer wastes more CPU time than asynchronous data transfer.
d. None of these

Correct Answer: d

Detailed Solution:

DMA provides fastest data transfer rate as compared to other data transfer techniques, asynchronous data transfer mode cannot be used for high speed devices as it waste lots of cpu time for checking device status after sending some blocks of data. Also, interrupt-driven transfer is faster than asynchronous data transfer. None of the statements are true.

The correct options is (d).

QUESTION 10:

Synchronous data transfer mode can be used for keyboard?

a. Yes
b. No

Correct Answer: b

Detailed Solution:

Synchronous data transfer mode cannot be used to interface keyboard as it allows data transfer at fixed speed only, but we cannot assure that the end user who is typing through keyboard will do so at the same speed.

The correct option is (b).

***********END*******

Course Name: Computer Architecture and Organization

Assignment- Week 10

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 10 **Total mark: 10 x 1 = 10**

QUESTION 1:

Consider the following statement:
(i) In programmed I/O several instructions are executed for transfer of each word of data.
(ii) Programmed I/O is not suitable for high-speed data transfer.
Which of the following is correct?

a. Only (i) is true.
b. Only (ii) is true.
c. Both (i) and (ii) are true.
d. Both (i) and (ii) are false.

Correct Answer: c

Detailed Solution:

Programmed I/O is not suitable for high-speed data transfer due to the following reason:

i) **Several program instructions have to be executed for each data word transferred between the I/O device and memory.**
ii) **Many high-speed peripheral devices like disk have a synchronous mode of operation, where data are transferred at a fixed rate. This sustained data transfer rate is comparable to the memory bandwidth and cannot be handled by programmed I/O.**

The correct options is (c).

QUESTION 2:

Consider a programmed I/O system where 20 instructions are required to be executed for the transfer of each word of data. The cycles-per-instruction (CPI) of the machine is 1.5 and the processor clock frequency is 2 GHz. The maximum data transfer rate will be ___________ million words per second. (Assume 1 million = 10^6)

Correct Answer: Range 66.00 to 67.50

Detailed Solution:

Time required for each word transfer = 20 * 1.5 * 1 / (2 x 10^9) = 15 nsec

So, maximum data transfer rate = 1 / (15 x 10^{-9}) = 66666666.666 = 66.67 million words per second.

QUESTION 3:

Which of the following statement(s) is/are true for DMA data transfer?

a. Data transfer requires very less CPU intervention.
b. Suitable for transferring large blocks of data
c. Allow direct data transfer between I/O and memory.

Correct Answer: a, b, c

Detailed Solution:

DMA mode of data transfer allows direct data transfer between I/O device and memory. It only requires CPU intervention at start and at the end, thus suitable for transferring large blocks. All the statements are true.

The correct options are (a), (b) and (c).

QUESTION 4:

Suppose the rotating speed of disk is 36000 rpm, with average rotational delay of 10 msec, suppose there are 512 Kbytes of data recorded in every track. Once the disk head reaches the desired track, the sustained data transfer rate will be ………. Mbyte/sec.

Correct Answer: Range 51.10 to 51.30

Detailed Solution:

Data transfer rate will be 512KB / 10msec = 51.2 MBps

QUESTION 5:

Which of the following registers needs to be initialized before transfer of any data in DMA mode?

a. Memory address
b. Word count
c. Address of data on disk
d. None of these.

Correct Answer: a, b, c

Detailed Solution:

For every DMA channel, the DMA controller will have three registers: Memory address, Word count, Address of data on disk which are initialized by CPU before each DMA transfer operation.

QUESTION 6:

Consider the following statements for Bus implementation:
(i) Bus width defines number of wires available in the bus for transferring data.
(ii) Bus bandwidth defines the total amount of data that can be transferred over the bus per unit of time.

a. Only (i) is true
b. Only (ii) is true
c. Both (i) and (ii) is true
d. Both (i) and (ii) are false

Correct Answer: c

Detailed Solution:

Both the statements are true, as bus width = number of wires available and bus bandwidth indicates total amount of data that can be transferred over the bus per unit of time.

The correct option is (c).

QUESTION 7:

Consider a matrix keyboard consisting of 256 keys, organized as 16 rows and 16 columns. How many port lines will be required to interface the keyboard?

a. 256
b. 128
c. 64
d. 32

Correct Answer: d

Detailed Solution:

If the keyboard is organized in a matrix format the number of port lines required will be the sum of the number of rows and number of columns.

Here, 16 + 16 = 32

The correct option is (d).

QUESTION 8:

Suppose that it is required to transfer 20K bytes in interrupt-driven mode of data transfer. Every time an interrupt occurs, it involves the transfer of 64 bytes of data that takes 20 microseconds for the processor to service. The time required to transfer 20K bytes of data will be ……………… milliseconds? (Assume 1K = 1024)

Correct Answer: 6.35 to 6.45

Detailed Solution:

To transfer 64 Bytes of data, we require 20 microseconds.
So, to transfer 1 byte of data, we require 20 / 64 = 0.3125 microseconds.
So, to transfer 20K bytes of data, we require 20K * 0.3125 microseconds = 6400 microseconds = 6.4 milliseconds.

QUESTION 9:

Which of the following is/are advantage of serial bus over parallel bus?

a. Low implementation cost
b. High speed
c. No interference
d. All of these

Correct Answer: a, c

Detailed Solution:

The advantage of serial bus connection is the implementation cost of serial bus is very low and does not produce any interference, but transfer speed is slow.

The correct options are (a) and (c).

QUESTION 10:

The maximum data transfer rates supported by USB 1.1 and USB 3.0 standards are respectively:

a. 12 Gbps and 50 Gbps
b. 12 Mbps and 5 Gbps
c. 5 Gbps and 10 Gbps
d. 2 Gbps and 10 Gbps

Correct Answer: b

Detailed Solution:

The maximum data transfer rates supported by various USB versions are:

USB 1.1	**Up to 12Mbps**
USB 2.0	**Up to 480Mbps**
USB 3.0	**Up to 5Gbps**
USB 3.1	**Up to 10Gbps**

The correct option is (b).

************END*******

Course Name: Computer Architecture and Organization

Assignment- Week 11

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 10 **Total mark: 10 x 1 = 10**

QUESTION 1:

Consider a 5-stage instruction pipeline with stage delays of 20 nsec, 25 nsec, 35 nsec, 30 nsec, and 22 nsec respectively. The delay of an inter-stage register stage of the pipeline is 2 nsec. The total time required for the execution of 1000 instructions will be ……… microseconds.

Correct Answer: 37.10 to 37.20

Detailed Solution:

Pipeline clock period T = max. {20, 25, 35, 30, 22} + 2 nsec = 35 + 2 = 37 nsec

Number of stages k = 5

Total time required = ((k – 1) + 1000) * 37 nsec

= (4 + 1000) * 37 nsec = 37148 nsec

= 37.148 microseconds

QUESTION 2:

Consider a 3-stage instruction pipeline with stage delays of 25 nsec, 30 nsec and 15 nsec respectively, and the delay of an inter-stage register stage of 5 nsec. Suppose the pipeline is modified by splitting the 1st stage into two simpler stages with delays 10 nsec and 15 nsec, and 2nd stage into two simpler stages with delays 15 nsec and 15 nsec. For the execution of 1000 instructions, the speedup of the new 5-stage pipeline over the previous 3-stage pipeline will be _________.

Correct Answer: 1.70 to 1.80

Detailed Solution:

For the 3-stage pipeline:

Pipeline clock period T1 = 30 + 5 = 35 nsec

Number of stages k1 = 3

Time required = ((3 – 1) + 1000) * 35 nsec = 35.07 microseconds

For the 5-stage pipeline:

Pipeline clock period T2 = 15 + 5 = 20 nsec
Number of stages k2 = 5
Time required = ((5 – 1) + 1000) * 20 nsec = 20.08 microseconds

Hence, the speedup = 35.07 / 20.08 = 1.746

QUESTION 3:

Consider a non-pipelined CPU working at 1GHz clock. The frequency of ALU operations, branches and memory operations are 50%, 25% and 25% respectively. If ALU and memory operations take 4 cycles and branch operation takes 7 cycles, the average instruction execution time will be ……….. nsec.

Correct Answer: 4.70 to 4.80

Detailed Solution:

Clock period = 1 nsec
Average execution time = 1ns x (.5*4 + .25*7 + .25*4) = 4.75 nsec.

QUESTION 4:

Which of the following statement(s) is/ are true?

a. Pipeline hazards prevent pipeline from operating at its maximum possible speed.
b. Data hazard arise due to resource conflicts.
c. Control hazard arise due to branch and other instructions that change the PC.
d. All of these.

Correct Answer: a, c

Detailed Solution:

Ideally pipeline implementation can complete execution of an instruction in every clock cycles, but the hazards such as data dependency between instructions, branching instructions etc. prevents pipeline implementation to achieve its top speed. Data hazard arise due to data dependencies between instructions and control hazard arise due to branch and other instructions that change the PC.

Thus options (a) and (c) are true.

QUESTION 5:

Consider a non-pipelined processor with a clock rate of 4 GHz and average cycles per instruction of 10. The same processor is upgraded to a 6-stage pipelined processor but due to the internal pipeline delay, the clock rate is reduced to 2 GHz. Assume there are no stalls in the pipeline. The speed up achieved in this pipelined processor will be ....

Correct Answer: 4.9 to 5.1

Detailed Solution:

For non-pipelined processor:

Cycle time = 0.25 nsec

Thus single instruction will execute in 10 * 0.25 = 2.5 nsec

For pipelined processor:

Cycle time = 0.5nsec

Thus single instruction will execute in 1*.5 = 0.5 nsec

(As there are no stalls; ideally each instruction will be executed in single clock)

Speedup = 2.5/0.5 = 5

QUESTION 6:

Consider the execution of following instructions in a 5-stage MIPS pipeline (IF, ID, EX, MEM, WB):

1: ADD R2, R5, R8

2: MUL R1, R4, R5

3: SUB R9, R2, R6

4: ADD R1, R5, R6

The **Read After Write** (RAW) data dependency exist between which pair of instructions that can lead to data hazard?

a. 1 and 2
b. 1 and 3

c. 2 and 3
d. 2 and 4

Correct Answer: b

Detailed Solution:

The dependency exist between instruction 1 and 3 is RAW data dependency (instruction 3 should not read the content of R2 before the correct value is written by instruction 1).

Thus the correct option is (b).

QUESTION 7:

For the following MIPS32 program segment, how many stall cycles will be required ……….?

1: LW R5, 200(R2)

2: ADD R1, R6, R8

3: SUB R3, R5, R8

Correct Answer: 0

Detailed Solution:

Between instructions (1, 2) and (2, 3), there is no data dependency. Between instructions (1, 3) there is a data dependency, but the instructions are separated by 2 units. Hence there will be no hazard.

QUESTION 8:

Which of the following data hazards can cause performance degradation in the MIPS32 integer pipeline?

a. WAR data hazard.
b. WAW data hazard.
c. RAW data hazard.
d. Memory load followed by use of the loaded data.

Correct Answer: c, d

Detailed Solution:

For MIPS32 integer pipeline, only RAW hazard can affect the pipeline performance. WAR and WAW hazards are not possible in the integer pipeline.

Thus, options (c) and (d) are correct.

QUESTION 9:

Consider the MIPS32 pipeline with ideal CPI of 1.5. Assume that 30% of all instructions executed are branch, out of which 90% are taken branches. The pipeline speedup for (i) predict taken and (ii) predict not taken approaches to reduce branch penalties will be approximately:

a. 3.94, 3.85
b. 4.34, 4.29
c. 3.85, 4.34
d. 3.85, 3.94

Correct Answer: d

Detailed Solution:

For predict-taken:

Branch penalty = 1
Speedup = 5 / (1 + 0.3x 1) = 3.846

For predict-not-taken:

Branch penalty = 1
Speedup = 5 / (1 + 0.30 x 0.90) = 3.937

The correct option is (d).

QUESTION 10:

In a MIPS pipeline with Branch Target Buffer (BTB), assume that 85% of the branches are found in BTB, 15% of the predictions are incorrect, and 75% of the branches are taken. The branch penalty will be ………… clock cycles.

Correct Answer: 0.49 to 0.53

Detailed Solution:

Branch penalty = (% Branches found in BTB x % Miss Predictions x 2)
+ (% Branches not found in BTB x % Taken branches x 2)

+ (% Branches not found in BTB x % Not-taken branches x 1)

= (0.85 x 0.15 x 2) + (0.15 x 0.75 x 2) + (0.15 x 0.25 x 1) = 0.255 + 0.225 + 0.0375 = 0.5175 clock cycles.

**************END*******

NPTEL Online Certification Courses

Indian Institute of Technology Kharagpur

Course Name: Computer Architecture and Organization

Assignment- Week 12

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 8 **Total mark: 8 x 1.25 = 10**

QUESTION 1:

In MIPS32 floating-point extension, for double-precision operations the register pair <F14, F15> is referred as:

a. F15
b. F14
c. F13
d. F12
e. None of these

Correct Answer: b

Detailed Solution:

For double-precision operations, 64-bit register pairs are used to store the operands and also the result. For this purpose we require to pair two 32-bit registers to hold 64-bit values. In this case register pair <F14, F15> is also referred to as F14.

Thus, option (b) is correct.

QUESTION 2:

Consider the given floating-point instruction:

L.D F2, 400(R6)

The data from location [R6+400] and [R6+404] will be loaded to which of the following registers?

a. F1, F2
b. F2, F3
c. F3, F2
d. None of these

Correct Answer: b

Detailed Solution:

For double-precision operations, the data are loaded in register pairs, F2 actually refers to the register pair <F2, F3>. The data from location R6+400 and R6+404 will be loaded into registers F2 and F3 respectively.

Thus, option (b) is correct.

QUESTION 3:

Which of the following techniques can be used to improve the CPI?

a. Sequencing unrelated instructions
b. Separating related instructions
c. Loop unrolling
d. None of these

Correct Answer: a, b, c

Detailed Solution:

By identifying related and unrelated instructions we can make sequence of unrelated instructions that can be overlapped without causing hazard. Similarly, we can separate related instructions by appropriate number of clock cycles to avoid hazards. With this we can exploit parallelism which can lower the CPI. Replicating the body of the loop multiple times using loop unrolling can reduce loop-overhead "per iteration".

Thus, options (a), (b) and (c) are correct.

QUESTION 4:

Which of the following statement(s) is/are false for superscalar MIPS32 machine?

a. It can issue multiple independent instructions every clock cycle.
b. It can result in a CPI of less than 1.
c. It can dynamically check dependency between instructions.
d. It consists of more than one functional units that can run in parallel
e. None of these.

Correct Answer: e

Detailed Solution:

Superscalar machine identifies the dependency between instructions and issue multiple independent instruction into multiple functional units in single clock which results CPI less than 1. The dependency among instructions is checked dynamically by the hardware. All the options are true.

Thus option (e) is correct.

QUESTION 5:

Loop unrolling requires significantly greater number of registers?

a. True
b. False

Correct Answer: a

Detailed Solution:

Loop unrolling consists of replicating the body of a loop such that more instruction level parallelism can be exposed. However, the number of registers required increases significantly.

Thus, option (a) is correct.

QUESTION 6:

Which of the following is/are advantage of vector processor?

a. It gives good speedup when we carry out similar operations on vectors.
b. No loop overhead.
c. The number of instructions gets reduced.
d. None of these.

Correct Answer: a, b, c

Detailed Solution:

A vector processor reduces the number of instructions that are executed, as a single high-level instruction can represent an entire loop; also it reduces loop overheads. A similar operation for all numbers can be performed in fewer cycles.

Thus, options (a), (b) and (c) are correct.

QUESTION 7:

In a vector processor, suppose that the start-up time of vector multiply operation is 20 clock cycles. After start-up, the initiation rate is 5 clock cycles. The number of clock cycles required per result for a 128-element vector will be _______________

Correct Answer: 5.13 to 5.17

Detailed Solution:

clock cycles required per result for a vector operation of length n

= Total time / Vector length = (Start-up Time + (n x Initiation Rate))/ Vector length

= (20 + (128 * 5))/128 = 5.156

QUESTION 8:

Which of the following statement(s) is/are false for various types of multi-core processors?

a. In asymmetric multi-core system, all the cores are identical.
b. In symmetric multi-core system, different cores may have different functionalities.
c. In a tightly coupled multiprocessor all the processors have access to a common shared memory.
d. None of these.

Correct Answer: a, b

Detailed Solution:

In asymmetric multi-core system, different cores may have different functionalities. Whereas in symmetric multi-core system, all the cores are identical. In a tightly coupled multiprocessor, there are multiple processors that have access to a common shared memory. The processors communicate among themselves through the shared memory.

Thus, options (a) and (b) correct.

************END*******