EE287 Spring 2019 Project

A simple Spread Spectrum Correlator

V 0.0001

This semester, you are designing a simple spread spectrum correlator. The correlator is used to recover a signal that has been spread with a Gold Code using phase shift keying. The project requires you to build a unit that runs at 333Mhz, can accept a base band sample every clock, and produces a correlation output. The block has 4 registers. A 10 bit Gold code is used. For more information on Gold Codes, refer to a web page https://natronics.github.io/blag/2014/gps-prn/ The output from the Gold Code is either a 1 or 0. The correlation is performed by adding the input sample when the Gold code is a 1, and subtracting when it is a zero. After processing all samples for the code length (1023 chips), the correlation value is output, The correlator sum cleared, and the process continues. The Gold code progresses at a 'chipping' rate. This rate need not be the sample rate of the system. (Possibly at 333MHz).

A DDS (Direct Digital Synthesis) system is used to provide a phase and frequency for determining when the Gold code should be advanced. This works by adding a 32 bit frequency value to a 32 bit accumulator. Whenever the accumulator is > 100,000,000, subtract 100,000,000 and advance the Gold code to the next chip. The accumulator is initialized to the phase when a sync signal is received.

There are multiple gold codes. The gold codes are described in the literature with the low order bit being indexed with '1'. Make sure you take care of this if your variables have a low order bit of 0.

A register is used to indicate which Gold code should be used to generate the chip values. The two PRN registers are initialized to all 1's at sync time.

Address	What	Comment
0	Freq	32 bit value. Set to 0 if > 100,000,000
4	Phase	32 bit value. Set to 0 if > 100,000,000
8	S1	Selects second polynomial bit for final chip xor. If outside the range 1-10, set to 1
12 (0xC)	S2	Selects second polynomial bit for final chip xor. If outside the range 1-10, set to 1

The block has the following interfaces

Name	**Bits**	**Dir**	**Description**	**Notes:**
clk	1	In	Rising edge clock	333Mhz
reset	1	In	Active High Reset	Reset all Flip Flops

Name	Bits	Dir	Description	Notes:
Din	32	In	Data input bus	Not all bits used
Dout	32	Out	Data output bus	Read of the selected register. Always reads, no strobe required
addr	4	In	Selects register	Sub portion of larger bus address
strobe	1	In	Write a register	High when a register should be written
samp	12	In	Sample value from ADC	2’s complement
push_samp	1	In	Valid sample present	Not always high
sync	1	In	Sync gold code	Syncs the Gold code, and the DDS. Gold code to all 1’s in both PRNs DDS accumulator to phase. May occur with a push_samp, or alone
push_corr	1	Out	Push out of correlation result	At the end of the last sequence, beginning of the next sequence.
corr	32	Out	Correlation sum	12 bit samples, but may be sampled many times per chip. Resulting in a larger result.

Notes:

A general discussion of spread spectrum communications may be found at
http://www.sss-mag.com/pdf/Ss_jme_denayer_intro_print.pdf