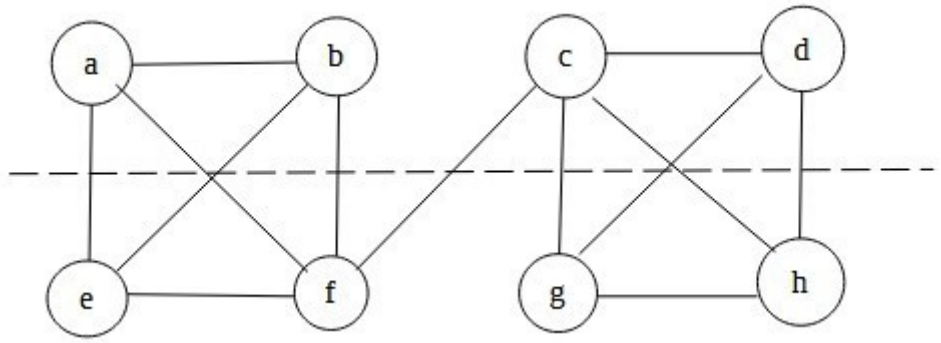
(c) Solve the KL algoritm



- For first iteration

Initial cut cost = 9
Number of No fixed points = a , b , c , d , e , f , g , h

D value of each node :
$D_x=E_x - I_x$

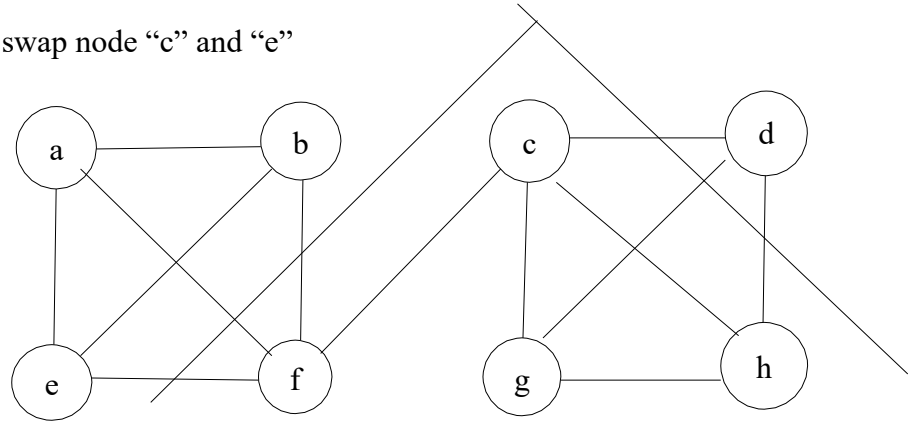
$D_a = 1$
$D_b = 1$
$D_c = 2$
$D_d = 1$
$D_e = 1$
$D_f = 2$
$D_g = 1$
$D_h = 1$

Now Compute Gain of each node

$G_{ae} = 1+1 - 2*1 = 0$	$G_{af} = 1+2 -2*1 =1$	$G_{ag} = 1+1-2*0= 2$	$G_{ah} = 1+1-2*0= 2$
$G_{be} = 1+2 - 2*1 = 0$	$G_{bf} = 1+2 -2*1=1$	$G_{bg} = 1+1 - 2*0=2$	$G_{dh}= 1+1-2*0= 2$
$G_{ce} = 2+1 – 2*0 =3$	$G_{cf} = 2+2 -2*1=2$	$G_{cg} = 2+1- 2*1= 1$	$G_{ch} = 2+1 -2*1=1$
$G_{de} = 1+1 – 2*1 =2$	$G_{df} = 1+2 – 2*0=3$	$G_{dg} = 1+1 – 2*1=0$	$G_{dh} =1+1 -2*1=0$

Gain of the G_{ce} and G_{df} is max so we can swap anyone of the two numbers

Lets swap node “c” and “e”



- Now second iteration

Cut cost = 6
Number on no fixed points = a, b , d , f, g , h

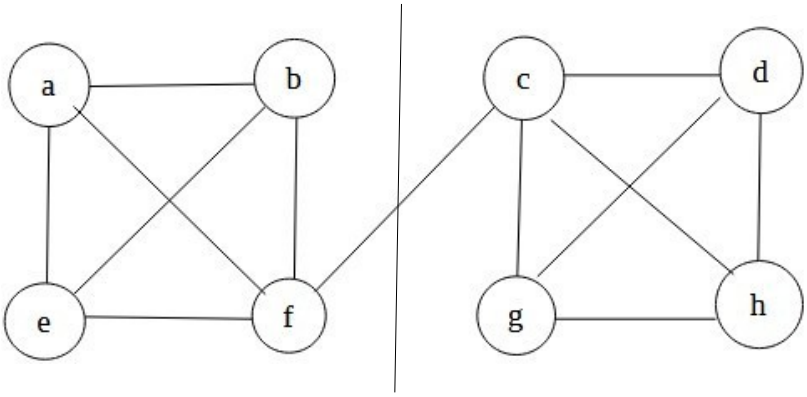
Now updated D value of the graph

D_a' = -1
D_b' = -1
D_d' = 3
D_f' = 2
D_g' = -3
D_h'= -1

Now calculate the gain of the nodes

G_{fd} = 2+3-2*0 =5

We got max max gain by swapping the node “f” and “d”



- Now for the third iteration

Cut cost = 1
Number of no fixed points = a , b, g , h

Hence we got the most optimized graph with cut cost of 1 and Gain(G) = 8

	IIT Bombay	IIT Indore
VLSI Testing and Verification	Scope of testing and verification in VLSI design process. Issues in test and verification of complex chips, embedded cores and SOCs. Fundamentals of VLSI testing. Fault models. Automatic test pattern generation. Design for testability. Scan design. Test interface and and boundary scan. System testing and test for SOCs. Iddq Description testing. Delay fault testing. BIST for testing of logic and memories. Test automation.Design verification techniques based on simulation, analytical and formal approaches. Functional verification. Timing verification. Formal verification. Basics of equivalence checking and model checking. Hardware emulation.	**Unit 1**: Scope of testing and verification in VLSI design process. Issues in test and verification of complex chips, embedded cores and SOCs. **Unit 2**: Fundamentals of VLSI testing, Fault models, Automatic test pattern generation. **Unit 3**: Design for testability, Scan design, Test interface and boundary scan, System testing and test for SOCs, Iddq testing, Delay fault testing, BIST for testing of logic and memories, Test automation. **Unit 4**: Design verification techniques based on simulation, analytical and formal approaches. Unit 5: Functional verification, Timing verification, Formal verification, Basics of equivalence checking and model checking, Hardware emulation.