Modelling Heat Transfer in Electronic Devices

B.Tech. Project Report

by

Harshit Paramhans, Vishnu Meena

170030018, 170030008

Faculty Adviser

Dr. Ponnulakshmi V.K.

School of Mechanical Sciences

Indian Institute of Technology Goa

Declaration

I declare that this written submission represents my ideas in my own words and where others' ideas or words have been included, I have adequately cited and referenced the original sources.

I understand that any violation of the above will be cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

_____

(Signature)

_____

(Name of the student)

_____

(Roll No.)

Date: _____

Abstract

The current shift in the electronic industry is towards miniaturization of electronic components. Miniaturisation of electronic components has made it possible to build small portable and handheld computer devices that can be carried almost anywhere and at any time. As a result, smaller and lighter devices having high processing capacity are available on the market.

High processing speed, AI technology requires density packaging. It has resulted in a large amount of heat generation. As a result of it, Temperature of electronic equipment increases very much which is critical for high performance and can lead to failure of electronic equipment. Conventional cooling techniques are not much efficient in thermal management of these chips. So new methods for thermal management of electronic equipment have been developed. One of those is cooling by Peltier Cooler.

This report focuses on thermal management of an electronic chip by Peltier cooler. This chip was developed by Dr. NandaKumar's group, School of Electrical Sciences, IIT Goa. We modelled the geometry of chip in Ansys using Design Modeller. We performed two simulations in ANSYS on the whole setup. One simulation was performed in the Steady State Thermal Module without giving current to Peltier. Another simulation was performed in Thermal-Electric Module with input current of 4 Ampere to Peltier.

Contents

List of Figures

List of Tables

Chapter 1: Introduction

1.1 Background

All electronic components are subject to failure due to overheating. It reduces the lifespan of electronic devices. This rise in temperature can be due to increase in ambient temperature of the environment, heat production by the device itself and the device's heat removing efficiency. There is no denying the fact that recent trends are towards reducing the size and weight of electronic chips to increase the processing speed. It has been made possible due to technological advancement in circuit components, density packing and miniaturization of modern electronics. But this miniaturization comes at the cost of increased power consumption and heat generation within the system. This high heat generation has severe effects on the device's performance and user's health; Consumers are more exposed to the effects when they are required to use electronic devices closer to their bodies (for example - mobile phones, VR headsets etc.). Such negative effects create the essential need for thermal management in electronic devices.

High processing speed, power, miniaturization of electronic devices, reliability has been made possible due to better thermal design and control of electronic components. Thermal design is one of the important application areas of Heat Transfer Branch. Advancement in computational power, heat transfer technology has resulted in better thermal management of electronic devices

1.2 Motivation and Research Objective

Dr. NandaKumar's group at IIT Goa developed a chip and used Peltier cooling method to keep the chip at a particular operating temperature. The chip is placed on an Aluminium slab. As aluminium has good thermal conductivity; there will be heat transfer through aluminium base. The bottom surface of the Aluminium slab will be in contact with the cold plate of Peltier Cooler. The objective of this report is to simulate the temperature distribution inside a chip in the following scenario using ANSYS. Apart from simulating the temperature distribution, the goal is also to decide an effective heat removal system. Towards this, following simulations are carried out to understand the effect of different parameters in the system.

1. Without any thermal management – Here, the cooling mechanism such as Peltier cooling and Fins which are used to remove the excess energy is turned off. The principal mode of heat transfer is through conduction inside the chip. At boundary, there will be an energy transfer to the surrounding through natural convection. So, air will act as coolant

2. Using Peltier Cooler- Here, current flows through Peltier which will be used to remove the excess energy.

The aim is to compare the result obtained in above 2 different cases. The primary objective will be to investigate how well temperature is below critical level.

1.3 Research Plan

Simulations were performed in Steady State Thermal Analysis in Ansys. Natural convective boundaries on both faces were used as given in the book. This model verified use of ANSYS for modelling actual problem. Later geometry of the actual setup was made consisting of chip, aluminium slab, and peltier cooler in Ansys design modeller. Initially, Simulations were performed on this model without giving current (i.e; Peltier is off) in the Steady State Thermal module. Later, with Peltier on (a current of 4 Ampere) the simulation was carried on actual setup in Thermo-Electric module in Ansys. As heat transfer coefficient, h of air is somewhere between 10 and 100 W/m2 K, simulation was performed by taking both minimum and maximum value of h..

Chapter 2: Literature Review

2.1 Cooling by convection

Air cooling has been used extensively for thermal management in the past. Due to its simple nature, less expensive, no specialized fluid requirement, easy to modify and high reliability, it is still the most common method today to control temperature at optimum level. Cha and Lloyd[3] used Finite difference method to simulate natural convection between two vertical parallel plates where one surface of temperature is kept varying. Starner and McManus[4] studied about natural convection heat transfer from fin arrays. They investigated four different fin array configuration and calculated heat transfer coefficient. Kim et al.[6] investigated laminar free convective heat transfer on vertically placed parallel plate with small line heat source inside.

2.2 Thermo-electric Module

Jean Peltier discovered the thermoelectric cooling effect in 1834. This thermo-electric cooling is known as Peltier Cooling effect [1]. He found that temperature difference is caused by current passing through a junction of two different materials. Peltier cooler consists of p type and n type semiconductors. These legs are connected together by copper to form a thermoelectric pair known as p-n couple. These couples are connected electrically in series and thermally in parallel. It consists of two ceramic plates generally known as cold side and hot side of Peltier Cooler. Ceramics are electrically insulating but have good thermal conductivity.

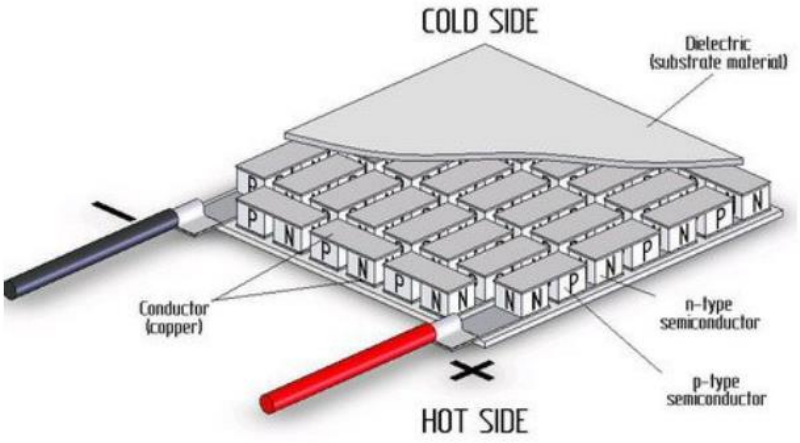


Fig 2.1 Peltier Module

2.3 Working Principle of Peltier Cooler (Thermoelectric cooler)

Thermoelectric coolers work on the principle of Peltier effect. This effect creates a temperature difference by heat transfer between two electric junctions. To create electric current, a voltage is applied across the joined conductors. On flowing of current through the junctions of the two conductors, heat is removed at one junction and cooling occurs and that removed heat is transferred and deposited at the other junction.

Pooja Iyer Mani [2] worked on Design and modelling of a thermoelectric cooling system using theoretical modelling and numerical simulation. The author studied the relation between various leg lengths and electrical contact resistance. She found out that electrical contact resistance in low leg length is higher than high leg length. So, the calculated cooling effect without taking contact resistance shows larger deviation in low leg length

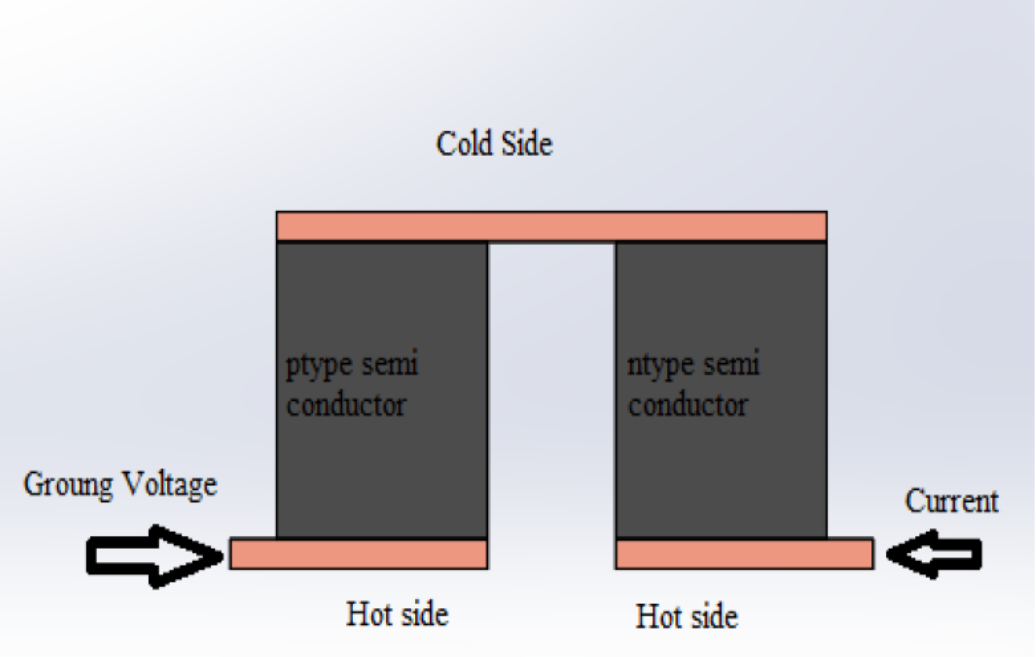


Fig 2.2 Peltier Cooler Working [2]

Chapter 3: Geometry

The description of the various components used in the entire electronic system is discussed in this chapter.

3.1 Electronic Device -Theoretical model

To model heat transfer in an electronic device, an electric chip developed by Dr.Nandkumar, School of Electrical Sciences, IIT Goa was used. The structure of the original chip is as follows:

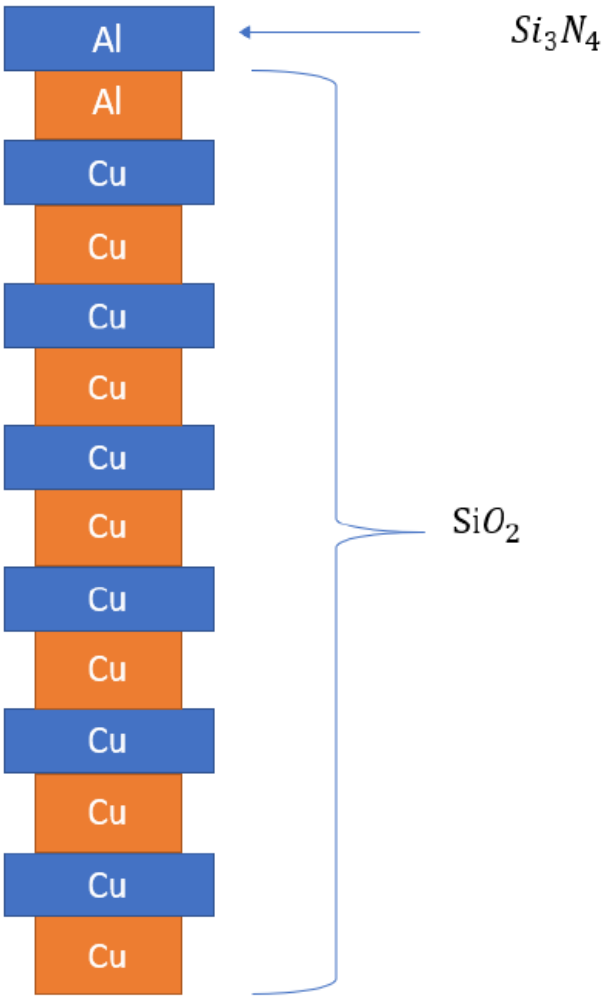


Fig 3.1 – Original Chip Structure

The height of the original chip is 380 micrometers, but this chip was approximated to be made up of equal proportion of copper and silicon for simplicity as shown in fig 3.2

3.1.1 Copper-Silicon Chip Design

This chip was approximated to be made up of equal proportion of copper and silicon for simplicity as shown in fig 3.2.

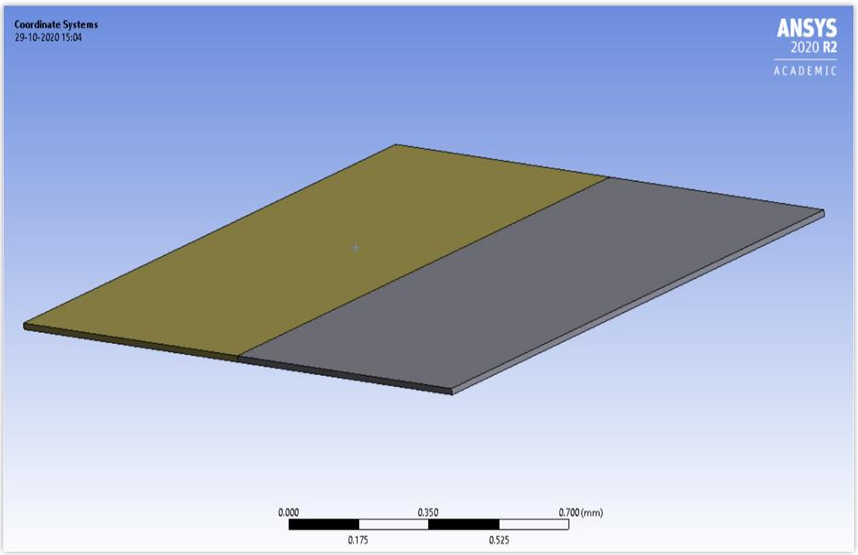


Fig 3.2 Copper-Silicon Chip

Dimensions of Silicon Dioxide and Copper chip are:

- Length: 0.75 mm
- Breadth: 1.35 mm
- Height: 0.01 mm

3.1.2 Heat Source Estimation

Heat source generated in chip was estimated by assuming heat generation in a very thin copper plate as shown in figure no.

Dimensions of copper heat source plate:

- Length: 1.5mm
- Breadth: 1.35mm
- Width: 0.01mm

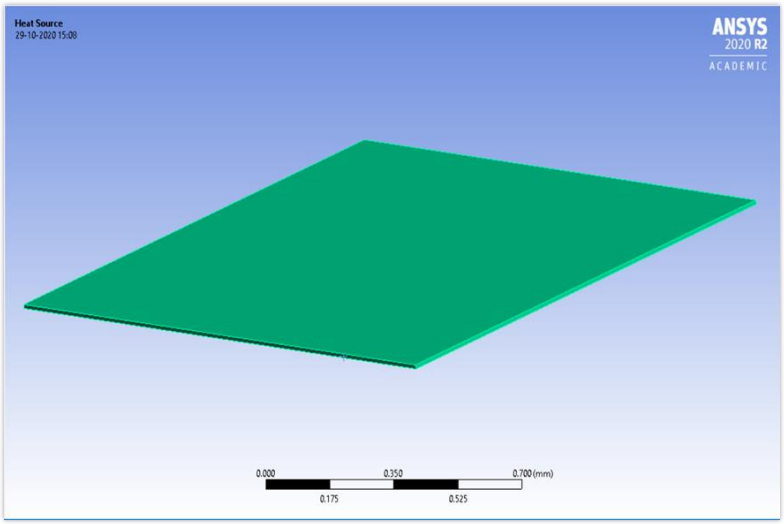


Fig 3.3 Heat Source

3.1.3 Silicon Base

Silicon base is constructed at the bottom of estimated heat source. This completes the structure of the electronic device.

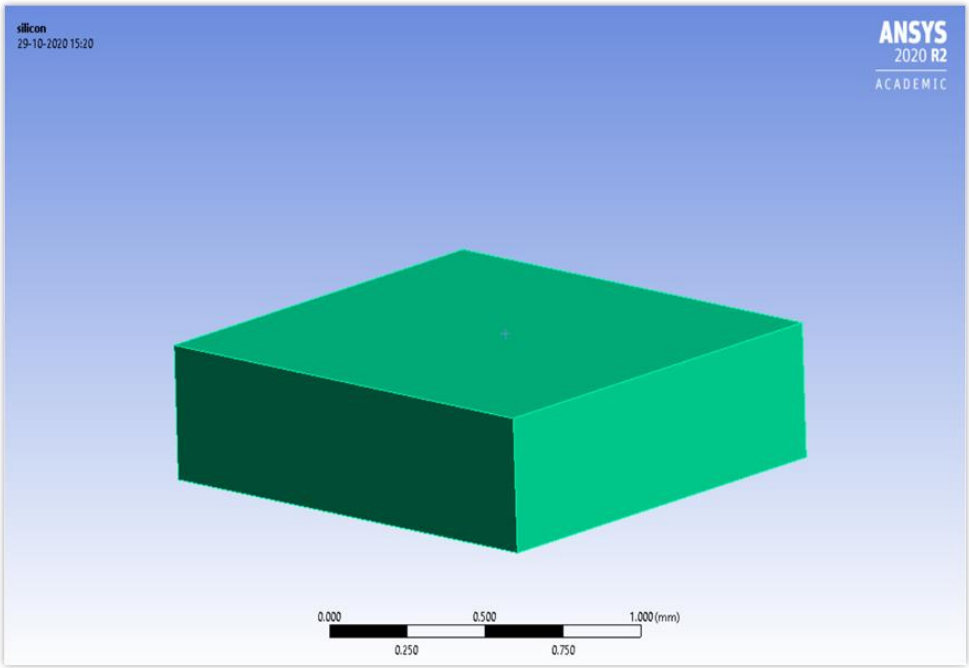


Fig 3.4 Silicon base

Dimensions of copper plate:

- Length: 1.5mm
- Breadth: 1.35mm
- Width: 3.665mm

3.2 Aluminium Base

Aluminium Base for flow of heat through the chip as it is a good thermal conductor. Also, it makes the thermoelectric cooler more effective.

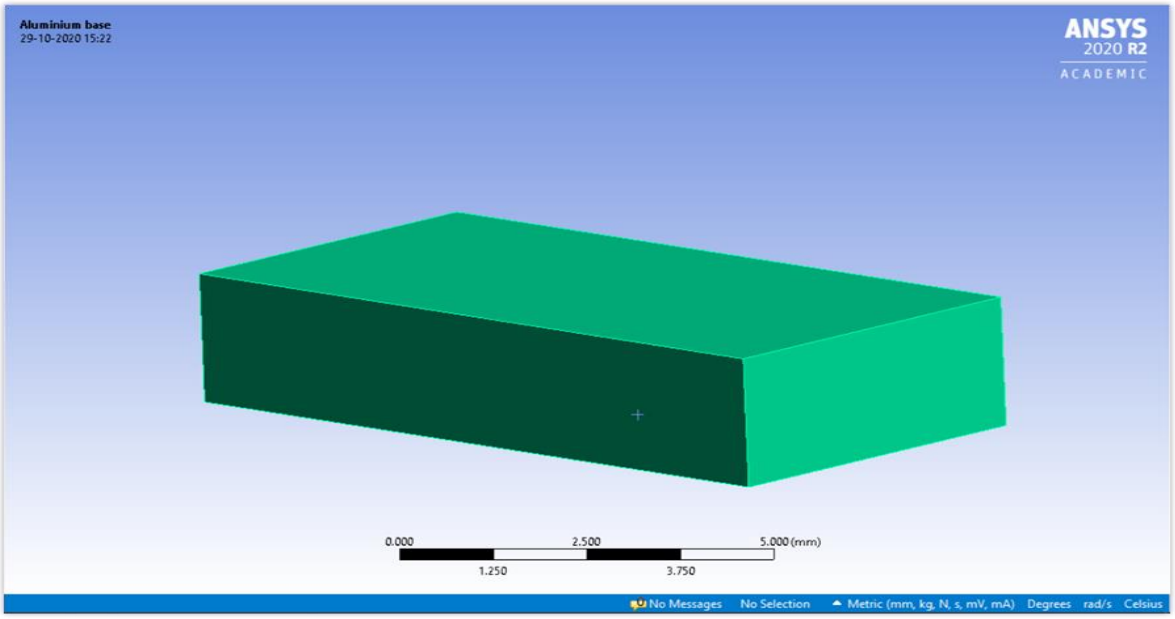


Fig 3.5 Aluminium Base

Dimensions of Aluminium base are:
1) Length: 10 mm
2) Breadth: 5mm
3) Height: 2mm

3.3 Thermoelectric cooler Design

A Peltier module was constructed to reduce temperature and cool the electric chip. Construction of the standard Peltier module is shown in figure 3.6 below.

The Peltier shown in the figure 3.6 has standard dimensions of 40mm x 40 mm. There are three parts of this peltier module:

1) Ceramic Plate
2) Copper Plate
3) NP couples placed alternately

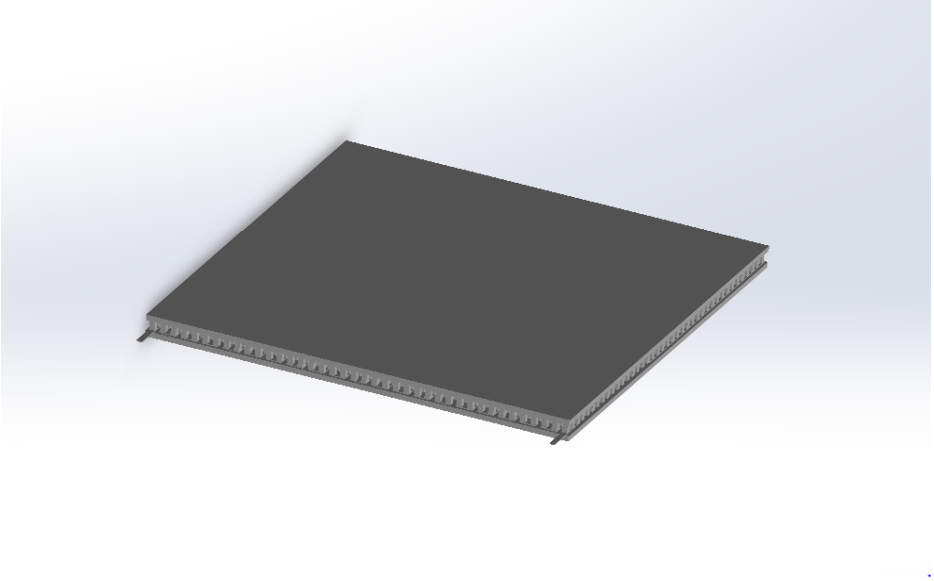


Fig 3.6 Peltier Module

Dimensions of Ceramic Plate:

1) Length: 40mm
2) Breadth: 40mm
3) Height: 0.6mm

Dimensions of Ceramic Plate:

1) Length: 40mm
2) Breadth: 1.5mm
3) Height: 0.1mm

Dimensions of N-P Couples:

1) Length: 0.5mm
2) Breadth: 0.5mm
3) Height: 1mm

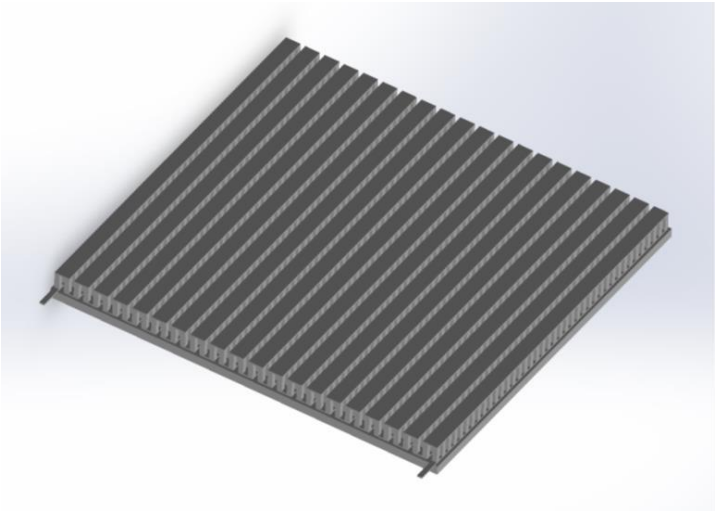


Fig 3.7 Cross section of Peltier Module

Chapter 4 : Methodology

The modeling of the heat transfer process within the set-up is discussed, boundary conditions used and other parameters used for simulation are also described in this chapter.

4.1 Heat Transfer (Steady State Thermal Simulation)

A 3D Heat Transfer model was used to simulate the temperature distribution in the chip, Aluminium base and thermoelectric cooler.

Conduction occurs inside the solid bodies while convection occurs at the surface where the body is in contact with surroundings.

- The general form of heat diffusion equation foe conduction is given as:

$$\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(k\frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right)+\dot{q}=\rho c_p\frac{\partial T}{\partial t}$$

Where,

ρ=$Density\ of\ the\ material$

T = Temperature

$\dot{q}$=$Internal\ Volumetric\ Heat\ Generation$

cp=$Heat\ Capacity$

The eqution shown above describes unsteady heat transfer in 3D cartesian coordinates involving heat generation. In our case we are assuming steady state heat transfer as we are more interested in knowing the temperature distribution when the chip reaches steady state. Hence, the term on the right hand side of the equation will be zero. Further, we assume the energy dissipated inside the chip to be uniformly distributed in space of specified magnitude.

Following Boundary conditions are generally used to know temperature distribution [7]:

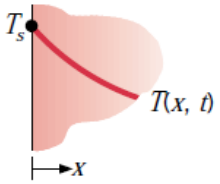
- Dirichlet Boundary Condition: This condition correspond to heat transfer through a surface with constant temperature.
- Neumann Boundary Condition: This boundary condition corresponds to specifying heat flux at the surface of a body.

- Mixed Boundary Condition: The boundary condition of the third kind corresponds to the existence of convection heating (or cooling) at the surface and is obtained from the surface energy balance discussed.

The following table shows the summary of the boundary conditions:

1. Constant surface temperature

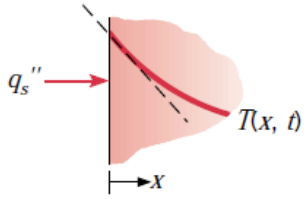
$$T(0, t) = T_s \qquad (2.29)$$



2. Constant surface heat flux

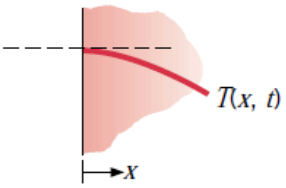
(a) Finite heat flux

$$-k\frac{\partial T}{\partial x}\Big|_{x=0} = q_s'' \qquad (2.30)$$



(b) Adiabatic or insulated surface

$$\frac{\partial T}{\partial x}\Big|_{x=0} = 0 \qquad (2.31)$$



3. Convection surface condition

$$-k\frac{\partial T}{\partial x}\Big|_{x=0} = h[T_\infty - T(0, t)] \qquad (2.32)$$

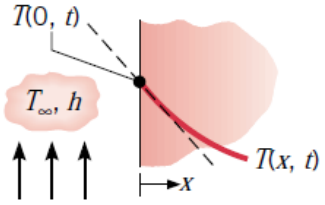


Table 4.1 Boundary Conditions [7]

- Convective Heat Transfer follows following equation:

$$q = h_c A dT$$

Where,

q = heat transferred per unit time (W)

A = heat transfer area of the surface (m2)

hc = convective heat transfer coefficient of the process (W/m2 C)

dT = temperature difference between the surface and the bulk fluid (C)

The simulation that we carried out used Mixed boundary condition as there is only convection on top face of the copper-silicon chip as well as on the bottom surfave of peltier. There is no boundary condition specifying constant surface temperature or constant heat flux. We cannot specify Dirichlet Condition because our aim is to find the temperature distribution in the body and in experimental set-up also no provision is available to fix the temperature of the other components also. Also, Neumann Condition cannot be assigned as information related to flux at boundaries is not available.

4.2 Thermoelectric Simulation (Thermoelectric Cooling)

Peltier Module was used as a thermoelectric cooler to cool the chip and dissipate the heat. The Peltier module works on the Peltier effect as described in literature review. [Section 2.2].
Two boundary conditions are given to the thermoelectric cooler in our model. One end of the Peltier is Grounded (0 mV) and the other end has been given 4A current.

Project schematic window of Ansys:

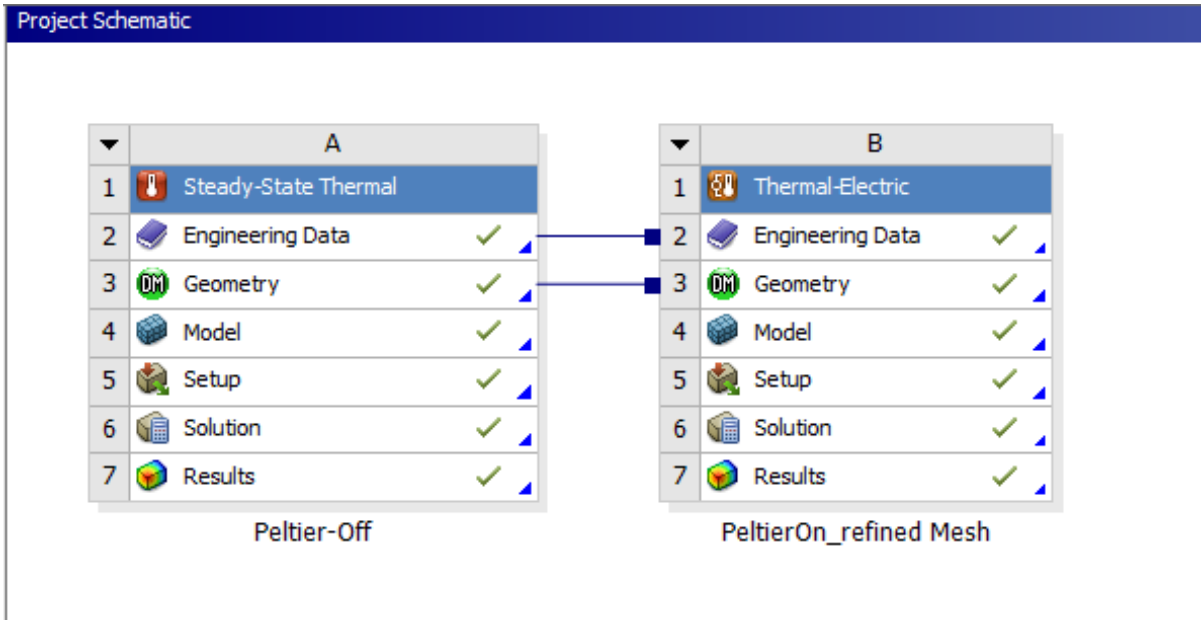


Fig 4.1 Project Schematic

4.3 Material Selection

The materials used in the simulation and their material properties are tabulated below:

MATERIAL	PROPERTIES
Aluminium	Density : 2689 kg m^{-3} Isotropic Thermal Conductivity: 237.5 W $m^{-1}C^{-1}$ Specific Heat: 951 J $kg^{-1}C^{-1}$
Aluminium Oxide	Density : 3960 kg m^{-3} Isotropic Thermal Conductivity: 35 W $m^{-1}C^{-1}$ Specific Heat: 850 J $kg^{-1}C^{-1}$
Bismuth n type	Isotropic Thermal Conductivity: 1.2 W $m^{-1}C^{-1}$ Isotropic Seebeck Coefficient: -0.000165 VC^{-1} Isotropic Resistivity: 1.05*10^{-5} ohm m
Bismuth p type	Isotropic Thermal Conductivity: 1.2 W $m^{-1}C^{-1}$ Isotropic Seebeck Coefficient: 0.00021 VC^{-1} Isotropic Resistivity: 9.8*10^{-6} ohm m
Copper	Density : 8933 kg m^{-3} Isotropic Thermal Conductivity: 400 W $m^{-1}C^{-1}$ Specific Heat: 385 J $kg^{-1}C^{-1}$ Isotropic Resistivity: 1.75*10^{-8}
Silicon	Density : 2330 kg m^{-3} Isotropic Thermal Conductivity: 148 W $m^{-1}C^{-1}$ Specific Heat: 712 J $kg^{-1}C^{-1}$
Silicon Dioxide	Density : 2220 kg m^{-3} Isotropic Thermal Conductivity: 1.5 W $m^{-1}C^{-1}$ Specific Heat: 745 J $kg^{-1}C^{-1}$

Table 4.2 Materials Used and their Properties (Data from Ansys Workbench)

Chapter 5: Results and Discussions

5.1 Assumptions

1. Chip is assumed to be made up of silicon dioxide and copper in equal proportions
2. Heat generation in chip comes from the copper slab (1.35mm x1.5mm x .01mm)
3. Bonded Contacts between bodies to perform simulations in ANSYS
4. No convection on surfaces other than Top Face of chip and bottom face of Peltier
5. a) Convection coefficient on top face- 10 and 100 W/m2 C (Air)

   b) Convection coefficient on bottom face is assumed to be 10 times to accommodate assumption of heat sink.

5.2 Temperature Distribution

As there is no information available on convective heat transfer coefficient (h W/m2 C), the simulation is carried out with two values of h. Temperature distribution is shown in two parts, when convective heat transfer coefficient is:

- h=10 W/m2 C
- h=100 W/m2 C

5.2.1 Temperature Distribution when h=10 W/m2 C

- Convective heat transfer is specified on the top face of the chip and bottom face of the peltier is assumed.
- Internal Heat Generation q= 123.456 W/$mm3$

PELTIER OFF:

Fig 5.1 above shows the temperature distribution in the assembled model when current as an input is not given to the peltier i.e no cooling effect. Maximum temperature occurs at the top of the chip where it is very near to the heat source. As we move down towards aluminium slab, temperature decreases gradually and attains minima at the bottom plate of the peltier cooler when Peltier is off. This is evident from Fig. 5.1.

Tmax = 56.781 °C (From Simulation)

Tmin = 37.101 °C (From Simulation)

Tmax = 57 °C (Experimental Result)

Tmin = 37 °C (Experimental Result)

We see that emperature results matches with the experimental result provided by Dr. Nandakumar, IIT Goa.

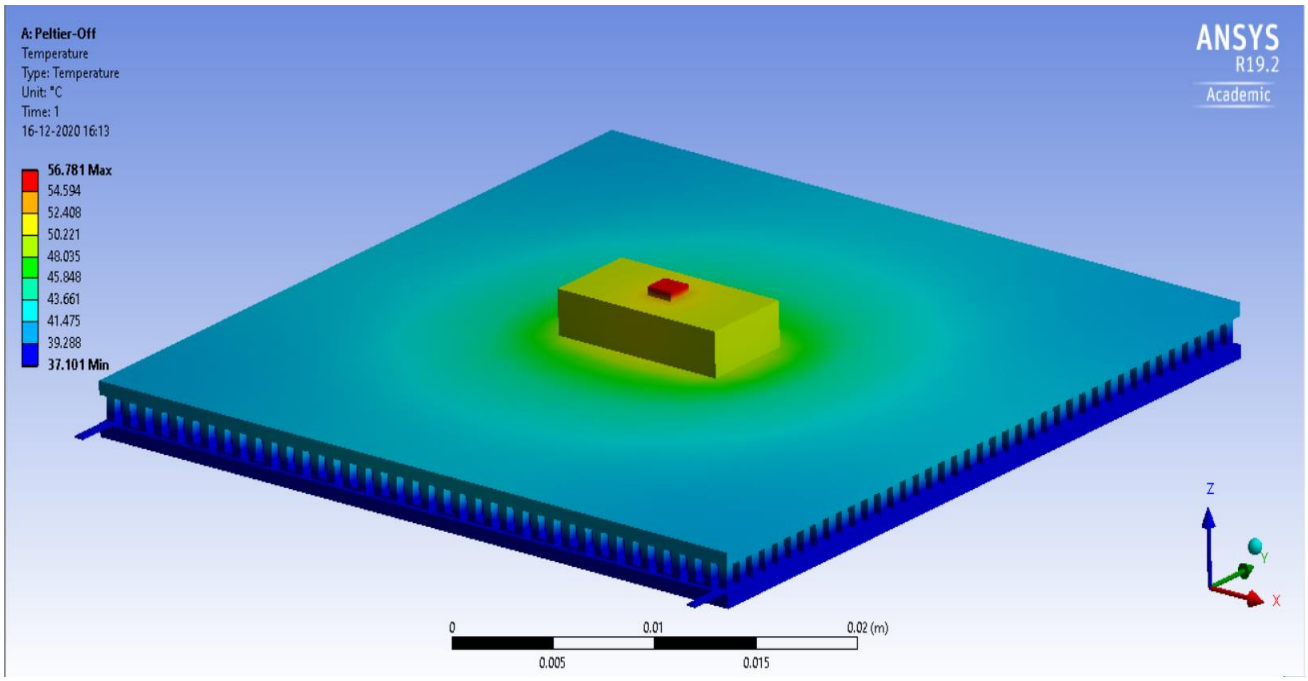


Fig 5.1 No current input

PELTIER ON:

When Peltier is on, maximum temperature occurs in silicon chip near heat source while minimum temperature occurs on top plate of Pelier cooler, indicating Peltier cooling.

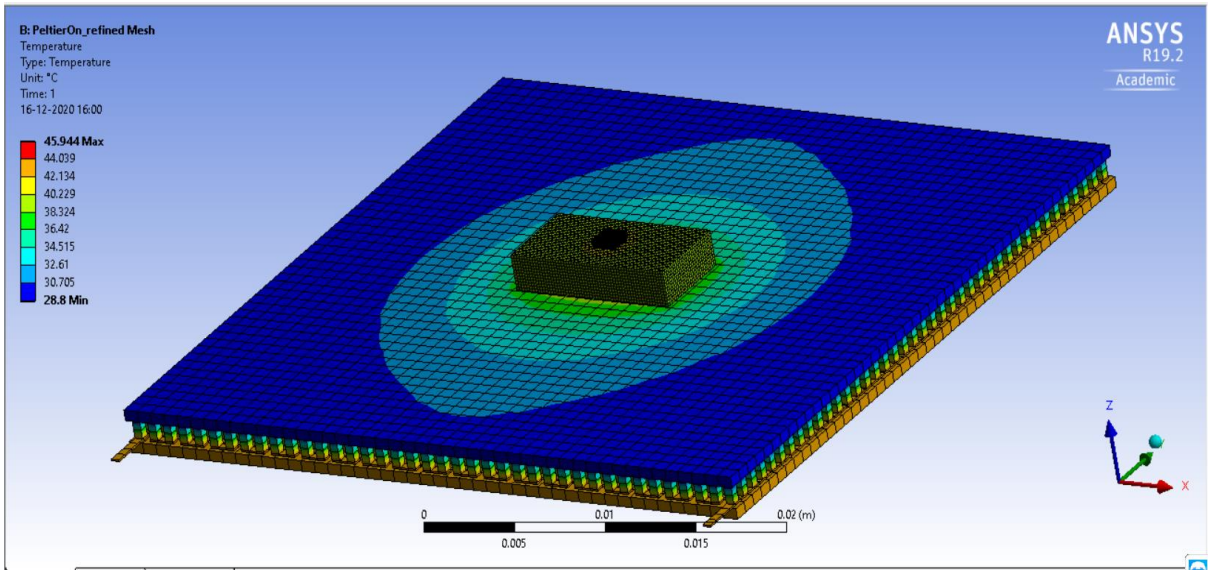


Fig 5.2 Current Input = 4 Ampere

Fig 5.2 shows temperature distribution in the model when the current in the peltier is turned on. As shown in the figure, maximum temperature is reduced because of the cooling effect by the peltier module.

Below shown is comparison in temperatures in silicon and aluminium base when current is off and on

Temperature Distribution in Silicon chip:

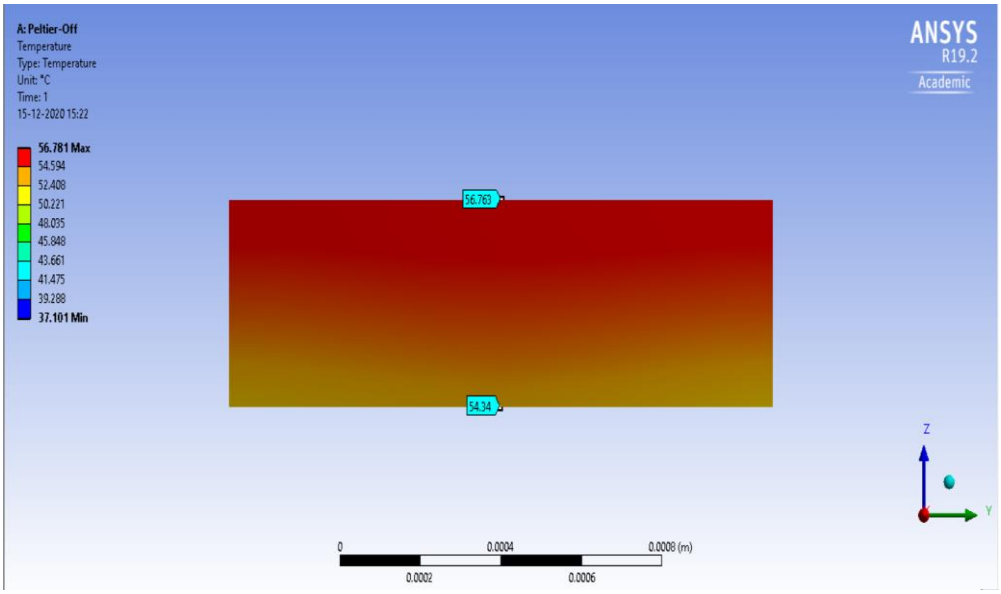


Fig 5.3 Current is Off, h = 10

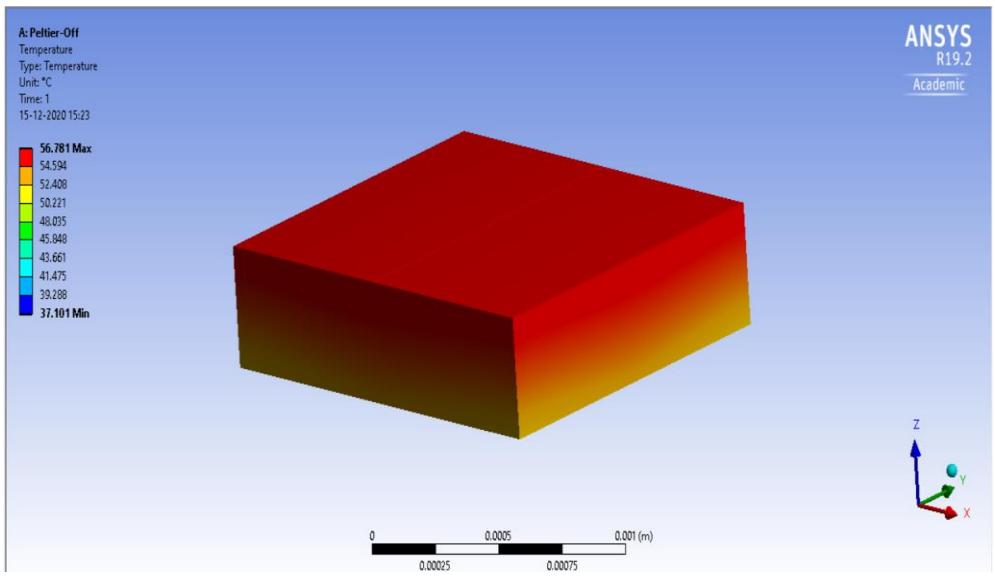


Fig 5.4 Current is Off, h =10, Isometric View

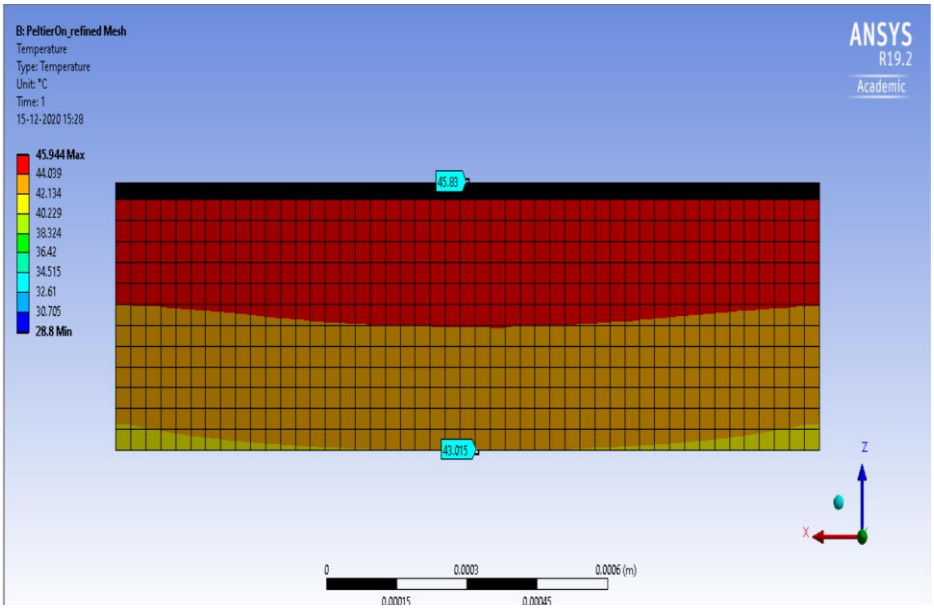


Fig 5.5 Current is On, h = 10

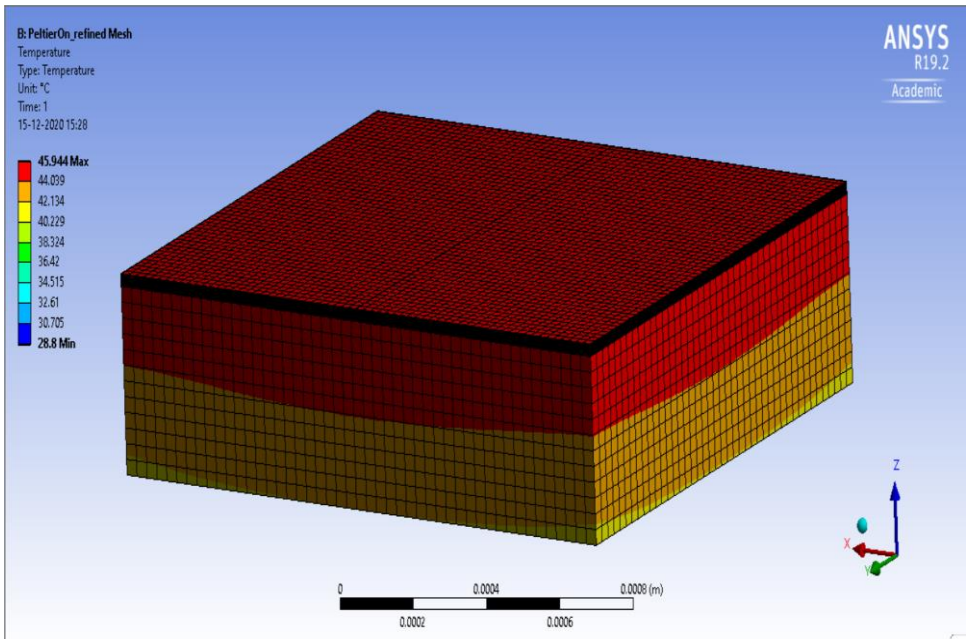


Fig 5.6 Current is On, h =10, Isometric View

From Fig 5.2 to Fig 5.6 we can conclude that when the current in the peltier is on, there is a temperature reduction of 10.787 °C in maximum temperature. Approximate reduction in temperature is summarized as:

ΔT=10.787 $°C$ (From simulations)

ΔT=12.5 $°C$ (From experiment)

5.2.2 Temperature Distribution when h= 100 W/m2 C

Maximum convection on top face of chip and peltier cooler is taken.

PELTIER OFF:

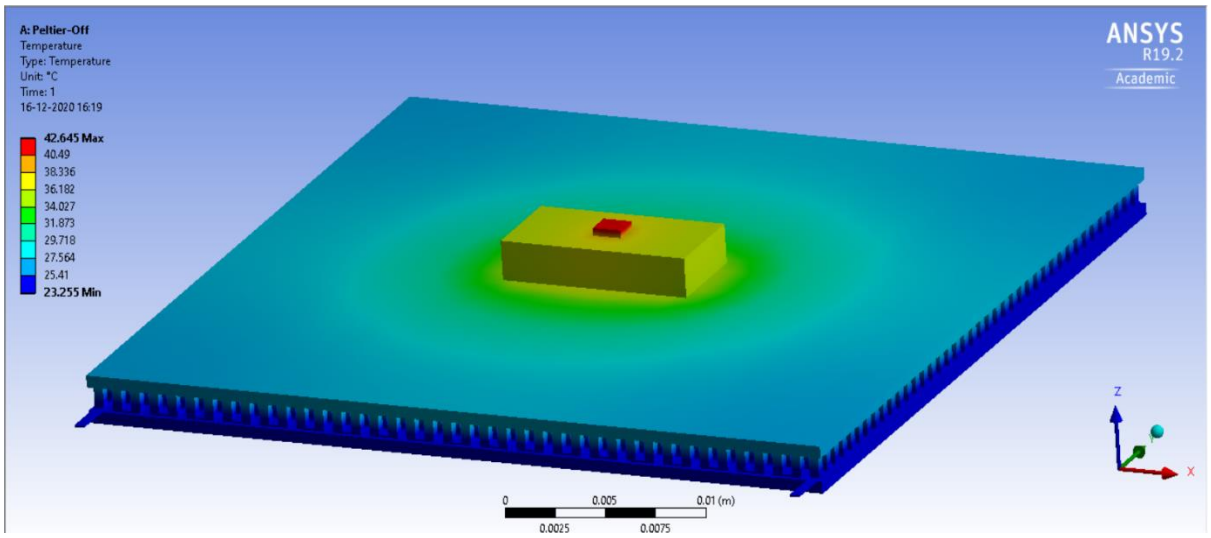


Fig 5.7 Peltier is off (h=100 W/m2 C)

PELTIER ON:

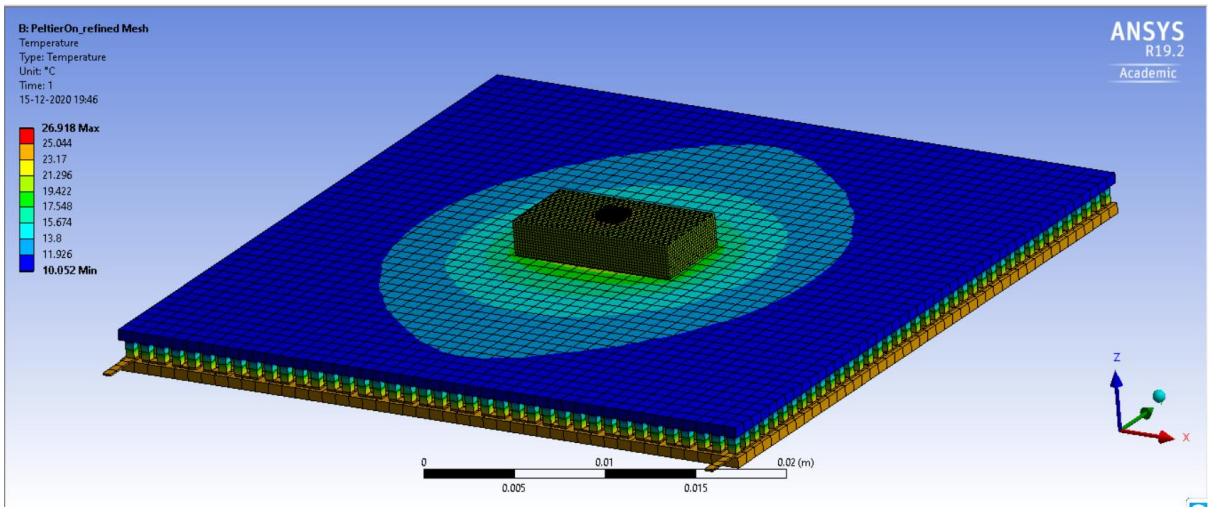


Fig 5.8 Peltier is on (h=100 W/m2 C)

From Fig 5.7 and Fig 5.8 it can be concluded that convection plays a major role in temperature distribution. At maximum convection (h=100), maximum temperature in chip reduces from 56.781 °C to 42.645 °C. Also, effect of Peltier cooler is more when the value of h is high which is evident because the bottom plate (heated plate) of peltier will be cooled easily when there is more convection. Approximate reduction in temperature when peltier is on at h=100 W/m2 C is ΔT=15.727 $°C$

which is bit far from experimental result of $\Delta T = 12.5$ °C.

5.3 Discussions

From the figures shown above, it is clear that peltier cooling has a noticeable effect on temperature. It reduces maximum temperature from 56.781 °C to 45.944 °C in case of h=10 W/m^2C. In case of h=100 W/m^2C it reduces maximum temperature from 42.645 °C to 26.918°C.

Moreover the results closely aligns with the experimental values provided to us. It shows that this model is a good approximation of the actual setup and hence assumptions in 5.1 can be considered reasonable. As predicted from the heat transfer analysis, conduction occurs from the body where internal heat is produced to other parts of the model. Hence, temperature is highest in the chip as it is closest to heat source. Peltier effect acts in such a way that top plate of Peltier module cools aluminium base which in-turn absorbs more heat from the silicon chip hence reducing the temperature.

Also, as seen from above convection co-efficient of air has drastic effect on temperature distribution.Convection co-efficient was not available in the information provided of experiment performed. Hence, results at both maximum and minimum (i.e 10 and 100 W/m^2C) Free Convection co-efficient of air is shown. Although, results obtained at minimum h (=$10W/m^2C$) are more close to experimental results.

Chapter 6: Conclusion and Future Scope

6.1 Conclusions

In this report, simulations for temperature distribution over a chip cooled by Peltier method is presented. It is clear from the results and discussion (5.1 and 5.2) that this model is able to predict the temperatures close to the experimentally observed values. Bottom plate of peltier module is getting heated when current is passed through the module, shows that model is working completely fine and as expected.

However, there are certain factors that must be accounted for to achieve best results. Proper experimental study with more information is required to verify the results. Also, some of the assumptions can be overcome by modelling the actual conditions such as Heat Transfer in heat sink using CFX.

6.2 Future Scope

1) Heat sink below peltier cooler can be modeled and simulations can be performed using CFX.
2) Better approximation of chip can be done.
3) Work can be done to include contact resitance in Heat Transfer Analysis.
4) Better experimental study on convective heat transfer of chip while performing experiment.
5) Convection on other faces can be considered in addition to top and bottom face of the chip.

Chapter 7 : References

[1] VAIDEHI BHARAT PATEL.“ Experimental/Computational Analysis Of Active Cooling Of Stacked Device Using Multidimensional Configured Thermoelectric Modules”(2012).

[2] Pooja Iyer Mani. “ Design, Modeling and Simulation of a Thermoelectric Cooling System (TEC)”.(2016).

[3] Cha, W., and Lloyd, J. R., 1989, “Numerical Study of Natural Convection Between Two Vertical Parallel Plates with One Oscillating Surface Temperature,” ASME HTD-Vol. 121.

[4] Starner K.E. and McManus H.N. “An Experimental Investigation of Free Convection Heat Trasnfer from Rectangular Fin Arrays”, Journal of Heat Transfer, 273-278, (1963).

[5] L.T. Yeh. “ Review of Heat Transfer Technologies in Electronic Equipment”.(1995)

[6] S. H. Kim ,N. K. Anand ,L. S. Fletcher. “ Free Convection Between Series of Vertical Parallel Plates With Embedded Line Heat Sources”. Journal of Heat Transfer (Transactions of the ASME (American Society of Mechanical Engineers), Series C); (United States)

[7] Bergman, T.L., Incropera, F.P., DeWitt, D.P. and Lavine, A.S., 2011. *Fundamentals of heat and mass transfer*. John Wiley & Sons.