Harshit Kumar Shakya

+91-8839609468 harshitshakya49@gmail.com Linkedin GitHub

SUMMARY

M.Tech graduate in VLSI & Embedded Systems, currently working as a Hardware Design Engineer. Skilled in PCB design and circuit optimization using Altium, KiCAD, and LTSpice. Proficient in Verilog/VHDL development with Xilinx Vivado. Hands-on with Arduino, Basys-3, and Artix-7 boards; working knowledge of C/C++ and Python.

EXPERIENCE

Sq.M Technologies Pvt. Ltd. **Mar 2025 – Present**

Hardware Design Engineer *Pune, Maharastra*

- Conducting functional testing and validation of PCB prototypes to ensure design accuracy and performance.
- Assisting in debugging hardware issues and verifying circuit integrity using lab tools and instruments.
- Collaborating with the engineering team to document test procedures and support continuous design improvements.

Faradtech Innovative Solutions Pvt. Ltd. **Nov 2023 – May 2024**

Hardware Engineer Intern *Bengaluru, Karnataka*

- Worked on PCB schematics, making sure every component was linked appropriately and complied with design specifications. Before the layout stage, mistakes were checked to avoid problems.
- Selected and arranged suitable ICs and microcontrollers to improve system performance and reduce power usage. Coordinated with the team to ensure smooth integration with the PCB layout handled by another team.
- Refined the electrical design of the Smart KVM Switch to lower production costs and enhance product performance, while the layout was handled by another team.

EDUCATION

Defence Institute of Advanced Technology **Aug 2022 – June 2024**

M.Tech in VLSI and Embedded Systems *Pune, Maharashtra*

Madhav Institute of Technology and Science **Aug 2017 – June 2021**

B.Tech in Electronics and Telecommunications *Gwalior, Madhya Pradesh*

TECHNICAL SKILLS

Programming Languages: Python (Basics), C/C++ (Basics)
Hardware Description Languages(HDLs): VHDL, Verilog
Technologies/Tools Used: Xilinx ISE, Vivado, Cadence Virtuoso, LT-Spice, KiCAD, Altium Designer
Embedded Platforms/Hardwares: Basys-3, Artix-7, Arduino Uno

PROJECTS

Designed 6T SRAM using CMOS Technology | *Cadence Virtuoso* **Feb 2023 –Jun 2023**

- Analyzed a 6T SRAM cell using 6T standard cells and Double Patterning Compatible (DPC) CMOS technology.
- Redesigned a 6T SRAM cell with characteristics such as low-leakage control, high read and write currents, efficient power management, and reduced standby power usage.
- Performed transistor-level circuit design and layout to enhance performance and area metrics, leading to a decrease in power consumption and a boost in circuit density.

Xilinx Analog to Digital Converter using 7-series board | *Xilinx Vivado* **Feb 2023 – Jun 2023**

- Designed and implemented an Analog Digital Converter using Xilinx 7-series FPGA development board.
- XADC excesses up to 17 external I/O analogue channels and these analogue inputs can be uni-polar, bi-polar, temp sensors and power supply sensors.
- Leveraged control and status registers to obtain XADC conversion data, resulting in a improvement in read/write operations and overall system performance.

Created and implemented an FPGA-powered vending machine | *Xilinx Vivado* **Oct 2022 – Nov 2022**

- Architected and innovated an FPGA-based vending machine via Xilinx Vivado, reducing transaction time and enhancing operational efficiency, thereby increasing sales revenue.
- Designed and restructured a finite state machine (FSM) in Verilog, leveraging behavioral modeling; executed rigorous testing with Xilinx Vivado, enhancing performance efficiency.
- Pioneered a detailed exploration of Mealy and Moore models, performing static timing analysis to markedly enhance design reliability and performance, achieving improvement in system robustness.

Design of a MIMO Antenna | *CST* **Jan 2021 – Apr 2021**

- Revolutionized MIMO antenna design by defining precise requirements boosting network performance metrics; achieved an increase in data speeds and reduction in network congestion.
- Conducted a detailed evaluation of spatial diversity and frequency range; refined design adjustments that increased signal quality and decreased interference, enhancing overall system efficiency

CERTIFICATIONS

- An Introduction to Programming the Internet of Things (IoT) Specialization | *Coursera* | Certificate Link
- FPGA Architecture and Programming | *MOOC NIELIT Calicut* | Certificate Link
- VLSI Design | *Internshala Trainings* | Certificate Link
- Natural Hazards | *NPTEL* | Certificate Link
- Renewable Energy Engineering: Solar, Wind and Biomass Energy Systems | *NPTEL* | Certificate Link
- Modern Digital Communication Techniques | *NPTEL* | Certificate Link
- RTL to GDS Flow (6-week Online Training) | *NIELIT Noida* | Certificate Link
- Advanced Physical Design and Verification | *Maven Silicon* | Certificate Link

EXTRACURRICULAR

- Volunteer at an inter-school sports festival as a sports captain.
- Twice, the district's school poster making the champion.
- 3 times, National qualified in school games of Kendriya Vidyalaya Sangathan in Taekwondo.
- Awarded Black Belt 2nd Dan Diploma in SHITO–RYU–KARATE from National Sports Council, Nepal Olympic Committee in Oct 2015.
- Served four years as an instructor at Martial Art Academy, Singrauli (M.P.) from 2013-17.
- Attended a workshop on "Entrepreneurship for Making Self-Sufficient Entrepreneurs, Innovators and Advances in Deep Architectures for Signal, Image and Vision Applications" in IIIT Allahabad.
- Qualified GATE-22 ECE.
- Completed a rigorous 7-day Cadence EDA workshop at DIAT, Pune; acquired advanced skills in electronic design automation, leading to a boost in design accuracy and overall productivity.
- Attended Internship/Training Program on VLSI Design flow (RTL to GDS-II) (Online Mode) from 24 June, 2024 to 02 August, 2024, conducted by NIELIT, Noida.

DECLARATION

I, Harshit Kumar Shakya, declare that all details furnished above are true to the best of my knowledge and belief.

[HARSHIT]