# Innovation and Entrepreneurship

Course Instructor: Dr Bishwajeet Pandey

## **Syllabus**

#### **Course Content:**

**Unit I:** Introduction to Entrepreneurship: Entrepreneurs; entrepreneurial personality and intentions - characteristics, traits and behavioral; entrepreneurial challenges.

**Unit II:** Entrepreneurial Opportunities: Opportunities. Discovery/ creation, Pattern identification and recognition for venture creation: prototype and exemplar model, reverse engineering.

**Unit III:** Entrepreneurial Process and Decision Making: Entrepreneurial ecosystem, Ideation, development and exploitation of opportunities; Negotiation, decision making process and approaches, Effectuation and Causation.

**Unit IV:** Crafting business models and Lean Start-ups: Introduction to business models; Creating value propositions-conventional industry logic, value innovation logic; customer focused innovation; building and analyzing business models; Business model canvas, Introduction to lean startups, Business Pitching.

**Unit V:** Organizing Business and Entrepreneurial Finance: Forms of business organizations; organizational structures; Evolution of Organisation, sources and selection of venture finance options and its managerial implications. Policy Initiatives and focus; role of institutions in promoting entrepreneurship.

### Some Question Asked by Student?

- Is it tough to pass this Course?
- I have PAN card, but my possible partner in my future startup has not pan card?
- I shall not become Entrepreneur because I have not an unique idea.
- I have an unique idea, what I shall do?
- So for right, now we can work on the patent and get it published, and then apply for the pan card?

## Is it tough to pass this Course?

- No, it is easy to pass because it has less syllabus.
- It has only 28 lectures.
- There is 4 lecture in every week as per class schedule, 3 will use for syllabus and 1 for Entrepreneur Lecture Series.
- Out of 28, only 21 related to syllabus (Unit I-V) and rest 7 are for Entrepreneur Lecture Series, you should learn only 21 lecture slide for exam.
  - 3-3-3 Lecture for Unit I-II-III: Total 9 Lectures for Unit I-II-III
  - 6-6 Lectures for Unit IV-V: Total 12 Lectures for Unit IV-V
- 7 Entrepreneur Lecture Series:
  - Just for information (who do not want to become an Entrepreneur)
  - For Inspiration (who want to become an Entrepreneur)

## I have PAN card, but my possible partner in my future startup has not pan card?

• For opening a bank account of startup, you need a pan card of startup.

• Pan card of startup has no any father name and date of birth, whereas it has date of incorporation (the date when startup come into existence)

• For application of pan card of startup, you do not need pan card of your partner but

you need partnership deed.





## I shall not become Entrepreneur because I have not an unique idea.

- A person become entrepreneur only when he want to become his own boss, he has desire to become rich.
- Jio was not unique idea, the idea of mobile phone existed as Airtel, Idea, BSNL and Vodafone.
- OLA was not unique idea, the idea of cab booking existed as UBER and many more.
- One of my student is going to open a web designing company as a startup,
   but there are thousands of web designing company already in existence.
- So, you need not have a unique idea for startup, you may copy any existing idea and begin a startup to earn money.

## I have an unique idea, what I shall do?

- If you have a unique idea, then you may
  - Get a patent for that idea
  - Initiate your own startup based on that unique idea.

## So for right, now we can work on the patent and get it published, and then apply for the pan card?

- Pan card is not needed for patent application.
- You have to a make partnership deed and then apply for pan card.
- For patent, you have to make a draft of patent application and then contact Patent Attorney, he/she will file your patent.

### Process of Filing a Patent

- For patent, you have to make a draft of patent application
- Contact Patent Attorney, he/she will file your patent application
- After filing patent, you will get an ACKNOWLEDGEMENT SLIP from PATENT OFFICE INTELLECTUAL PROPERTY BUILDING, S.M.Road, Antop Hill, Mumbai-400037
- Then patent office check your idea with database of existing patent, if they
  find your idea is unique then the patent office publish patent in Official Journal
  of Patent Office.

FORM 2 THE PATENTS ACT, 1970 (39 OF 1970)

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THE PATENTS RULES, 2003

COMPLETE SPECIFICATION

(SEE SECTION 10 AND RULE 13)

#### GPHL IO STANDARDS BASED ENERGY EFFICIENT VEDICMULTIPLIER DESIGN ON FPGA

#### FIELD OF INVENTION

The present invention relates generally to the field of electronics and communication and its application in Digital Signal Processing (Vedic Multiplier). More particularly, the present invention is directed towards GPHL IO Standards based energyefficient Vedic Multiplier design on FPGA.

#### BACKGROUND OF THE INVENTION

Important terms in relation to Vedic Multiplier using digital signal processing and communication technology:

#### 1. VedicMathematics:

Ancient mathematics is also known as Vedic Mathematics. Vedic mathematics is a part of four Vedas (books of wisdom). It is part of Sthapatya-Veda, which is an Upa-yeda (supplement) of Atharva Veda. It comprises the description of various modern mathematical terms that includes arithmetic, geometry, trigonometry, quadratic equations, factorization and even calculus. Vedic mathematics provides principles to solve the tedious mathematical

#### CLAIM:

- 1. AGPHL IO Standards and Verilog HDLbased energy efficient Vedic Multiplier design on FPGA of consisting of GTL, PCI, HSUL and LVTLL Input output Standards wherein energy efficiency is achieved by process variation, voltage scaling and thermal scaling techniques implemented on hardware.
- 2.The GPHL IO Standards and Verilog HDL based energy efficient Vedic Multiplier design on FPGA consisting of GTL, PCI, HSUL and LVTLL Input output Standards as claimed in claim 1 wherein process variation is achieved by using 28nm FPGA board for Vedic multiplier circuit design.
- 3.The GPHL IO Standards and Verilog HDL based energy efficient Vedic Multiplier design on FPGA consisting of GTL, PCI, HSUL and LVTLL Input output Standards as claimed in claim 1 wherein Voltage Scaling technique implemented on hardware results in total power consumption reduction of 58.92% on decreasing the value of voltage from 1.5 Volts to 0.5 Volts.
- 4. The GPHL IO Standards and Verilog HDL based energy efficient Vedic Multiplier design on FPGA consisting of GTL Input output Standard as claimed in claim 1 wherein Thermal Scaling technique implemented on hardware results in total power consumption reduction of

#### ABSTRACT

#### GPHL IO STANDARDS BASED ENERGY EFFICIENT VEDIC MULTIPLIER DESIGN ON FPGA

In the present invention, the inventors have integrated the expertise of electronics researcher and Arithmetic Logic Unit to develop low cost, low power and secure hardware based Vedic Multiplier design for applications like Digital Signal processing. The Vedic multiplier is designed on the basis of Urdhya Tiryagbhyam sutra of Vedic mathematics. In order to make Vedic multipliertime efficient, speedy and having lesser area are implemented in Arithmetic and Logical Units replacing the traditional multipliers and squares based on array and Booth multiplication. In order to make them energy efficient, techniques like voltage scaling, thermal scaling and process variation have been usedforLVTTL, PCI, GTL and HSUL IO standards for energy efficient Vedic multiplier.

### Receipt after Filing Patent Application

PATENT OFFICE INTELLECTUAL PROPERTY BUILDING Plot No. 32, Sector 14, Dwarka, New Delhi-110075 Tel No. (091)(011) 28034304-06 Fax No. 011

28034301,02

E-mail: delhi-patent@nic.in Web Site: www.ipindia.gov.in

Docket No 28980

To BANSAL KOMPAL सत्यमेव जयते



Date/Time 28/10/2014

User Code: kompal260

#### #5568, Sector 38 west

Sr.	Ref.	App.	Amount	C.B.R.	Form	Remarks
No.	No./Application No.	Number	Paid	No.	Name	
1	3064/DEL/2014		8000	21579	FORM 1	GPHL IO STANDARDS BASED ENERGY EFFICIENT VEDIC MULTIPLIER DESIGN ON FPGA

Total Amount: ₹ 8000

Amount in Words: Rupees Eight Thousand Only

#### Patent Publish in Patent Journal

पेटेंट कार्यालय शासकीय जर्नल

**OFFICIAL JOURNAL** 

OF THE PATENT OFFICE

निर्गमन सं. 23/2016 ISSUE NO. 23/2016

शुक्रवार FRIDAY दिनांक: 03/06/2016

DATE: 03/06/2016

#### Patent Publish in Patent Journal

ipindia.nic.in/writereaddata/Portal/IPOJournal/1\_347\_1/part1.pdf

165 / 1022							
(12) PATENT APPLICATION PUBLICATION (19) INDIA	(21) Application No.3064/DEL/2014 A						
(22) Date of filing of Application :28/10/2014		(43) Publication Date : 03/06/2016					
(54) Title of the invention : GPHL IO STANDARDS	BASED ENI	ERGY EFFICIENT VEDIC MULTIPLIER DESIGN ON FPGA					
(51) International classification	:G06F 7/00	(71)Name of Applicant : 1)CHITKARA UNIVERSITY					
(31) Priority Document No	:NA	Address of Applicant : CHITKARA UNIVERSITY					
(32) Priority Date	:NA	Chandigarh-Patiala National Highway(NH-64) Tehsil Rajpura ,					
(33) Name of priority country	:NA	Distt. Patiala Punjab India Punjab India					
(86) International Application No Filing Date	:NA :NA	(72)Name of Inventor: 1)PANDEY BISHWAJEET					
(87) International Publication No	: NA	2)GOSWAMI KAVITA					
(61) Patent of Addition to Application Number Filing Date	:NA :NA	A 200 300					
(62) Divisional to Application Number Filing Date	:NA :NA						

#### (57) Abstract:

In the present invention, the inventors have integrated the expertise of electronics researcher and Arithmetic Logic Unit to develop low cost, low power and secure hardware based Vedic Multiplier design for applications like Digital Signal processing. The Vedic multiplier is designed on the basis of Urdhva Tiryagbhyam sutra of Vedic mathematics. In order to make Vedic multiplier time efficient, speedy and having lesser area, are implemented in Arithmetic and Logical Units replacing the traditional multipliers and squares based on array and Booth multiplication. In order to make them energy efficient, techniques like voltage scaling, thermal scaling and process variation have been used for LVTTL, PCI, GTL and HSUL IO standards for energy efficient Vedic multiplier.

No. of Pages: 29 No. of Claims: 8

## Process of starting a Business/Startup

- Find Partner and Venture Capitalist
- Finalize name of Startup and Business Areas
- Finalize Shareholding
- Apply For Pan Card
- Open a Bank Account
- Book Domain Name
- Launch Website
- Start Marketing of your Businesses

## Find Partner and Venture Capitalist

#### CONSTITUTION OF PARTNERSHIP DEED

This DEED PARTNERSHIP was made at Motihari on the day 20th of August 2020 by and between.

- 1) Harshit Pathak (Hereinafter called the First partner)
- 2) Manas Joshi (Hereinafter called the Second partner)
- 3) Mrs Pushpanjali Pandey (Hereinafter called the Third partner or Venture Capitalist provide seed money)\
- 4) Prof G S Tomar, Director, BIAS Bhimtal (Hereinafter called the Fourth partner, who provide space for Office)





Finalize name of Startup and Business Areas

#### NOW THIS DEEDS OF PARTNERSHIP ARE FOLLOWING:

- That the deed of partnership shall be deemed to have come force with effect from 20.08.2020
- The parties have decided to run their business under the name and style of M/s XYZ
   Technology At Bhowali-Bhimtal Road, Bhimtal-263136 or any other name which partners may mutually decide on time.
- That the partnership business shall be carried on under the name and style of M/s XYZ
   *Technology At* Bhowali-Bhimtal Road, Bhimtal-263136 which shall deal in Al Based
   *Technology Solutions* and all other related items which parties may decide from time
   to time.
- That the principal place of business of the partnership shall be at Mathiya Zirat, Motihari, East Champaran, Bihar, India, 845401 or such other place or places as the parties shall from time to time mutually decide.

#### Finalize Shareholding and Mode of Operation

8. That the firm shall prepare a balance sheet and profits and loss account every year on 31<sup>st</sup> March and the Net Profit/Losses of the partnership Business after deduction of all expenses relating to the business of the firm as well as salary payable to the partners in accordance with this deed of partnership shall be shared or borne by the parties as the case may be in following proportion:

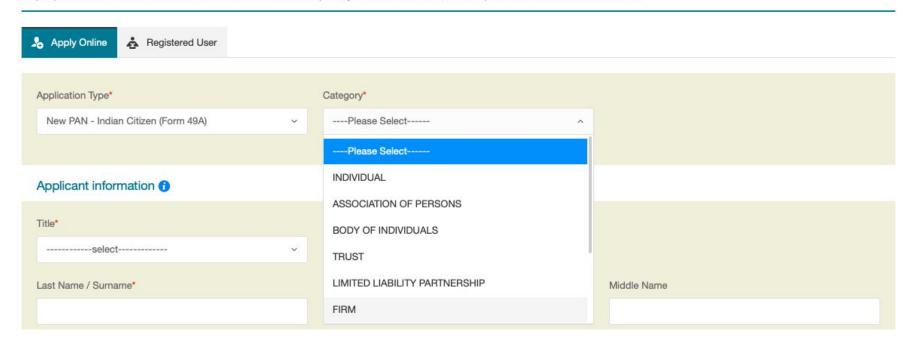
> Harshit Pathak - 45% Manas Joshi- 45% Pushpanjali Pandey : 5% BIAS Bhimtal: 5%

That the bank accounts of the firm may be opened in any scheduled bank and would be operated by Harshit Pathak and Manas Joshi jointly.

#### Apply For Pan Card

#### Online PAN application

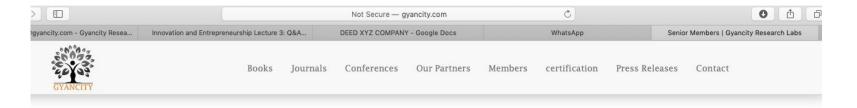
As per provisions of Section 272B of the Income Tax Act., 1961, a penalty of ₹ 10,000 can be levied on possession of more than one PAN.



#### **Book Domain Name**



#### Launch Website



#### The Senior Members of Gyancity Research Labs



Karan Singh Senior Member Gyancity Research Lab



Bishwajeet Pandey

Co-Founder, Gyancity
Research Lab, &
Gyancity Research
Consultancy



Kartik Kalia
Co-Founder Gyancity
Research Lab



Uday Shankar Pathak

Director, Gyancity
Research Lab



D. M. Akbar Hussain

Co-Founder
Gyancity Research Lab
& Gyancity Research
Consultancy



Pushpanjali Pandey
Director of Gyancity
Research Lab &
Gyancity Research
Consultancy

## Start Marketing of Your Business



#### Next Lecture No 4: Entrepreneur Lecture Series

