EDL 2024 P16-MON-08
An FPGA-instrument for RRAM characterization with on-board oscilloscope

Documentation for PCB

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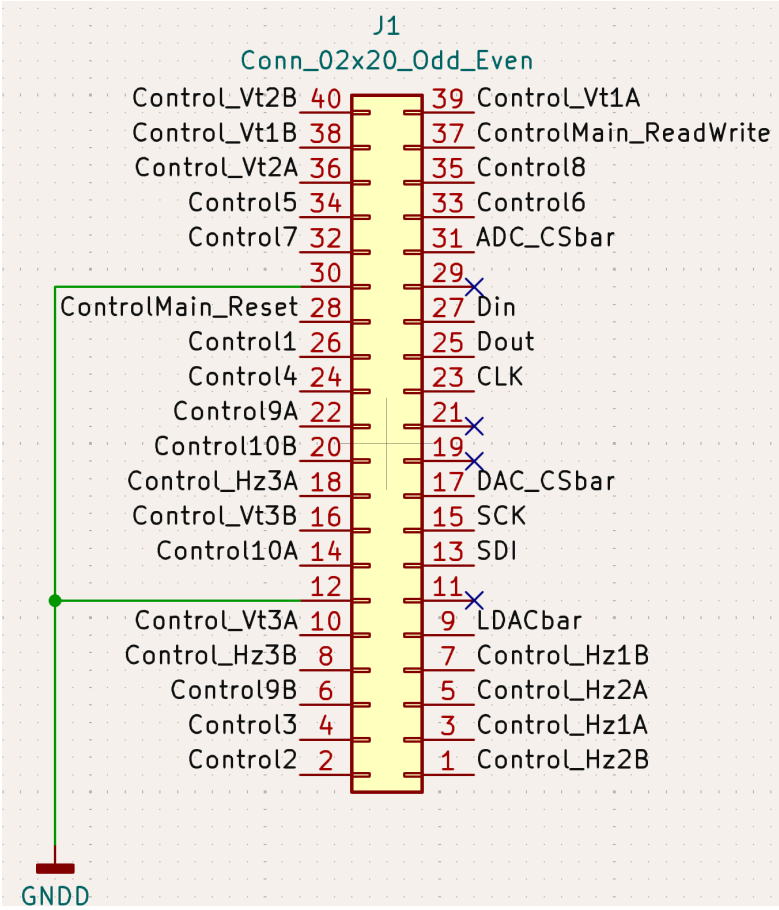
Control Signals:

1. Controls 1 through 8 correspond to the Switches 1 through 8 as in the paper. 1 is for writing and 2 through 6 are the sense resistors. 7 and 8 are for connection to the ADC.
2. Controls 9A and 9B correspond to the Switch 9 in the paper. It was an SPDT switch but since we used SPST switches, we needed two control signals and had to split it. 9A and 9B should always be the complement of each other. The same happens in Switch 10
3. VtXY corresponds to the vertical crossbar line X, and Y is either A or B, similar to the above point.
4. HzXY is similarly the horizontal crossbar line X, and Y is either A or B.
5. To choose a location say 2,3 — set Hz2A = 1 and Hz2A = Hz3A = 0, Vt1A = Vt2A = 1 and Vt3A = 0 (B will always be the complement of corresponding A). Hence, in HzXA, only one is set 1 whereas in VtXA, only one is set 0.
6. Read/Write and Reset is self explanatory and set 1 when doing that task.

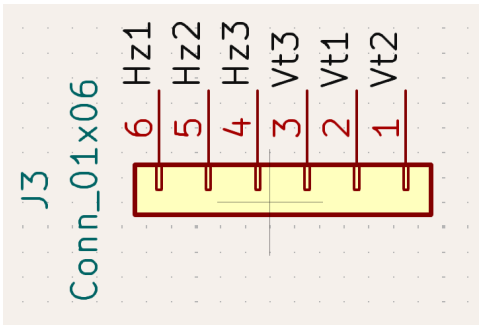
For the FPGA connection, connect it to header GPIO 00 such that the entire FPGA lies away from the main PCB. The pins 1 and 3 in DE0-nano were read only so we had to short it to empty pins to ensure we could write on it. The exact pin mapping is given below with pin 1 shorted to pin 19 and pin 3 to pin 21 using wire on the PCB.



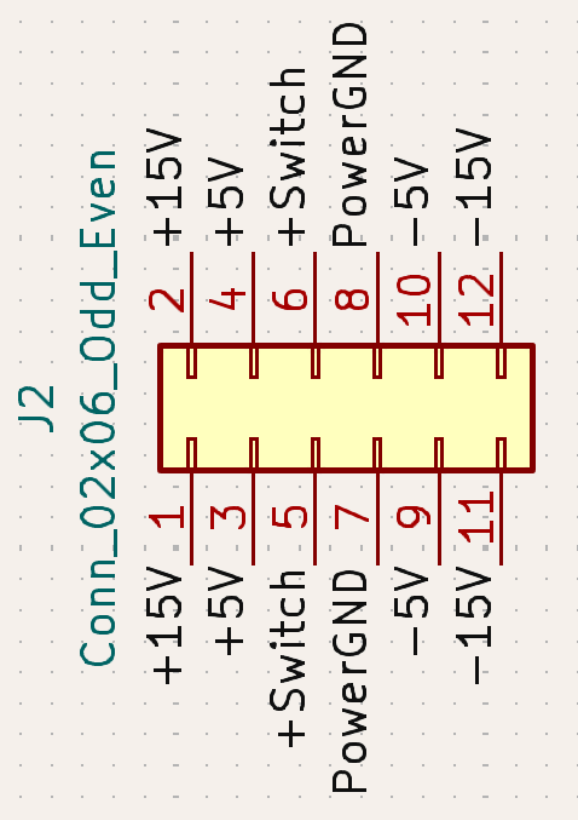
Note: The pins 11,12,29,30 are power and ground pins and so cannot be programmed. This is ensured in the mapping.

Due to the lack of time, PCB Lab didn't print our silkscreen. To identify the pin 1 in the FPGA header, look at the main PCB such that the RRAM connection header and the power header are towards your side with the FPGA header towards the right. In this orientation, the above image exactly matches the FPGA headers. So the bottom right pin will be pin 1.

While holding the PCB in the same orientation, the RRAM connection header and power header are as follows:



Note: The Vt and Hz pins are not in a serial order because of ease in routing. Do ensure this pinout when connecting.



Note: Here the upper and lower header are exactly the same, just for backup.

The `+15V` and `-15V` connect to the OpAmps, the `+5V` and `GND` connect to the DAC and ADC, and the `+Switch` and `-5V` connect to the Switches.
Currently for testing, we connected `+15V`, `+5V`, `+Switch` to +5V; `GND`, `-5V` to GND and `-15V` to –5V. For reliable switching, as per the datasheet, the following two combinations work:

	`+Switch`	`-5V`
1	+5V	GND
2	+9V	–5V