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Week 7 : Assignment 7

The due date for submitting this assignment has passed.

Due on 2025-03-12, 23:59 IST.

Assignment submitted on 2025-03-08, 19:18 IST

1) In a Flush+Reload attack targeting the last-level cache (LLC), what is the primary reason for using CLFLUSH instruction? ***1 point***

- To ensure cache coherency across cores
- To force the victim's data out of all cache levels without affecting memory
- To increase the speed of memory access
- To prevent cache pollution from other processes

Yes, the answer is correct.
Score: 1

Accepted Answers:
To force the victim's data out of all cache levels without affecting memory

2) Which property of modern CPU branch predictors makes Spectre Variant 2 possible? ***1 point***

- The use of a global history buffer
- The ability to train across different privilege levels
- The presence of a return stack buffer
- The implementation of ahead-of-time prediction

Yes, the answer is correct.

Score: 1

Accepted Answers:
The ability to train across different privilege levels

3) During a Prime+Probe attack, what determines the accuracy of timing measurements when probing cache sets? ***1 point***

- The CPU's maximum clock frequency
- The size of the cache line
- The number of ways in the cache set
- The resolution of the CPU's timestamp counter

Yes, the answer is correct.
Score: 1

Accepted Answers:
The resolution of the CPU's timestamp counter

4) In Meltdown attack implementation, why is exception handling crucial? ***1 point***

- To prevent system crashes during the attack
- To continue execution after accessing privileged memory
- To mask the attack from security monitoring
- To improve the attack success rate

Yes, the answer is correct.
Score: 1

Accepted Answers:
To continue execution after accessing privileged memory

5) What makes cache slice selection in modern Intel processors relevant to side-channel attacks? ***1 point***

- Complex hash functions determining cache slice mapping
- Dynamic slice allocation based on workload
- Hardware prefetcher interference
- ASLR implementation affecting slice selection

Yes, the answer is correct.
Score: 1

Accepted Answers:
Complex hash functions determining cache slice mapping

6) Which characteristic of speculative execution is specifically exploited in Spectre Variant 1? ***1 point***

- Out-of-order execution capabilities
- Branch direction prediction
- Memory disambiguation prediction
- Bounds check bypass during array access

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Yes, the answer is correct.
Score: 1
Accepted Answers:
Bounds check bypass during array access

7) When implementing a covert channel using cache timing, what primarily determines the channel's bandwidth? ***1 point***

- Cache replacement policy
- Number of distinct cache sets available
- Memory bus speed
- CPU pipeline depth

Yes, the answer is correct.
Score: 1
Accepted Answers:
Number of distinct cache sets available

8) Match the Following: ***1 point***

1. Spectre variant 1	A. Exploits branch prediction and speculative execution
2. Prime step in Prime+Probe	B. Uses performance counters to detect cache evictions
3. Flush+Reload on ARM	C. Relies on the manipulation of array bounds checking
4. DRAMA	D. Employs cache coherence protocol for cross-core attacks
5. Speculative buffer overflows	E. Fills specific cache sets with attacker-controlled data

- 1: A, 2:B, 3:C, 4:D, 5:E
- 1: C, 2:E, 3:B, 4:D, 5:A
- 1: C, 2:E, 3:D, 4:B, 5:A
- 1: A, 2:B, 3:D, 4:C, 5:E

Yes, the answer is correct.
Score: 1
Accepted Answers:
1: C, 2:E, 3:D, 4:B, 5:A

9) In a system with a 16-way set-associative L3 cache of size 16MB and cache line size of 64 bytes, how many cache sets are available for Prime+Probe attack targeting this cache?

16384

Yes, the answer is correct.
Score: 1
Accepted Answers:
(Type: Numeric) 16384

1 point

10) In modern Intel processors implementing inclusive cache hierarchy, evicting a cache line from LLC using CLFLUSH instruction guarantees its eviction from L1 and L2 caches as well. ***1 point***

- (●) True
- ( ) False

Yes, the answer is correct.
Score: 1

Accepted Answers:
True