CURRENT MIRROR:
CIRCUIT & THIER TOPOLOGIES

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CURRENT MIRROR: THEORY & SPECS

Key Types of MOS Current Mirrors

1. Simple Current Mirror

The **Simple Current Mirror** is the most straightforward current mirroring circuit, using two transistors—**M1** and **M2**—configured to mirror a reference current I_{REF} to the output. This structure relies on precise matching of transistor parameters (such as threshold voltage and gain factor) to achieve consistent current.

- **Pros**: Simplicity, minimal area usage, and ease of implementation make it valuable in designs where absolute current precision isn't critical.
- **Cons**: Output resistance is limited, which can degrade current matching with variations in output voltage. Channel-length modulation is a significant drawback, impacting performance when V_{OUT} changes.

2. Cascode Current Mirror

For applications requiring higher output resistance and less sensitivity to output voltage changes, the **Cascode Current Mirror** is preferred. This circuit adds an additional transistor layer (e.g., **M3** in cascode with **M2**), effectively increasing the output resistance and mitigating channel-length modulation effects.

- **Pros**: The cascode configuration provides higher impedance, significantly improving output accuracy by isolating the output node from variations in the drain-source voltage of the mirroring transistor.
- **Cons**: Increased headroom requirement due to the additional transistors, making it challenging to use in low-voltage designs.

3. Wide-Swing Cascode Current Mirror

In the **Wide-Swing Cascode Current Mirror**, the goal is to address the headroom limitation of traditional cascode mirrors while still benefiting from a high output resistance. This design modifies the gate biasing scheme of the cascode transistors, effectively allowing a **lower minimum supply voltage** without compromising on output resistance.

- **Pros**: Allows higher voltage swing at the output and is thus compatible with lower supply voltages, making it suitable for modern low-voltage applications.
- **Cons**: The gate-biasing circuit can increase design complexity and introduce dependencies on process variations.

4. Self-Biased Wide-Swing Cascode Current Mirror

The **Self-Biased Wide-Swing Cascode Current Mirror** further enhances the wide-swing mirror by incorporating a self-biasing mechanism. Self-biasing alleviates the need for external bias circuits, reducing design overhead and area, which is especially valuable in large-scale integrations (e.g., complex analog or mixed-signal systems).

- **Pros**: High output resistance, wide output swing, and the added benefit of stable self-biasing that adapts to variations, providing a robust and compact design.
- **Cons**: Self-biasing can be susceptible to process and temperature variations if not carefully managed, potentially impacting long-term stability.

Summary:

Each current mirror type presents a unique trade-off between accuracy, headroom, output swing, and complexity:

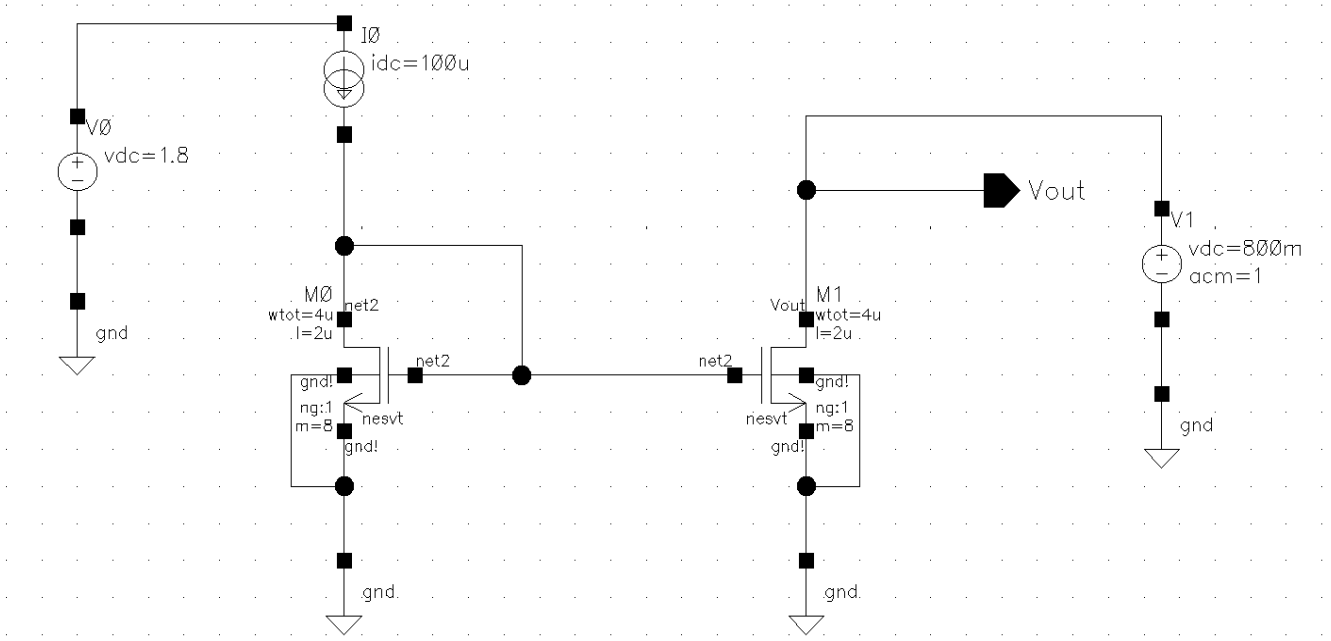
- **Simple Current Mirror**: Ideal for low-power, non-critical biasing circuits.
- **Cascode Current Mirror**: Provides high accuracy and is preferred in precision circuits but requires higher supply voltage.
- **Wide-Swing Cascode Current Mirror**: Balances high output resistance with low headroom, ideal for low-voltage applications.
- **Self-Biased Wide-Swing Cascode Current Mirror**: Offers wide swing and high impedance with a streamlined design, suitable for large-scale, integrated low-power circuits.

Specifications Required for Current Mirrors:

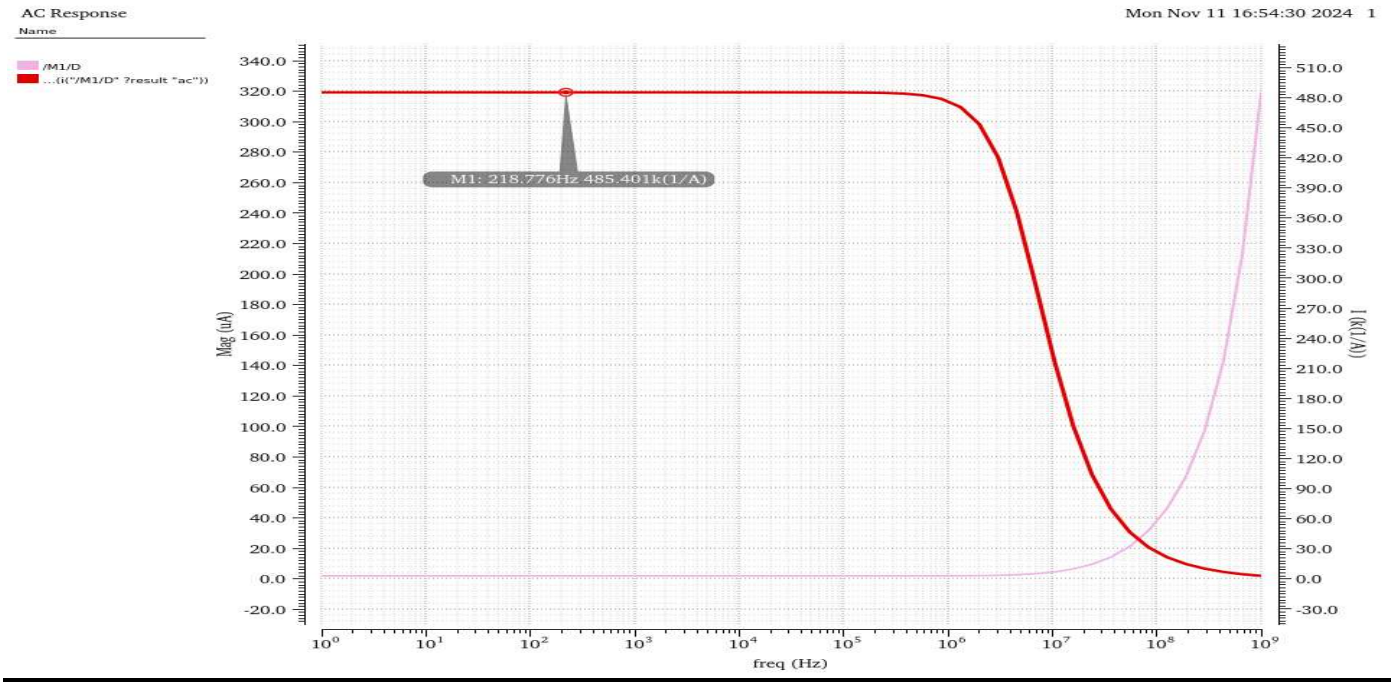
Specification	**Requirement**
Output Resistance	High output resistance to minimize current variation with changes in output voltage
Input Resistance	Low input resistance for accurate reference current setting and efficient current transfer
Linear I_{OUT} vs. I_{IN}	Slope of 1 for the I_{OUT} vs. I_{IN} characteristic, ensuring accurate current mirroring
Voltage Swing	High output voltage swing to enable operation across a wide range without compromising saturation

1. Simple Current Mirror:

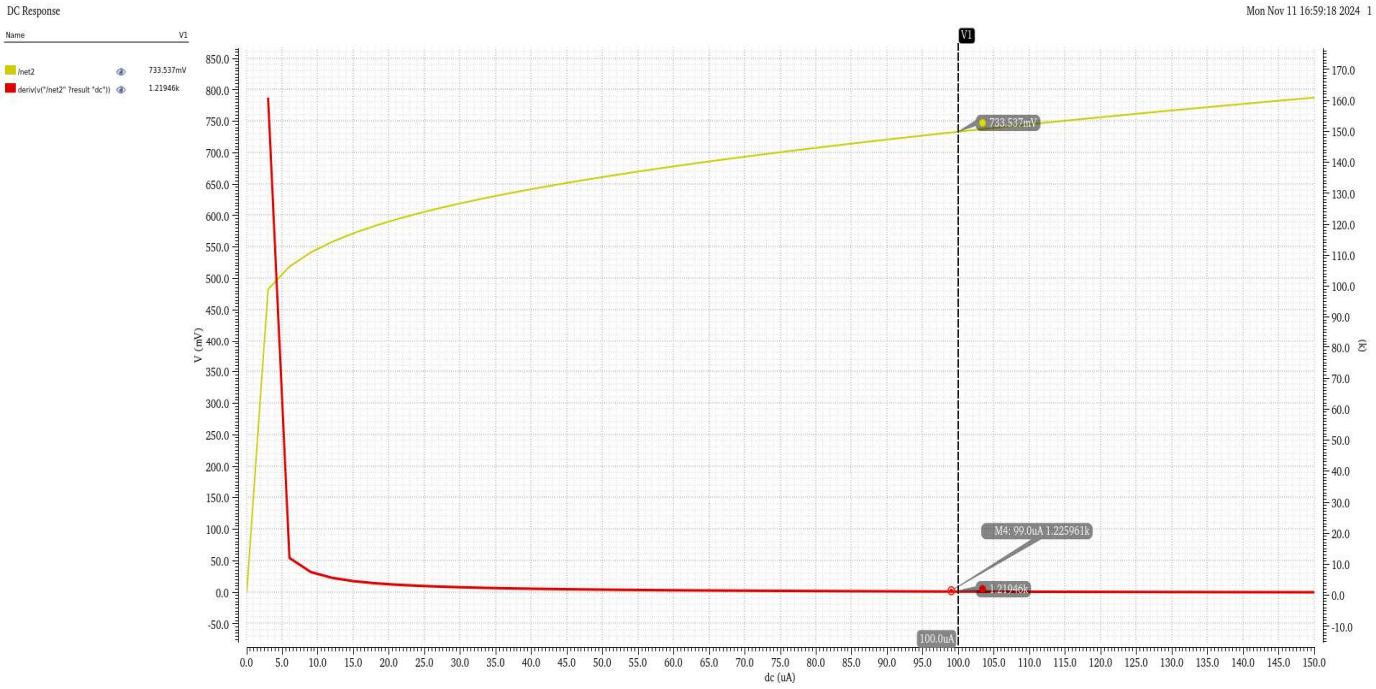
Schematic:



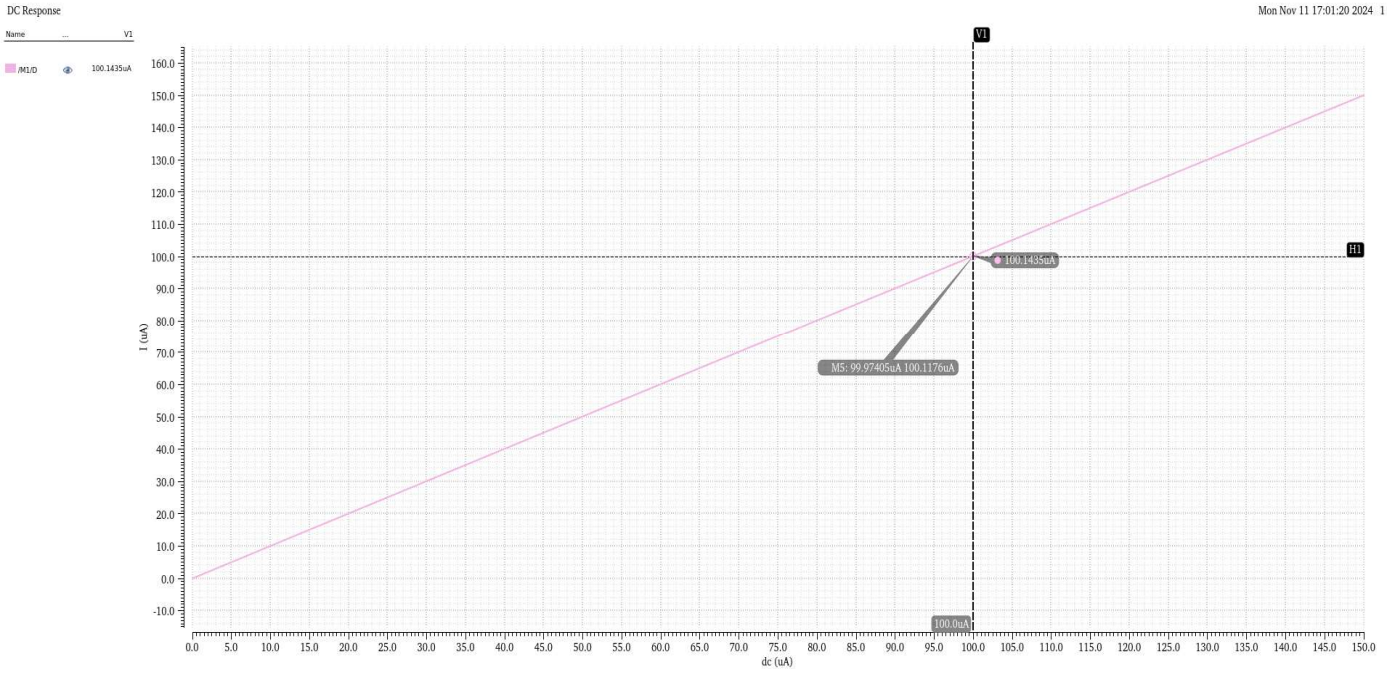
Simulation (Calculating Rout): $R_{out} = r_{o1}$ (where r_o denotes output resistance of a transistor)



Input Resistance: $R_{in} = 1/gm_o$ (where gm denotes the transconductance of the transistor)

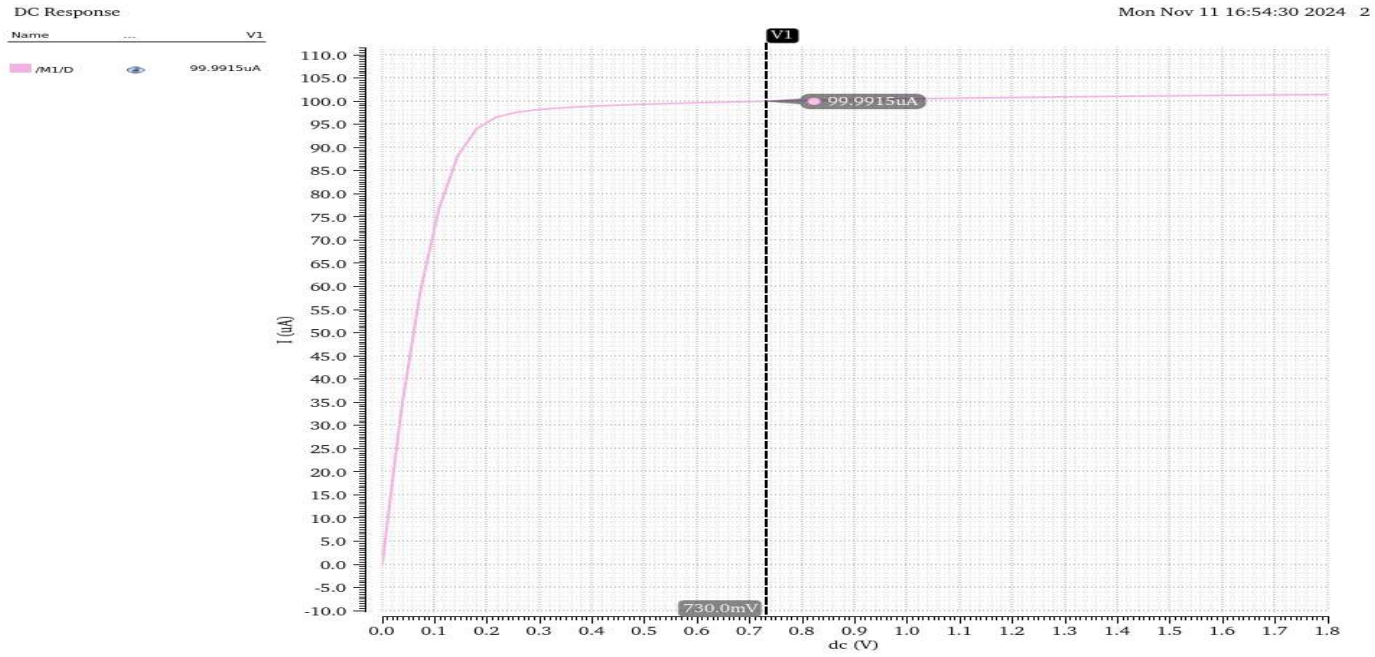


Iout v/s Iin plot:



NOTE: We observe a straight line here with slope = 1.

Vout(min) for accurate mirroring:

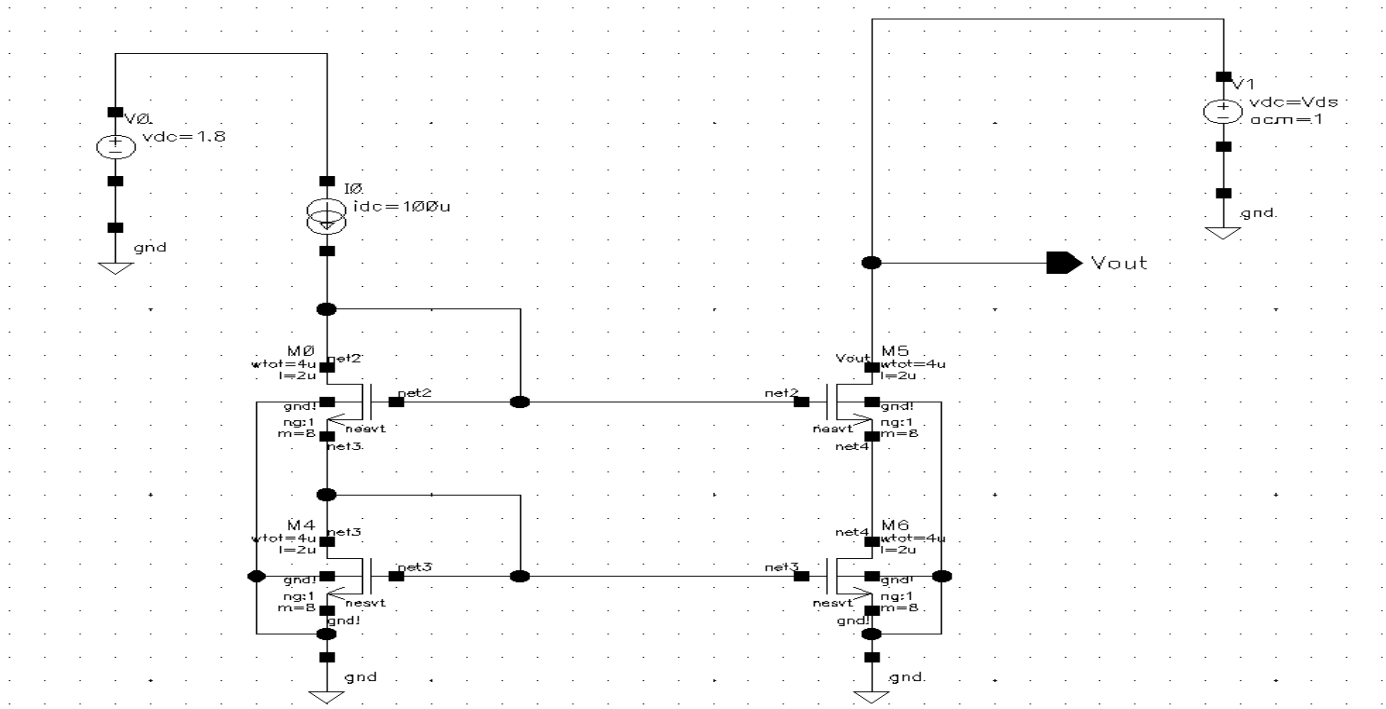


Observations:

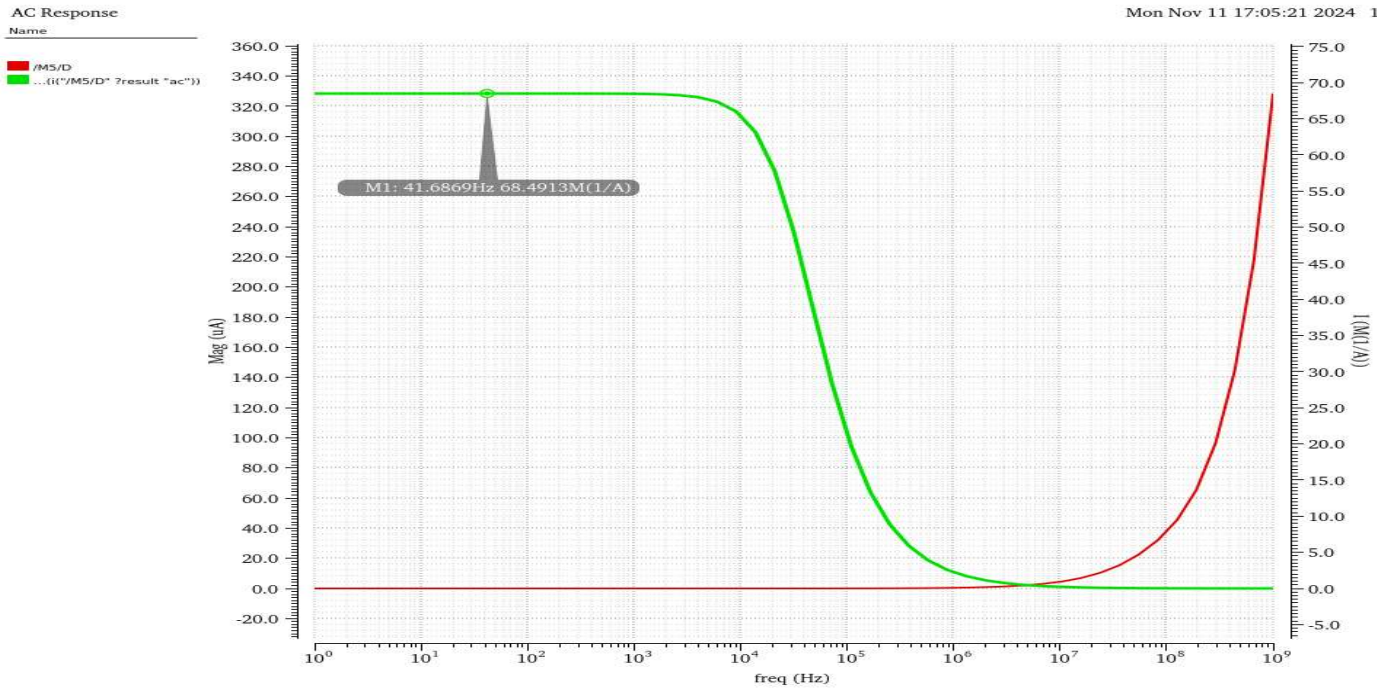
Rout	485.4 kΩ
Rin	1.22 kΩ
Vout(min)	730 mV

2. Cascode Current Mirror:

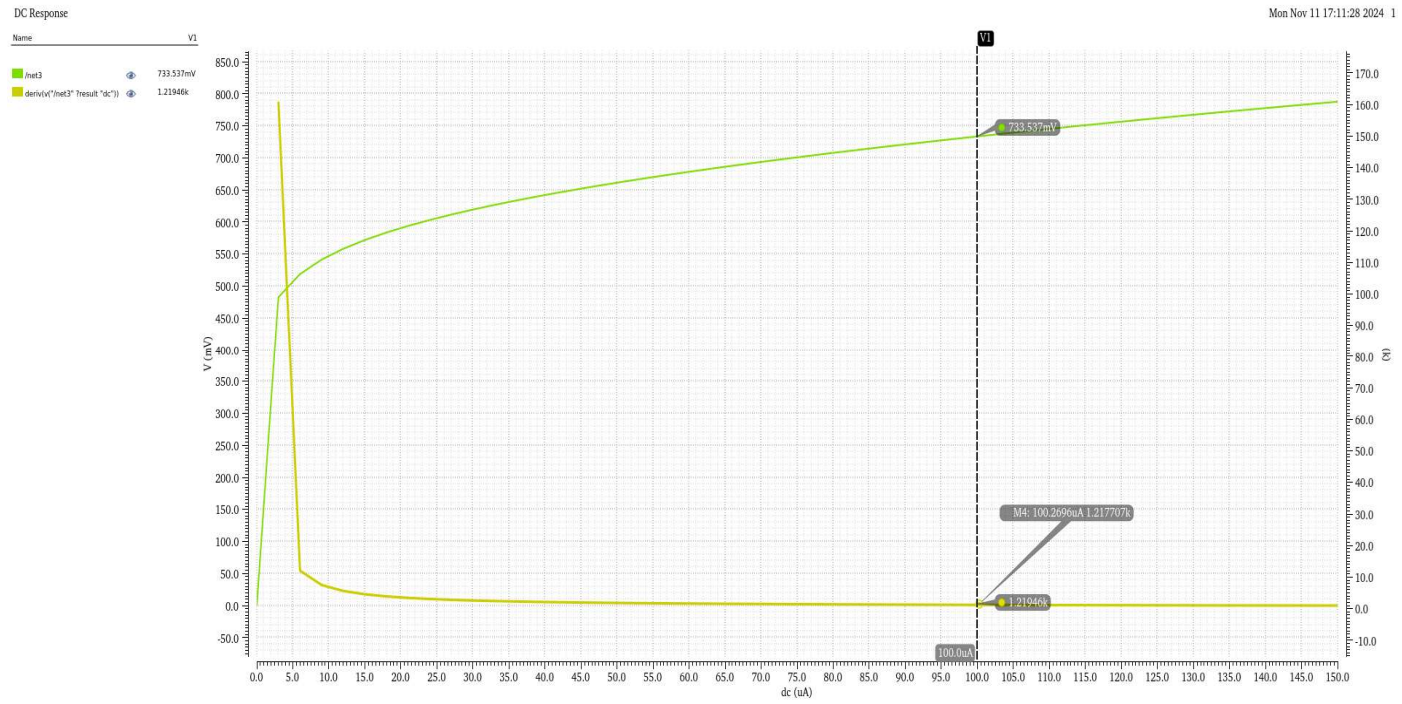
Schematic:



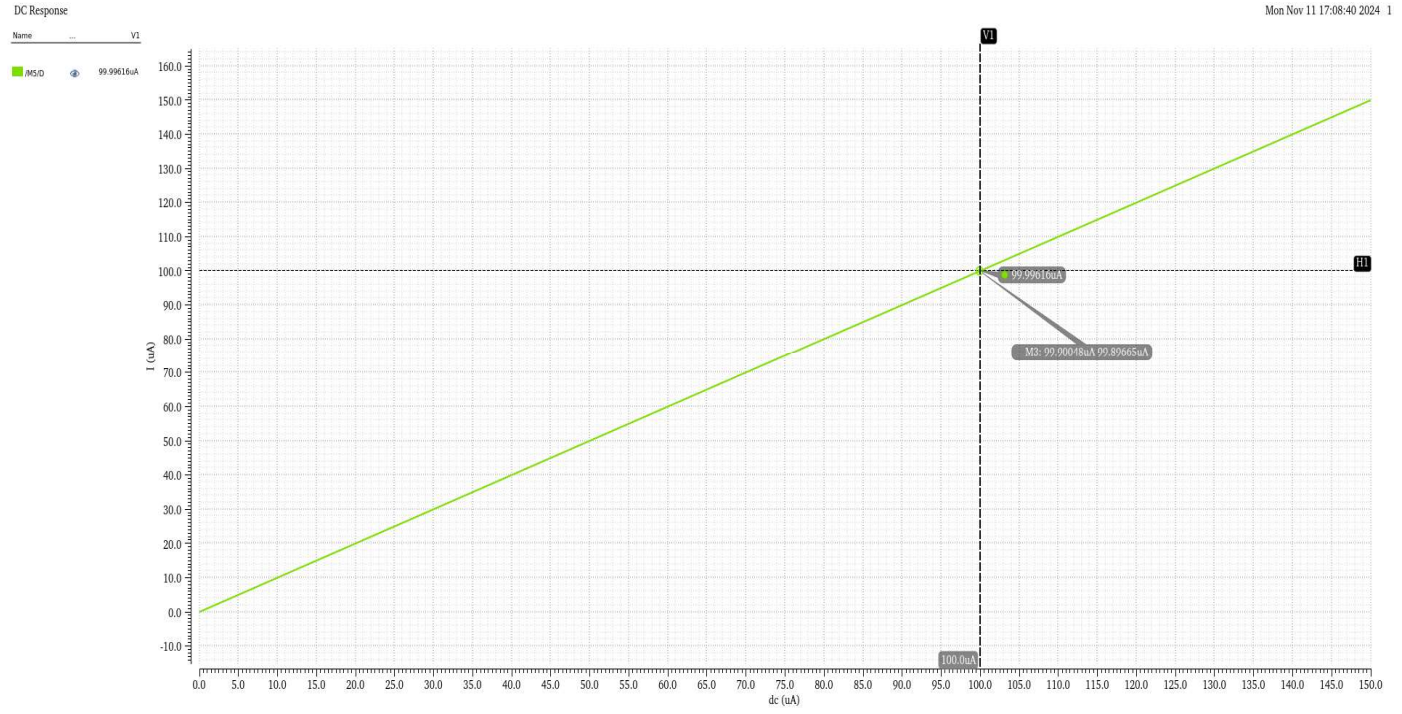
Simulation (Calculating Rout): $R_{out} = gm_5 * r_{o5} * r_{o6}$



Input Resistance: $R_{in} = 1/gm_4$

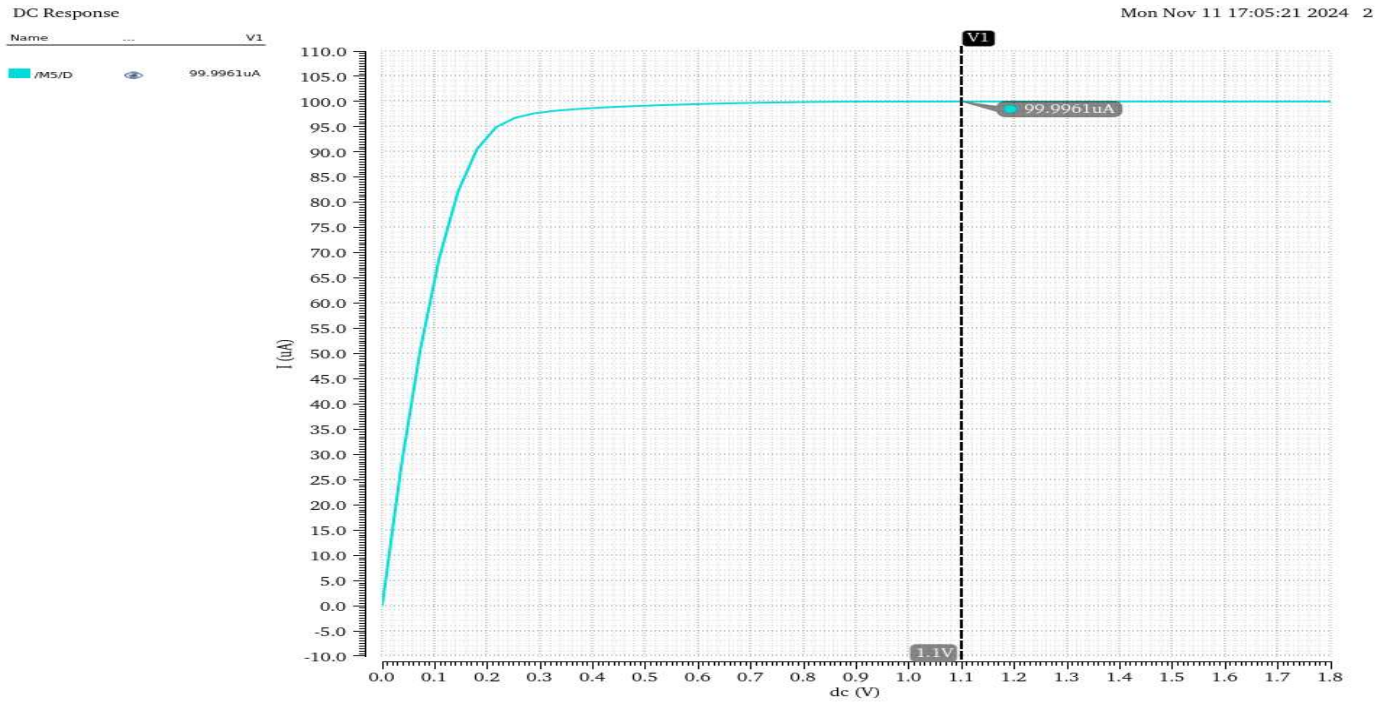


Iout v/s Iin plot:



NOTE: We observe a straight line here with slope = 1.

Vout(min) for accurate mirroring:

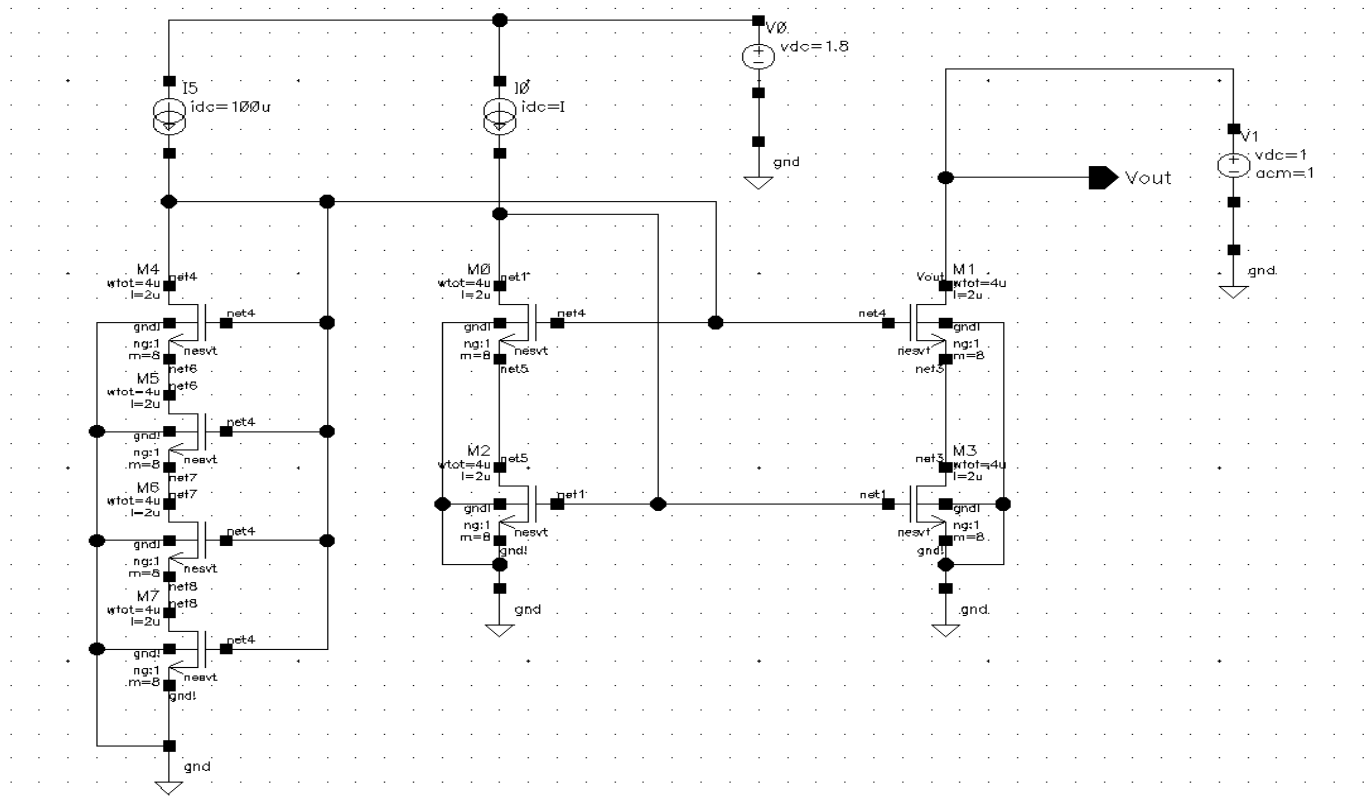


Observations:

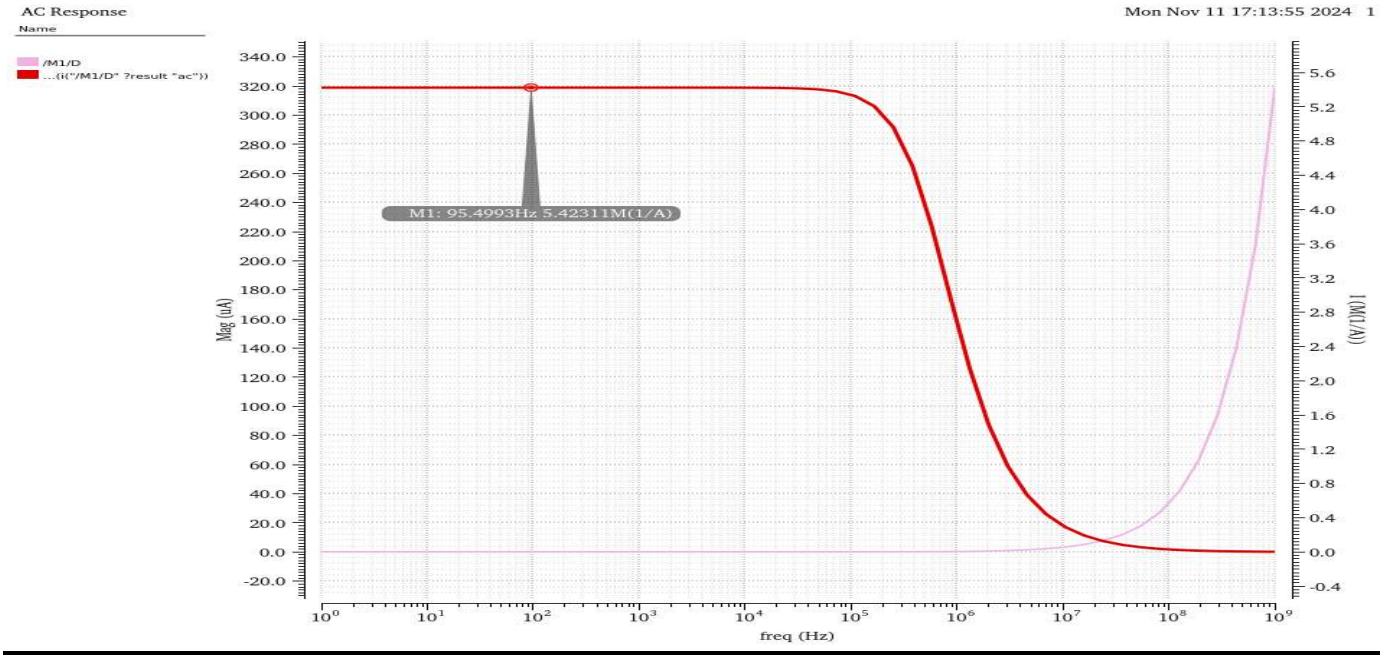
Rout	68.5 MΩ
Rin	1.22 kΩ
Vout(min)	1.1 V

3. Wide Swing Cascode Current Mirror:

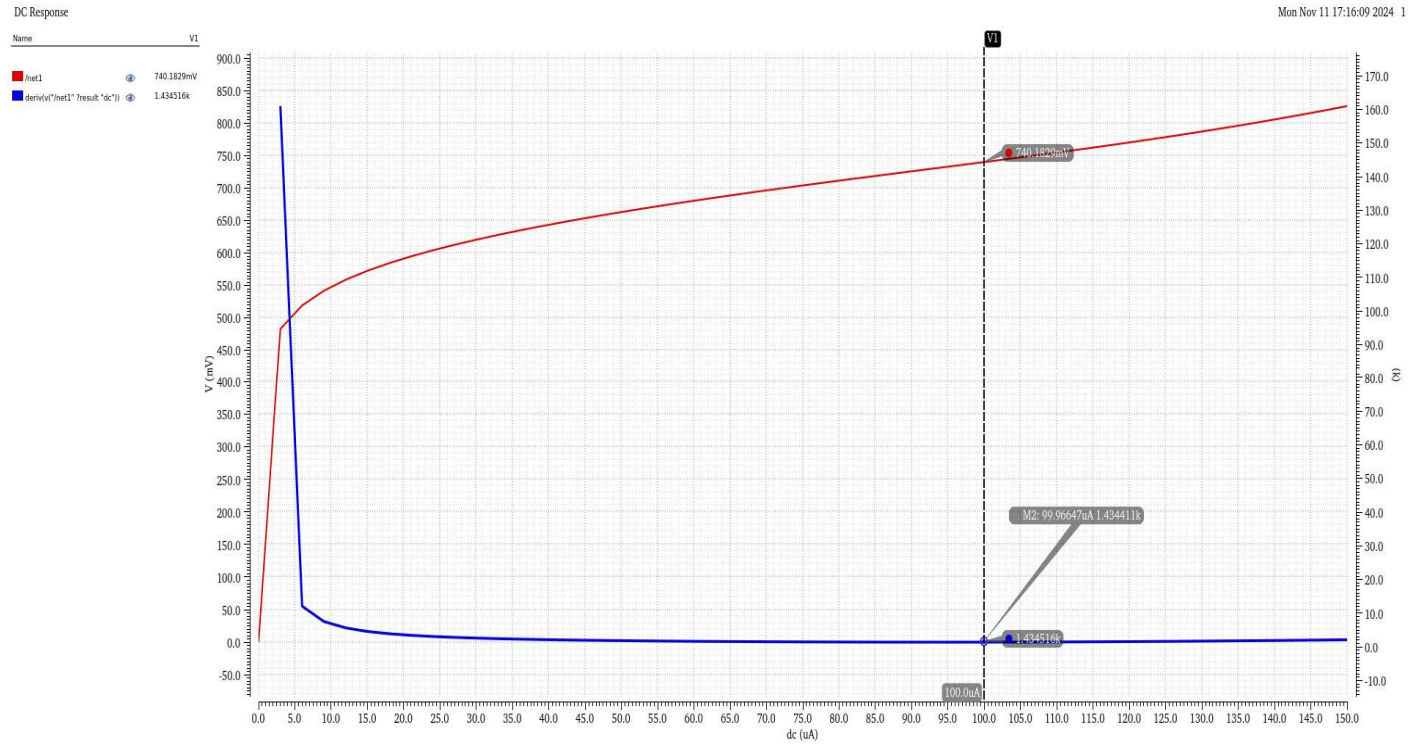
Schematic:



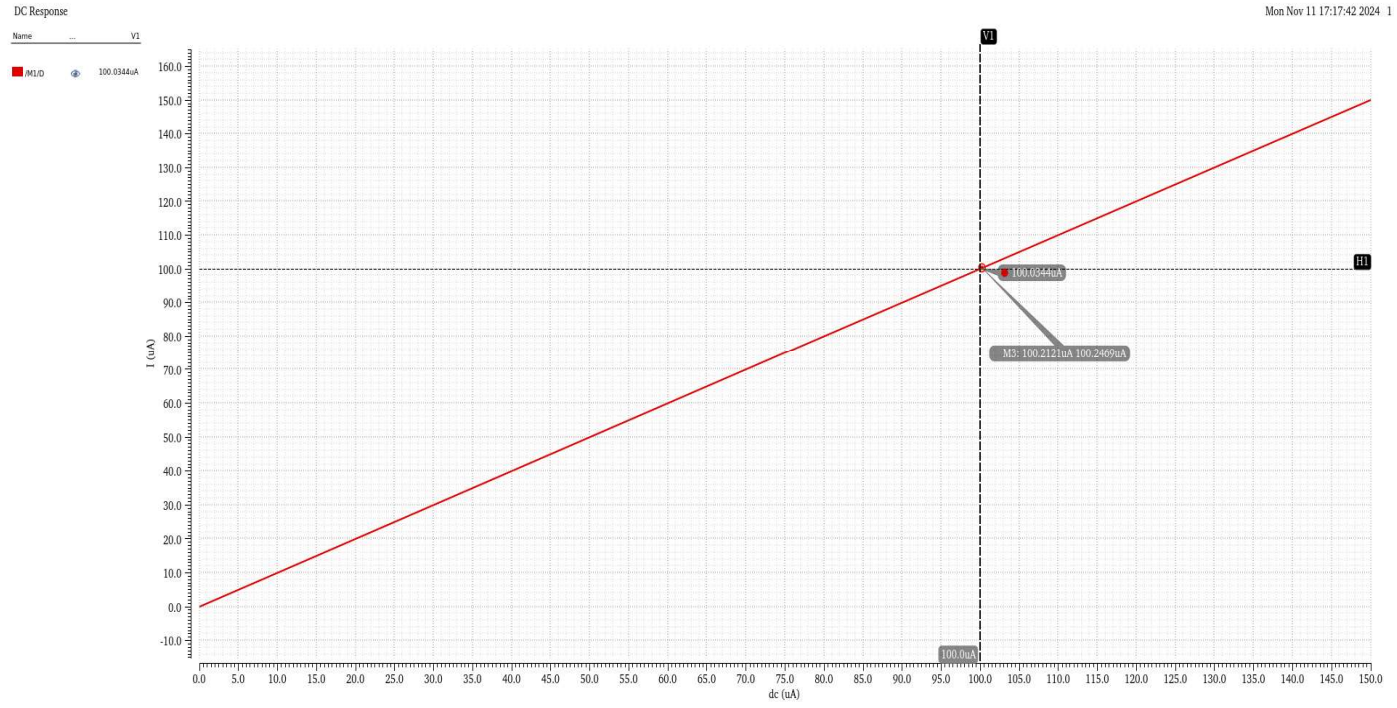
Simulation (Calculating Rout): $R_{out} = gm_1 * r_{o1} * r_{o3}$



Input Resistance: $R_{in} = 1/gm_2$

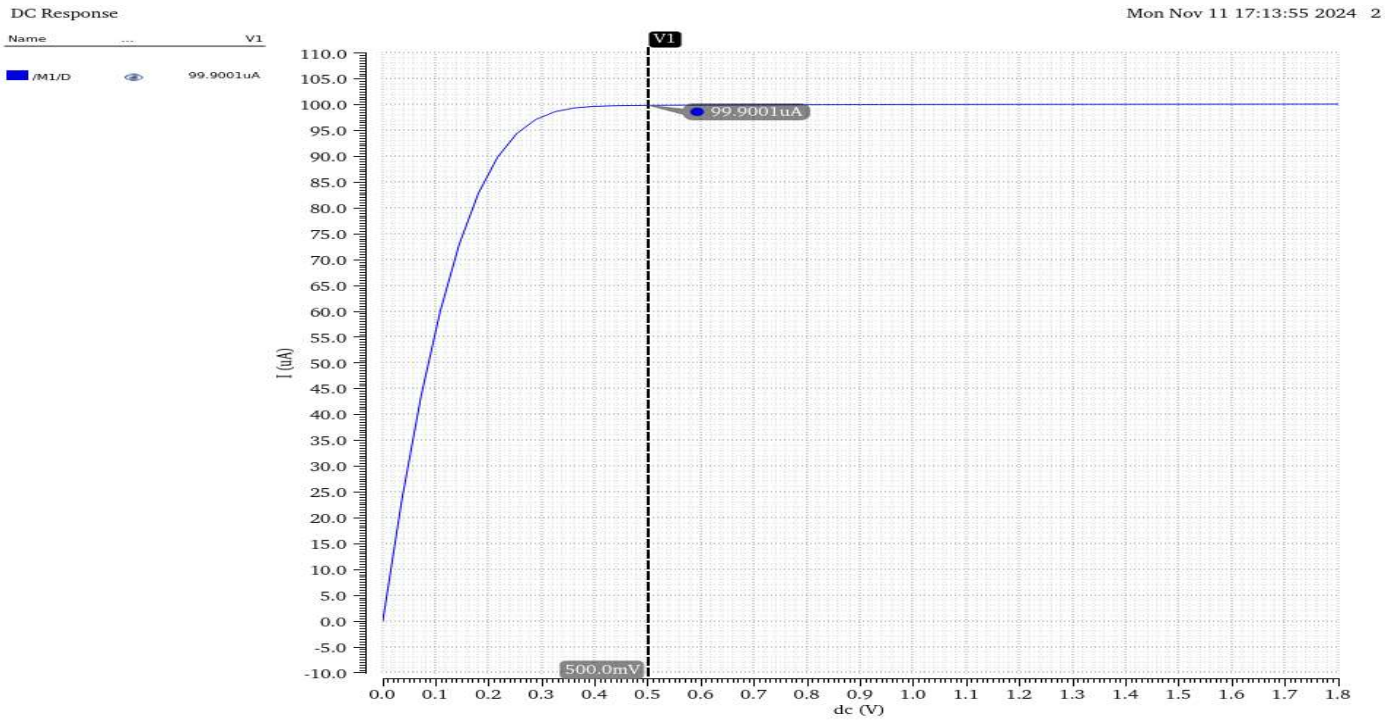


Iout v/s Iin plot:



NOTE: We observe a straight line here with slope = 1.

Vout(min) for accurate mirroring:

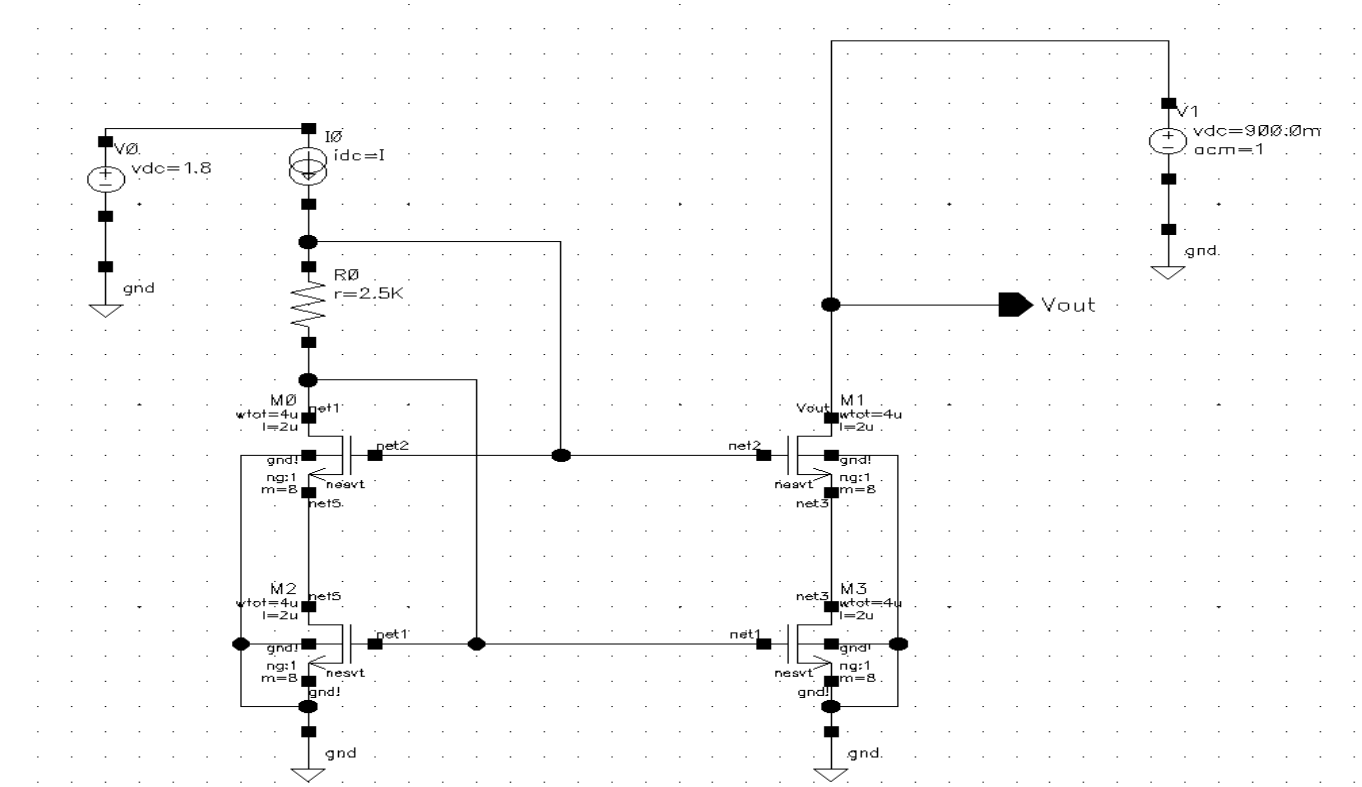


Observations:

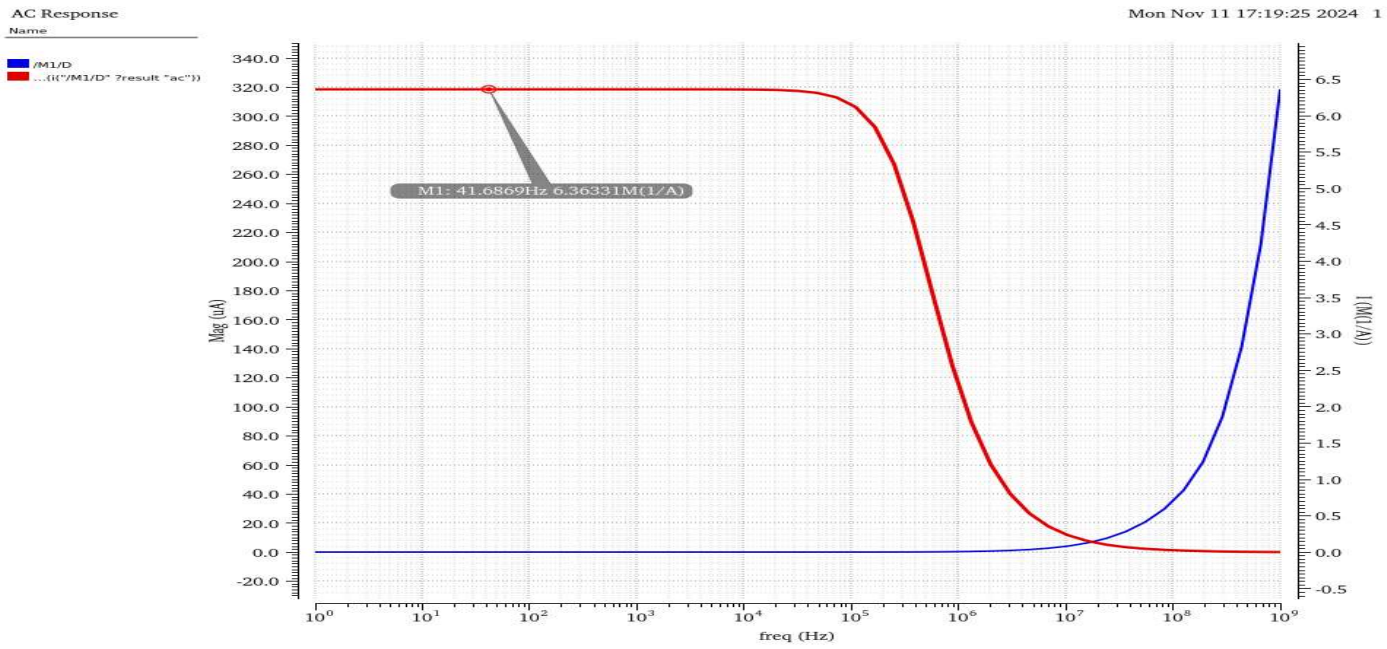
Rout	5.42 MΩ
Rin	1.44 kΩ
Vout(min)	500 mV

4. Self-biased Wide Swing Cascode Current Mirror:

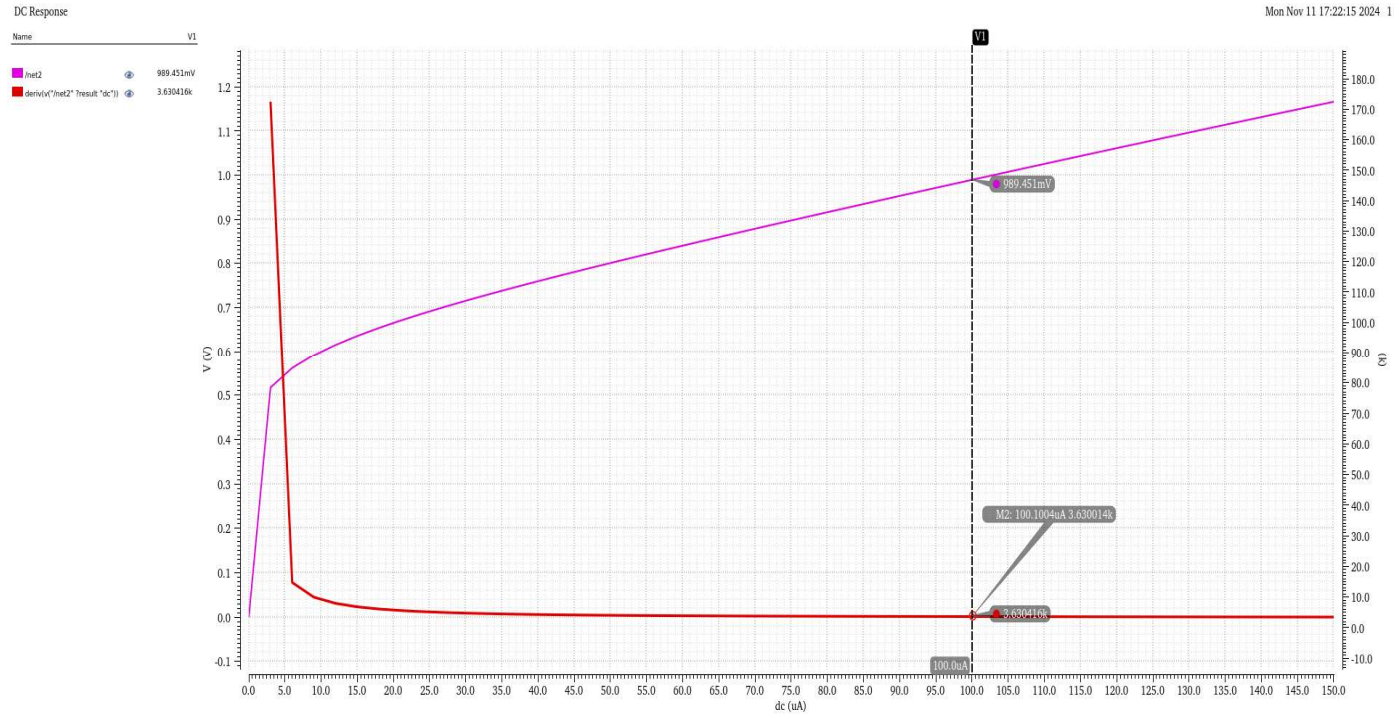
Schematic:



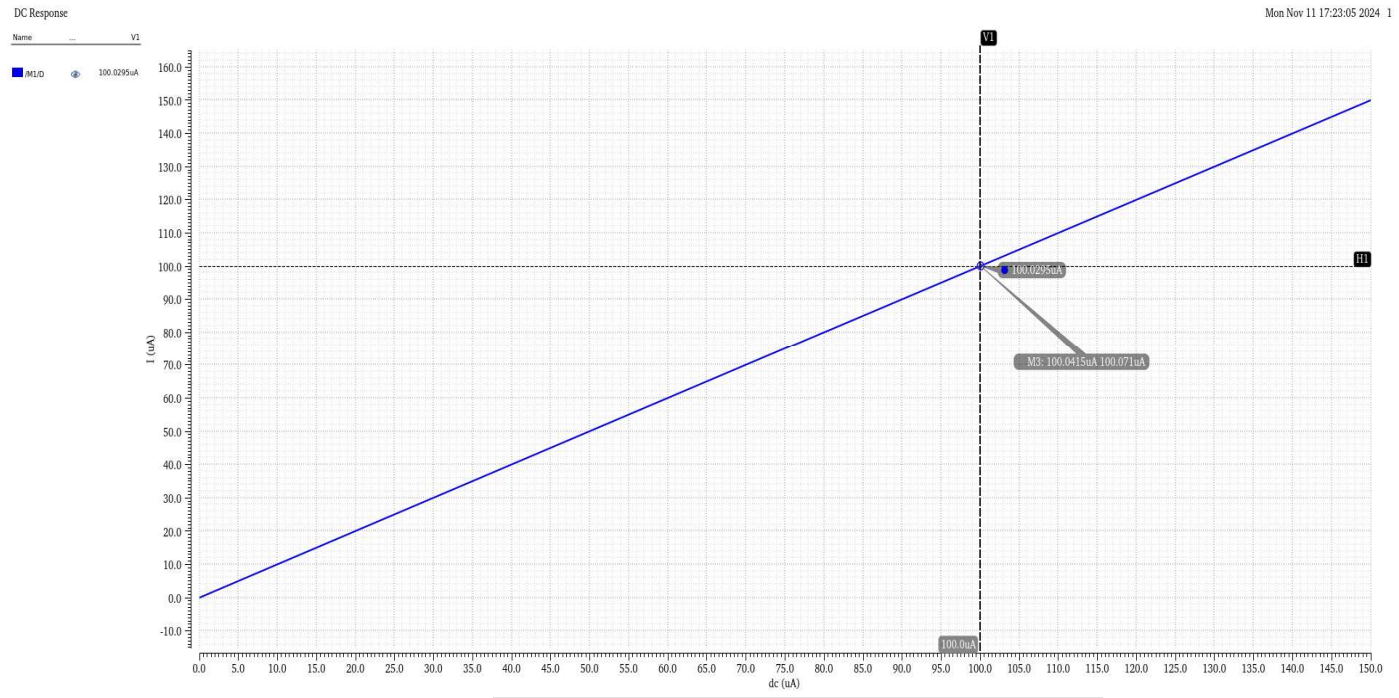
Simulation (Calculating Rout): $R_{out} = gm_1 * r_{o1} * r_{o3}$



Input Resistance: $R_{in} = r + 1/gm_2$ (here, r = 2.5kΩ)

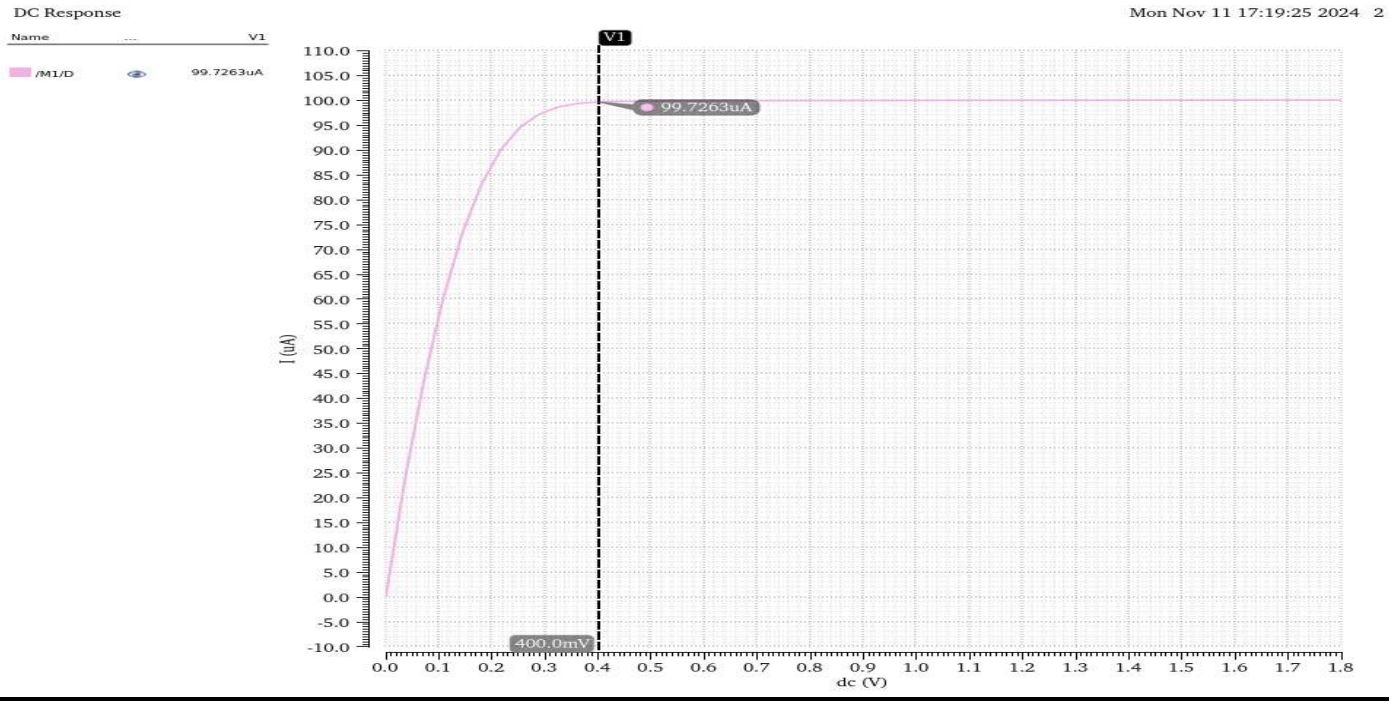


Iout v/s Iin plot:



NOTE: We observe a straight line here with slope = 1.

Vout(min) for accurate mirroring:



Observations:

Rout	6.36 MΩ
Rin	3.63 kΩ
Vout(min)	400 mV