BALANCED AMPLIFIER

Required specs for the amplifier:

Technology	180nm
Supply Voltage	1.8V ± 10%
Power Consumption	≤ 0.3 mW
Voltage Gain	≥ 50 dB
Load	10 pF
Unity Gain Bandwidth	≥ 10 MHz
Slew Rate	10 V/μsec
Phase Margin	≥ 60º

Balanced Amplifier: Theory

A **balanced amplifier** is a type of analog amplifier designed to amplify differential signals while rejecting common-mode signals. This configuration is highly valued in analog circuit design due to its ability to improve noise immunity, increase linearity, and provide better performance in systems requiring differential signal processing, such as communication systems, instrumentation, and analog front-ends.

Key Characteristics

1. **Common-Mode Rejection Ratio (CMRR):**
   The ability of a balanced amplifier to reject common-mode signals is quantified by the **Common-Mode Rejection Ratio (CMRR)**, which is defined as:

   $$\mathbf{CMRR = 20 \cdot \log_{10}(A_{diff}/A_{cm})}$$

   Where A_{diff} is the differential gain, and A_{cm} is the common-mode gain. A high CMRR is desirable for robust noise immunity.

2. **Gain:**
   - **Differential Gain (Adiff):** This is the gain applied to the differential input signal.

     $$\mathbf{Vout_{,diff} = A_{diff} \cdot Vin_{,diff}}$$

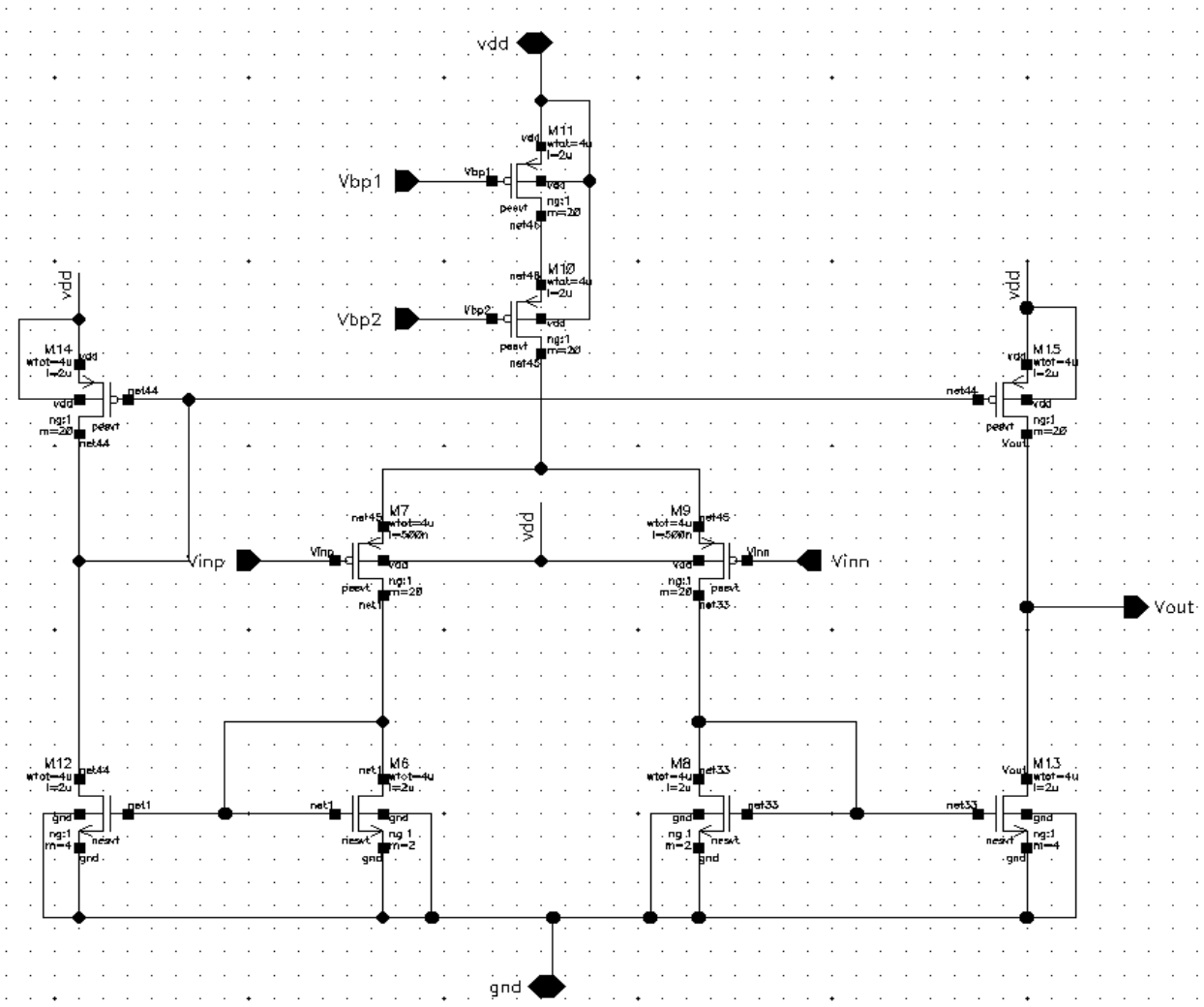
   - **Common-Mode Gain (Acm):** Ideally, the common-mode gain should be zero, meaning no amplification of common-mode signals occurs.
3. **Impedance Matching:**
   Balanced amplifiers typically exhibit matched input and output impedances, which is critical in high-frequency applications to minimize signal reflections and distortions.
4. **Linearity:**
   The balanced configuration improves linearity by symmetrically processing the differential signals, reducing harmonic distortion.

Design and Implementation

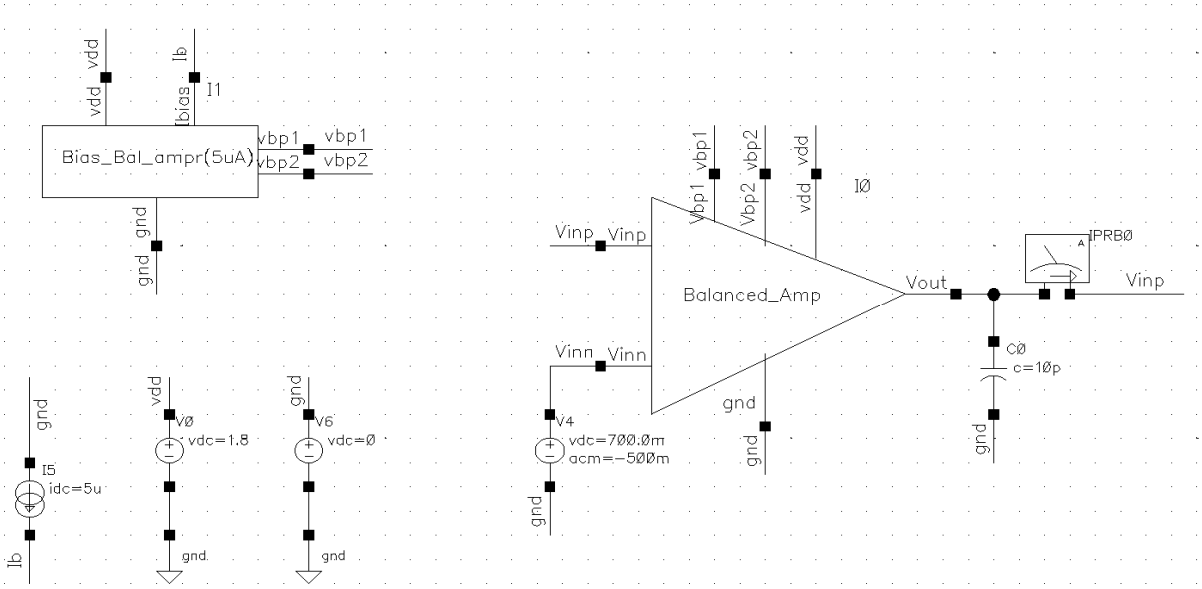
1. **Core Components:**
   - The input stage is often implemented using a **differential pair**, which provides the necessary differential-to-single-ended or differential-to-differential conversion.
   - The load can be resistive or active (e.g., current mirrors) depending on gain and linearity requirements.
   - The output stage ensures proper drive capability for subsequent stages or loads.

2. **Feedback Mechanisms:**
   Negative feedback is commonly employed in balanced amplifiers to enhance linearity, reduce distortion, and improve overall stability.
3. **Symmetry:**
   A critical design requirement for balanced amplifiers is maintaining symmetry between the two signal paths. Mismatches can degrade the CMRR and introduce distortion. Techniques such as matched transistors and precise layout are used to ensure symmetry.
4. **Biasing:**
   Proper biasing is essential for optimal performance, ensuring that the amplifier operates in the desired region (e.g., active region for MOSFETs).

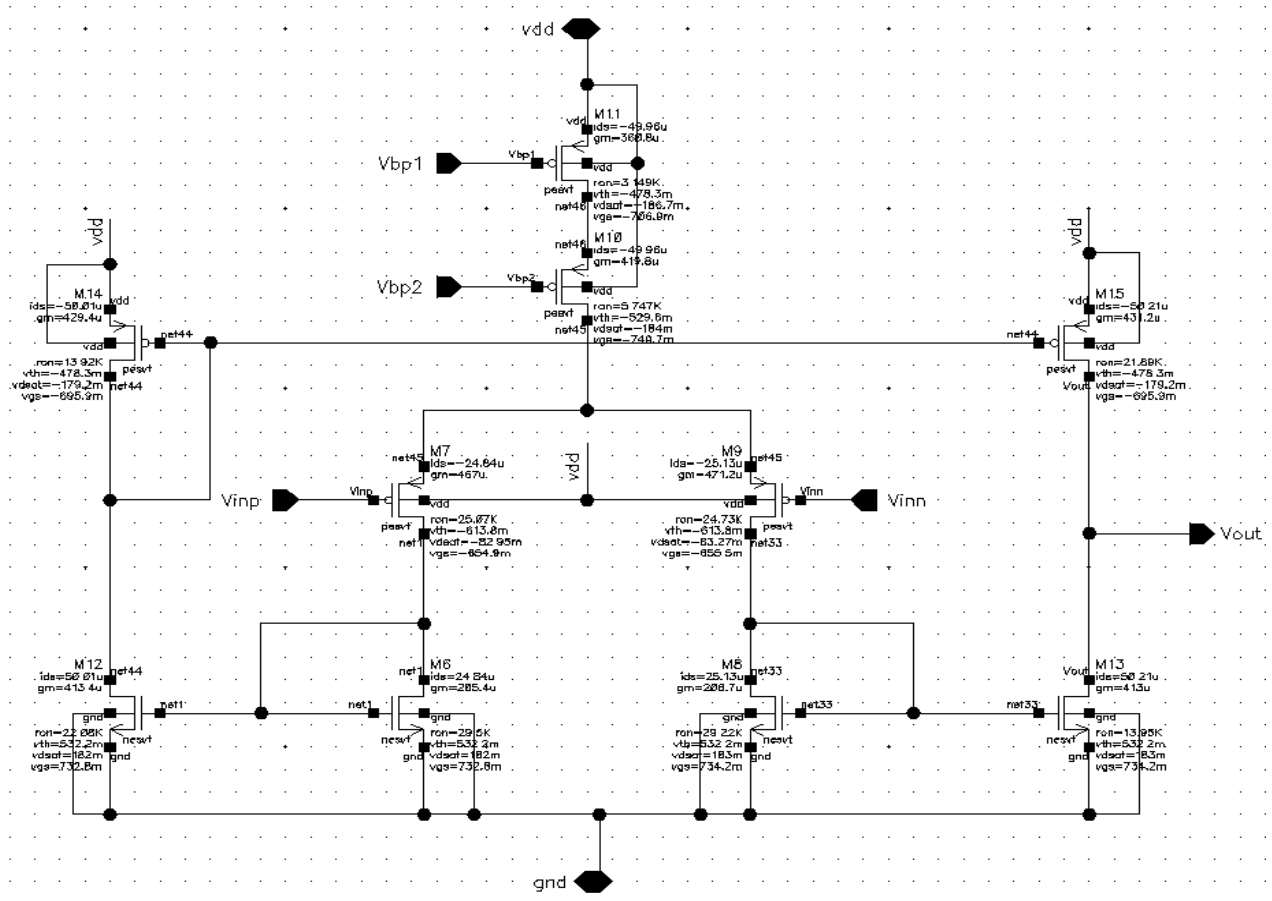
Schematic of Balanced Amplifier:



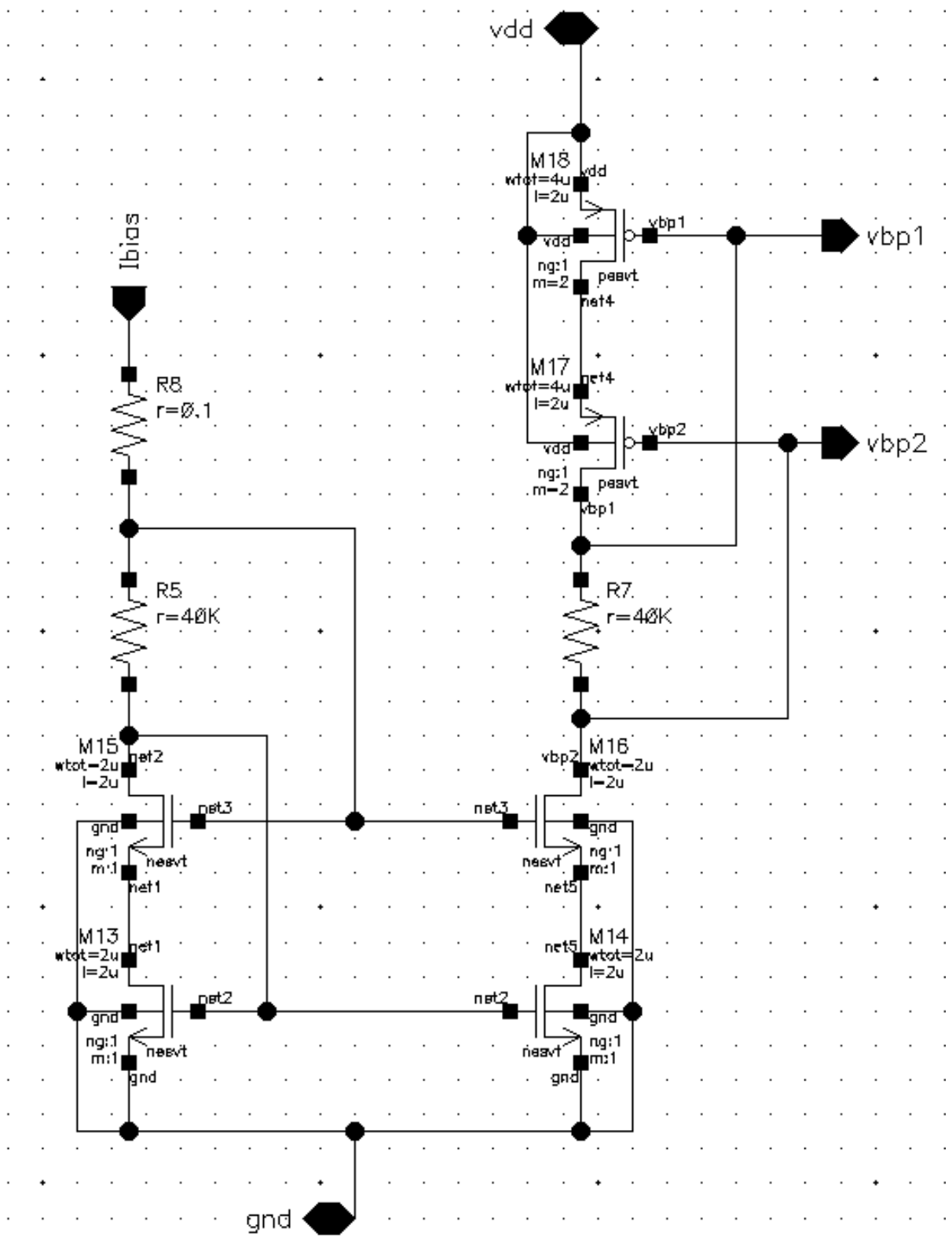
Closed loop simulation (Balanced Amp):



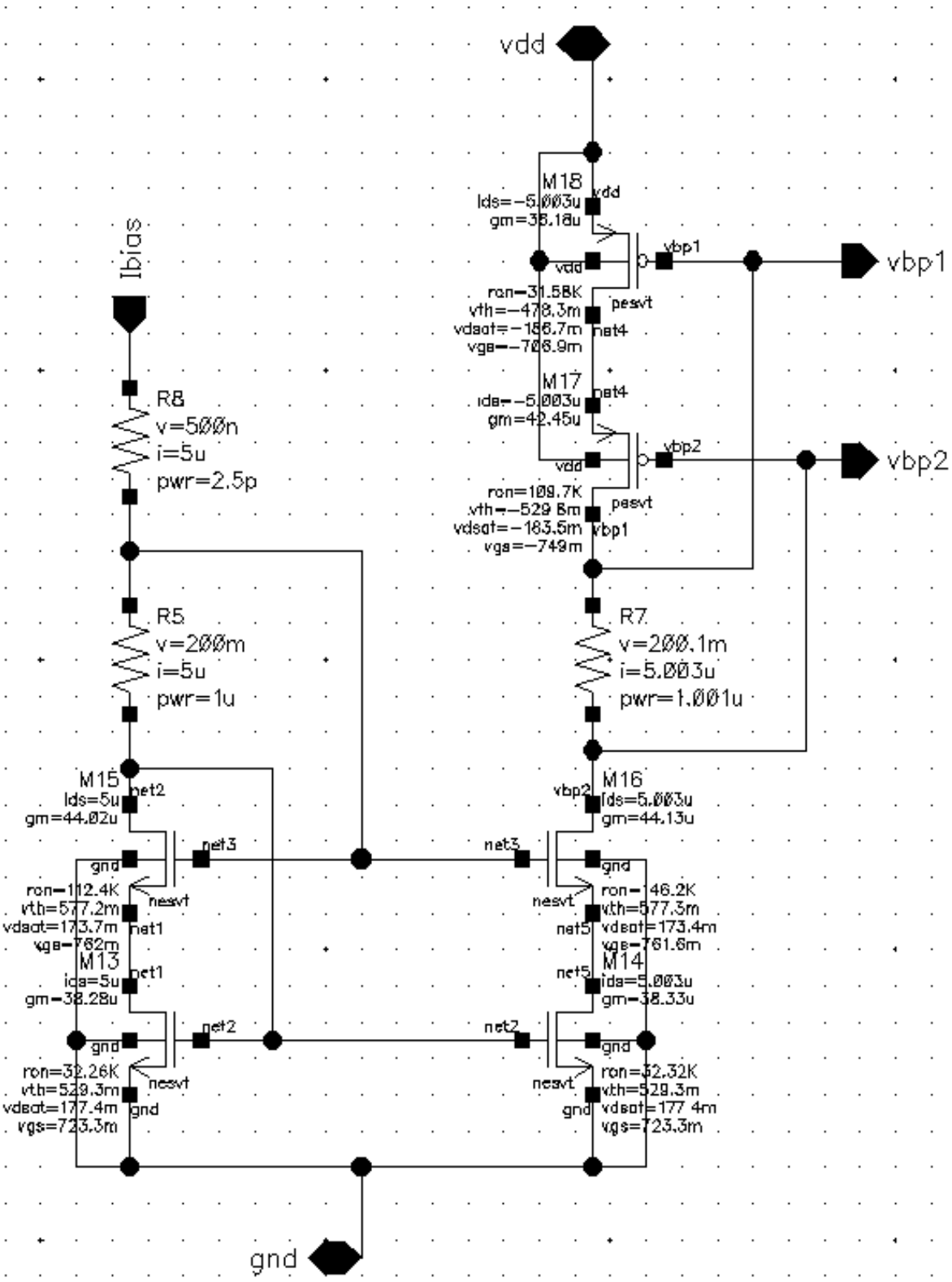
Schematic (Balanced Amp) DC op point:



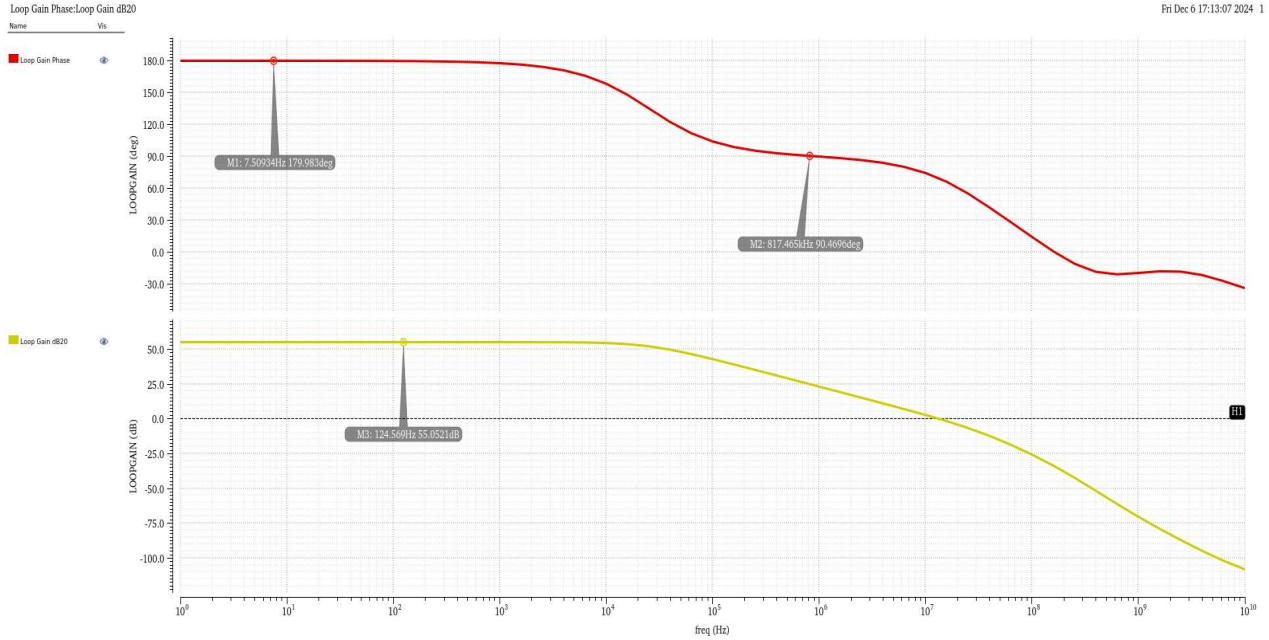
Bias circuit (Balanced Amp):



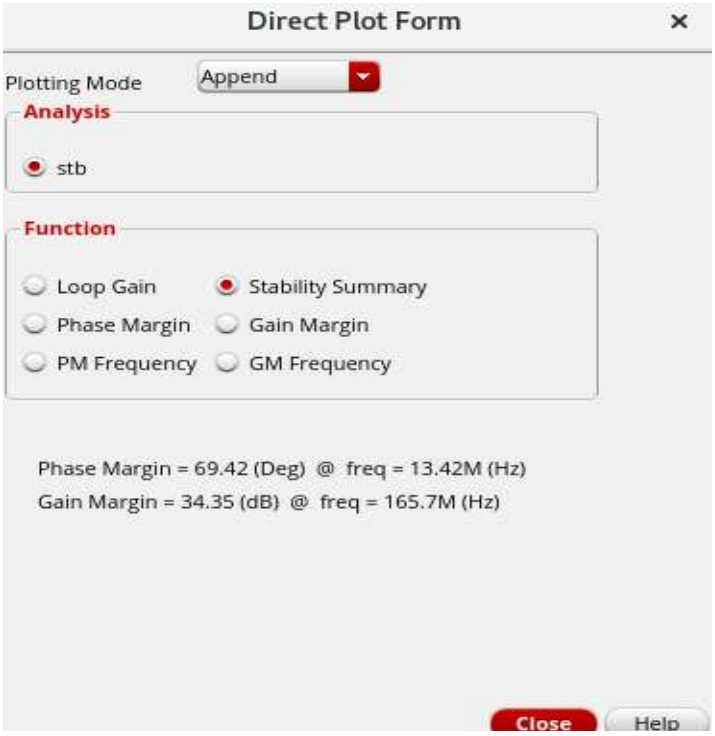
Bias circuit with DC op point (Balanced Amp):



Voltage Gain and Phase:



Stability Summary (Balanced Amp):



Required v/s Achieved Spec for the Balanced Amplifier:

	Required	**Achieved**
Power Consumption	≤ 0.3 mW	0.28 mW
Voltage Gain	≥ 50 dB	55 dB
Unity Gain Bandwidth	≥ 10 MHz	13.42 MHz
Slew Rate	10 V/µsec	10V/ µsec
Phase Margin	≥ 60º	69.42 º
Supply Voltage	1.8V ± 10%	1.8V