TWO-STAGE MILLER COMPENSATED OTA

Required specs for the OTA:

Technology	180nm
Supply Voltage	1.8V ± 10%
Power Consumption	≤ 0.4 mW
Voltage Gain	90 dB
Load	10 pF
Unity Gain Bandwidth	≥ 5 MHz
Slew Rate	20 V/μsec
Phase Margin	≥ 60º
ICMR	1V – 1.6V

Two-Stage Miller Compensated OTA: Theory

A two-stage operational trans-conductance amplifier (OTA) is a widely used configuration in analog circuit design due to its simplicity and ability to achieve high gain and drive capacitive loads. The inclusion of Miller compensation ensures stability, especially when the amplifier is used in feedback applications.

Structure

The two-stage OTA consists of:

1. **First Stage:** A differential amplifier, which provides high input impedance, large gain, and differential-to-single-ended signal conversion. Typically, a differential pair is used with a current mirror load.
2. **Second Stage:** A common-source amplifier, which provides additional voltage gain and acts as the primary driver for the output.

Miller Compensation

To stabilize the OTA in closed-loop configurations, a compensation technique called *Miller compensation* is employed. A compensation capacitor Cc is connected between the output of the second stage and the input of the first stage.
This capacitor introduces a dominant pole in the transfer function of the amplifier, effectively reducing the bandwidth and ensuring phase margin is sufficient for stability.

Key Design Considerations

1. **Gain and Bandwidth:**
   - The total gain Av is the product of the gains of the two stages: $Av = A1 \times A2$
   - The bandwidth is determined by the location of the dominant and non-dominant poles. Miller compensation pushes the dominant pole to a lower frequency, ensuring that the non-dominant pole does not degrade stability.
2. **Stability:**
   - Stability is measured by the phase margin, which is the difference between the phase lag at the unity-gain frequency and 180°. Proper sizing of Cc ensures a phase margin of 45°–60°, which is optimal for most applications.
3. **Slew Rate:**
   - The compensation capacitor affects the slew rate since it requires a large current to charge or discharge. To maintain a high slew rate, the trans-conductance of the second stage (gm_2) should be sufficiently high.
4. **Power Consumption:**
   - A trade-off exists between achieving high gain-bandwidth product and minimizing power consumption. Proper biasing of the amplifier ensures an efficient design.

Transfer Function and Poles in a Two-Stage OTA

The small-signal transfer function of the two-stage Miller-compensated OTA is derived from the equivalent small-signal model of the circuit. The overall transfer function can be expressed as:

$$A(s)=A_0/(1-s/p1)(1-s/p2)$$

Where:

- p1 is the **dominant pole**, located at a low frequency.
- p2 is the **non-dominant pole**, located at a higher frequency.

Effect of Miller Compensation

In a two-stage OTA, the uncompensated poles typically occur at relatively high frequencies, leading to stability issues when the OTA is used in a feedback loop. Miller compensation is employed to push the dominant pole to a lower frequency while moving the non-dominant pole further away from the origin.

A **Miller capacitor** (Cc) is placed between the output of the second stage and the output of the first stage. This capacitor introduces a feedback current proportional to the rate of change of voltage, which modifies the locations of the poles.

Zero Introduced by Miller Compensation

The Miller compensation capacitor also introduces a **right-half-plane (RHP) zero**, which can negatively impact the phase margin. The RHP zero is located at:

$$Z \approx +gm2/Cc$$

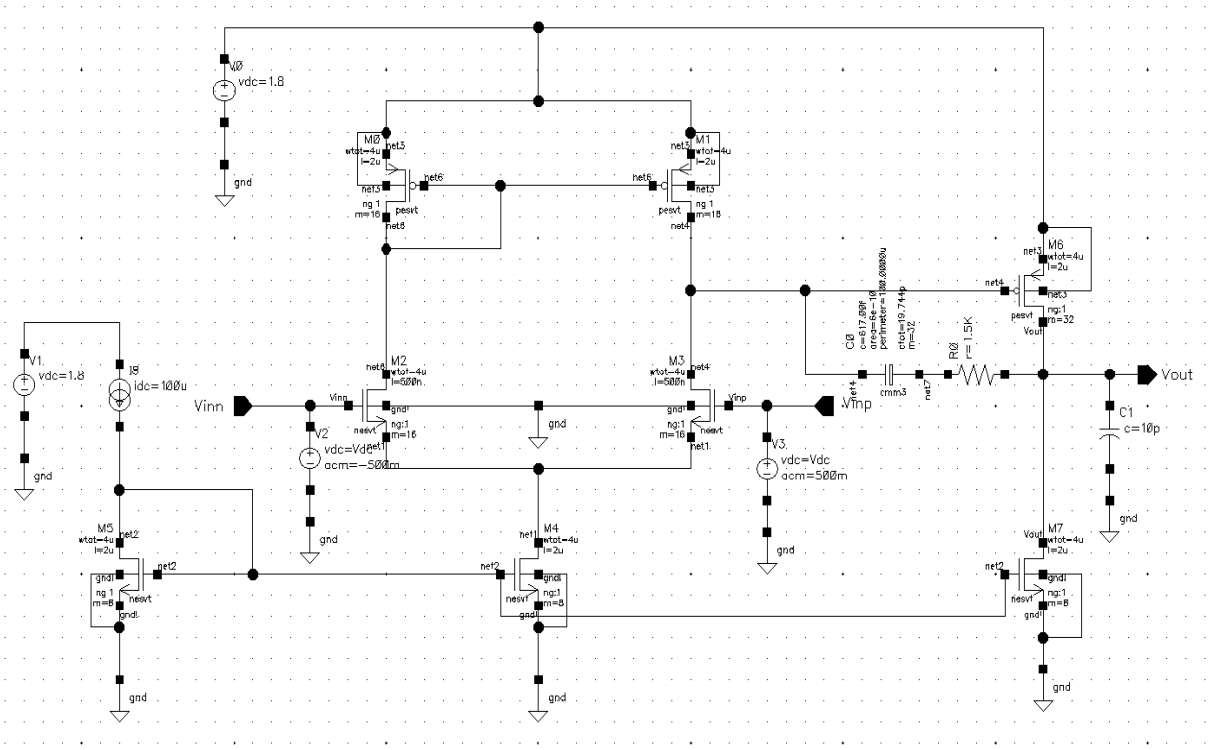
Since this zero occurs in the right-half-plane, it adds a positive phase contribution (leading to a phase lag) and can degrade the stability of the amplifier. To mitigate the effects of the RHP zero, a nulling resistor (Rz) is often added in series with Cc. This resistor shifts the zero to the left-half-plane (LHP), where it contributes positively to the phase margin. The new zero becomes:

$$z \approx -1/R_z Cc_z$$

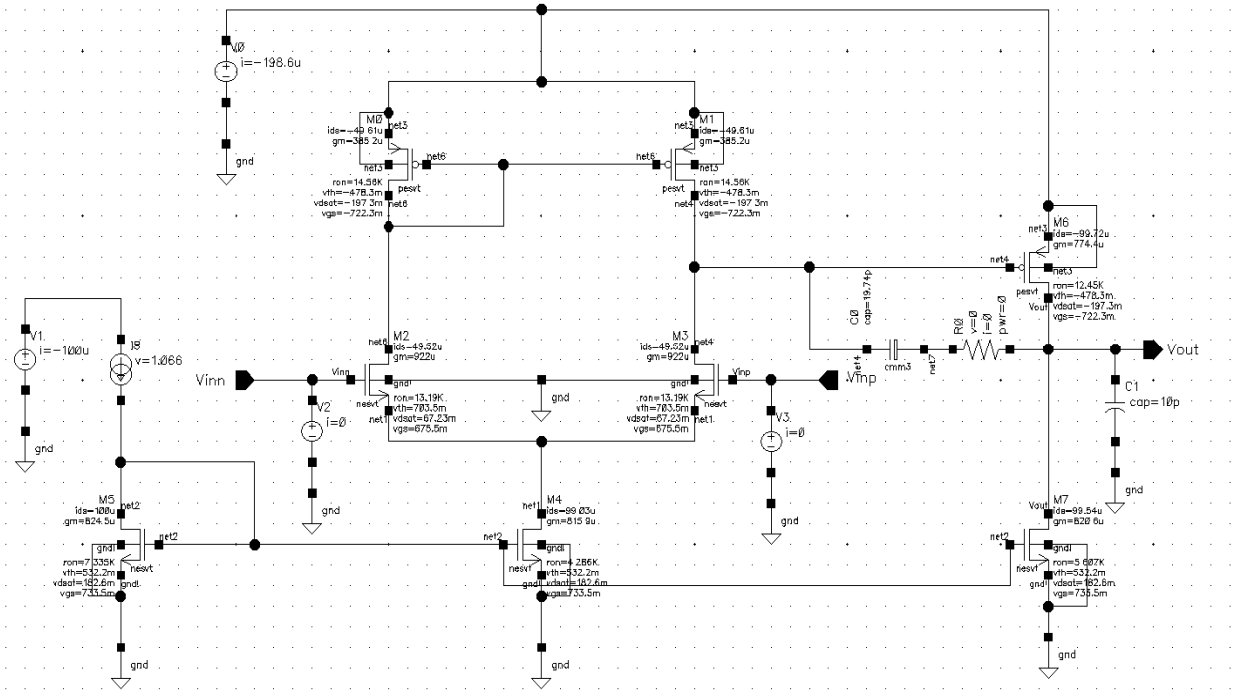
Design Considerations for Poles and Stability

1. **Pole Splitting:**
   Miller compensation separates p1 and p2 such that $|p1| \ll |p2|$. This ensures that the dominant pole is far below the unity-gain bandwidth (UGB) and the non-dominant pole is far above it, improving stability.
2. **Phase Margin:**
   The phase margin is directly affected by the locations of p1, p2, and z. Typically, a phase margin of 45−60 is targeted for optimal stability and transient response.

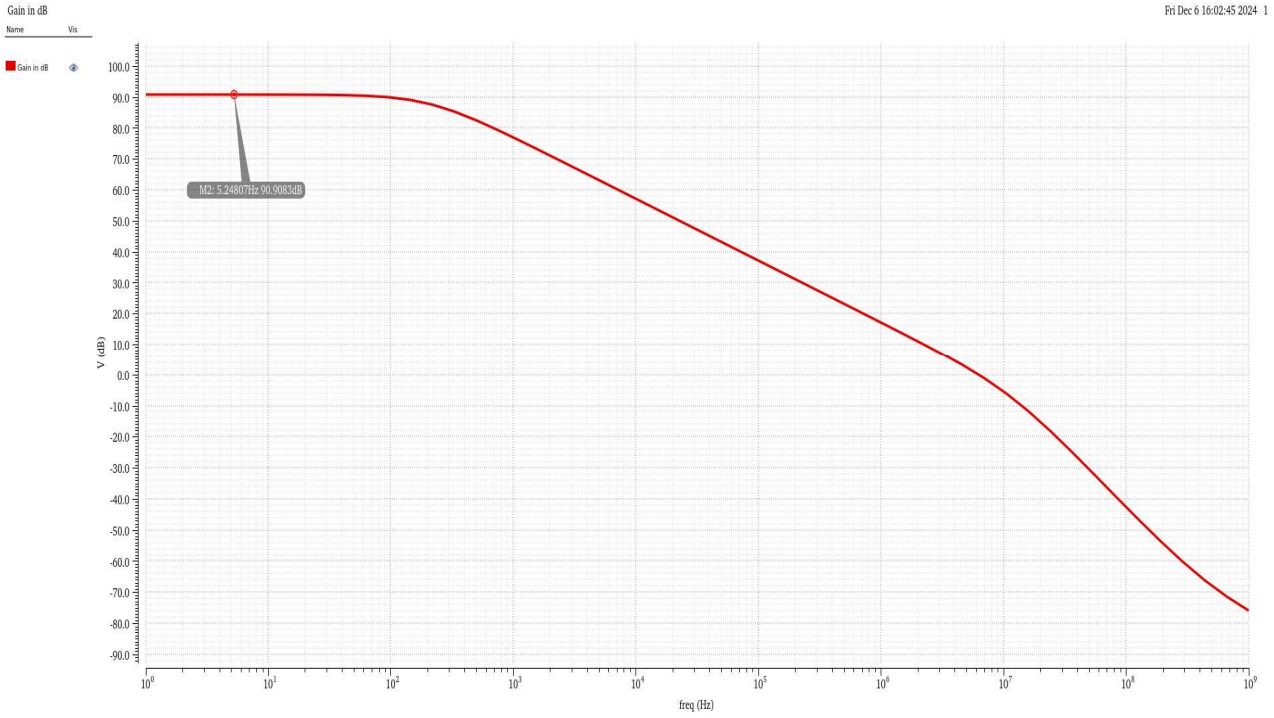
Schematic:



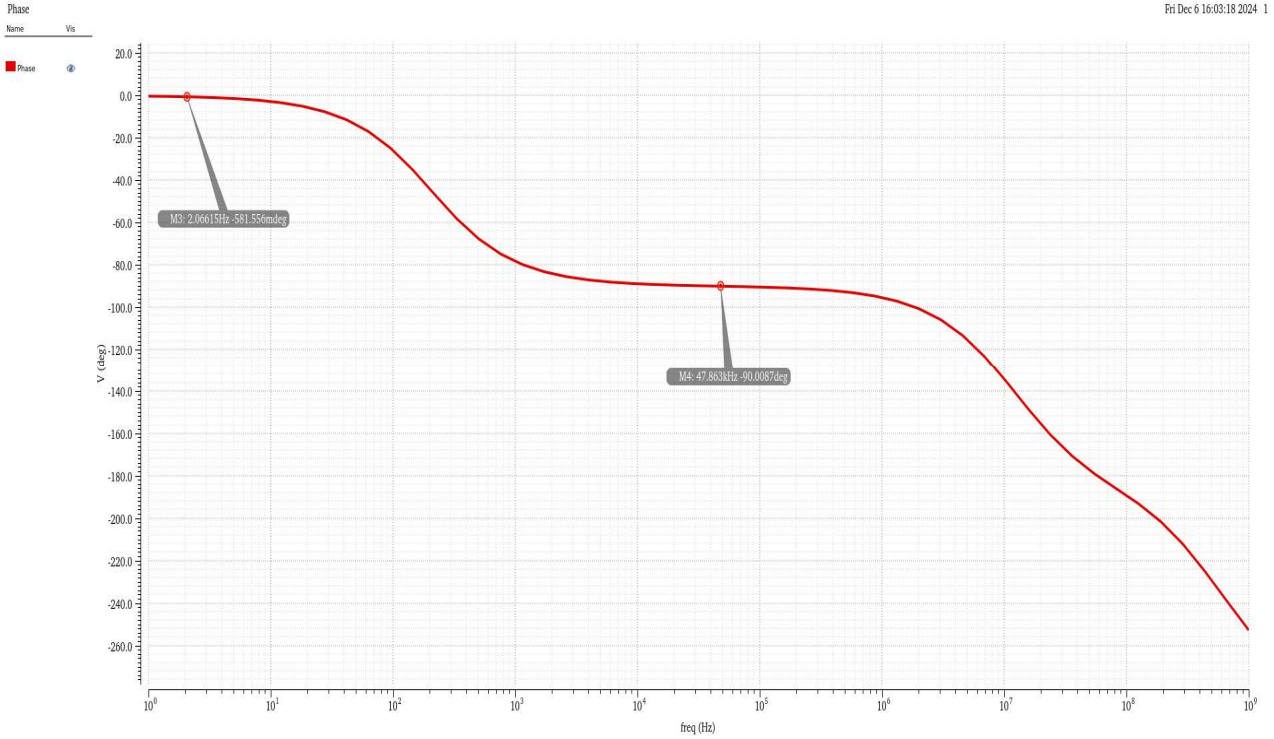
Schematic (DC Op point):



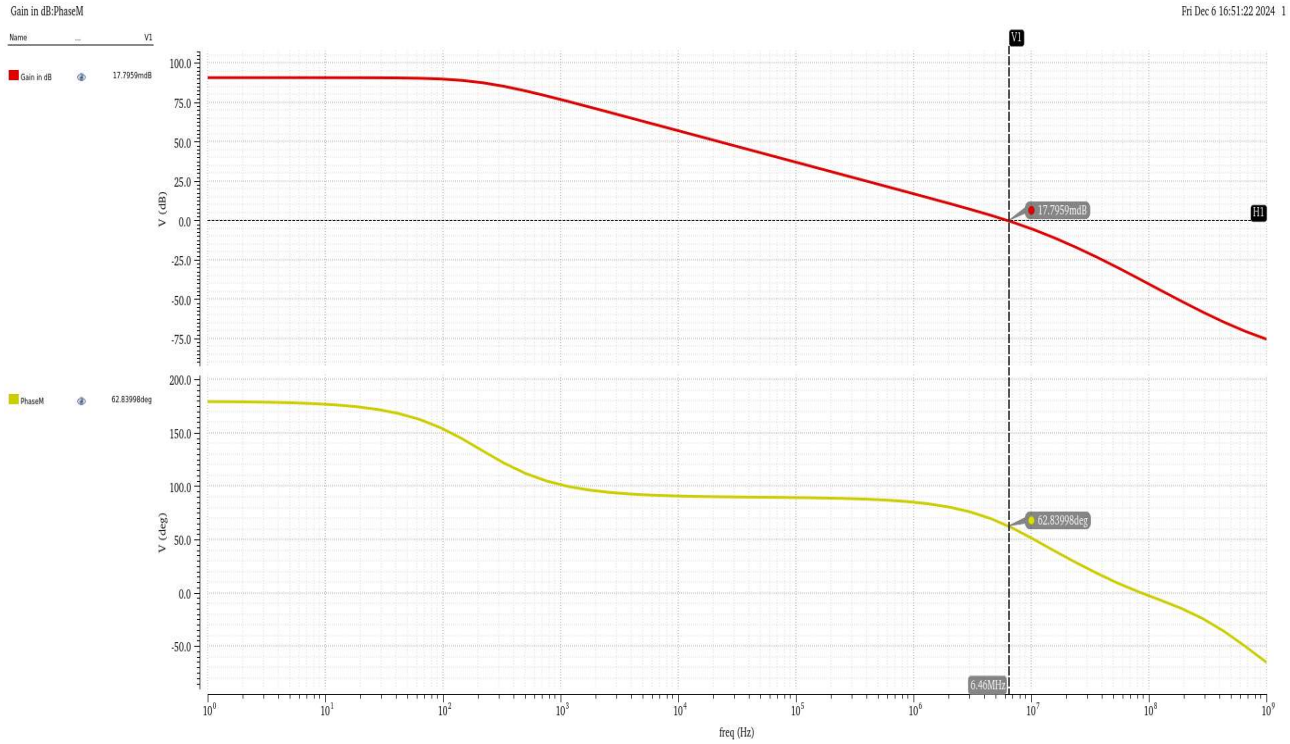
Voltage Gain (in dB):



Phase plot:



Stability-Phase Margin:



Required v/s Achieved Specs from the OTA:

	Required	Achieved
Supply Voltage	1.8V ± 10%	1.8V
Power Consumption	≤ 0.4 mW	0.3564 mW
Voltage Gain	90 dB	91 dB
Unity Gain Bandwidth	≥ 5 MHz	6.46 MHz
Slew Rate	20 V/µsec	19.94 V/ µsec
Phase Margin	≥ 60º	62.83º
ICMR low	1V	900 mV