SUB 1V BG Design

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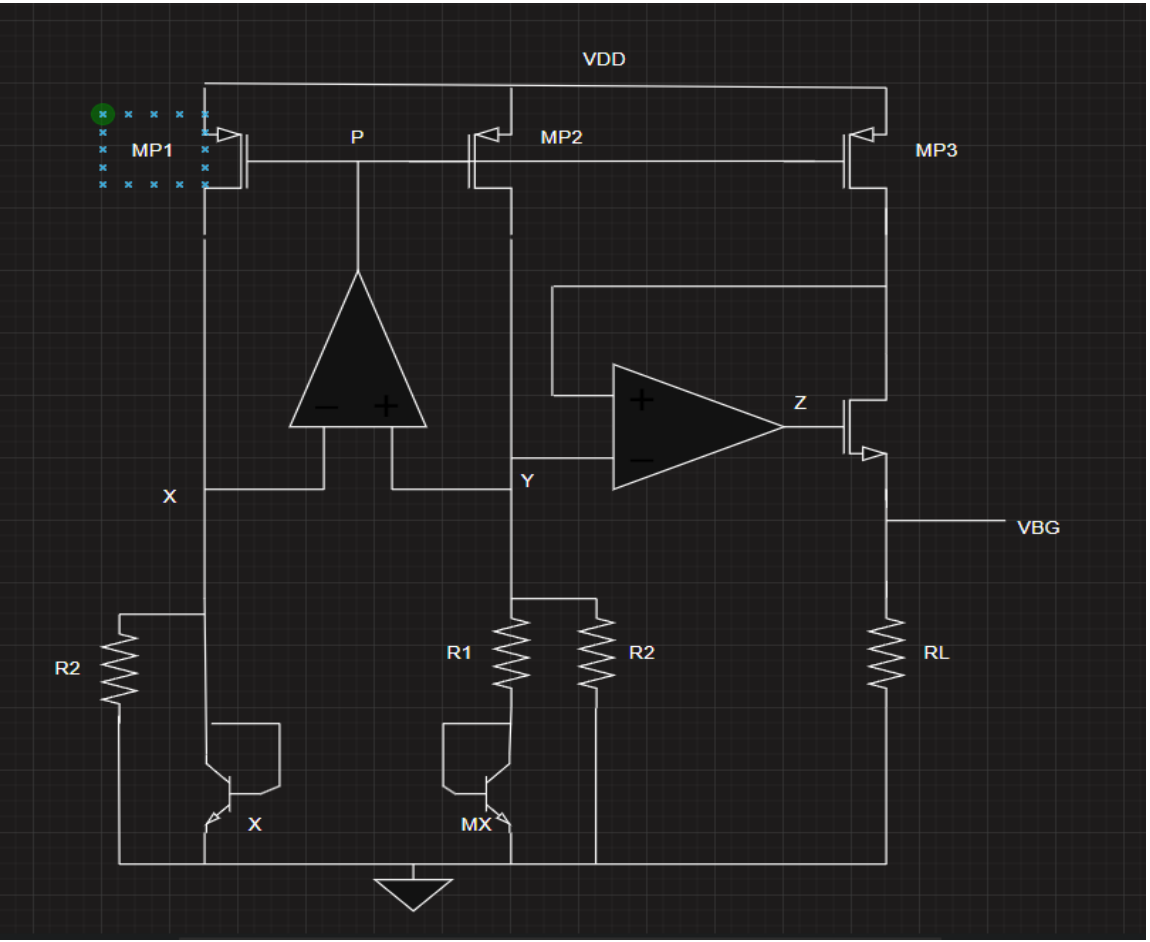
Reference Used : B. Razavi, "The Design of a Low-Voltage Bandgap Reference [The Analog Mind]," in *IEEE Solid-State Circuits Magazine*, vol. 13, no. 3, pp. 6-16, Summer 2021, doi: 10.1109/MSSC.2021.3088963. keywords: {Integrated circuits;Low voltage;Photonic band gap;Perturbation methods;Switches;Voltage control;Transient analysis;Operational amplifiers;Resistors;Low-pass filters},

Contents :

Target Specs

Output Voltage : 0.3 Volts
Output Voltage Variation < 1 % (0 ℃ to 100 ℃)
Supply Rejection > 40 dB
Power Consumption < 1 mW
Supply Voltage : 1.2 Volts ± 5 % (1.14 to 1.26 Volts)

Topology Used



Note :
Startup circuit is included later in the schematics section

Both Error Amps have the same input common mode range so they were re-used. (More details in the EA section)

Basic Operation

→ OPAMP Ensures Vx = Vy
⇒ Vbe1 = Vbe2 + I_R1*R1
⇒ I_R1 = Vt*ln(M)/R1

Now I_MP2 = I_MP1 (their W/L is same)
So I_MP = Vt*ln(M)/R1 + Vbe1/R2

Vbg = RL*(I_MP)

Vbg = RL/R1 *(Vt*ln(M) + (R1/R2)*Vbe1)

Now resistors are sized such that tempco is zero (just at 27 degree centigrade)

- We can't cancel the tempco at all the temperatures since the slope also changes with temperature but cancelling the tempco just at 27 would give good accuracy.

Vbg = RL/R1 * (PTAT + NTAT)

Slope (Vt*ln(M)) = (-1)*Slope(R1/R2 * Vbe1)
0.087*ln(M) = 1.702*(R1/R2)
→ Cancellation is done only at 27 ℃
→ Slope of Vbe is confirmed from the simulation (slide 6)

M=8
R1/R2 = 0.106

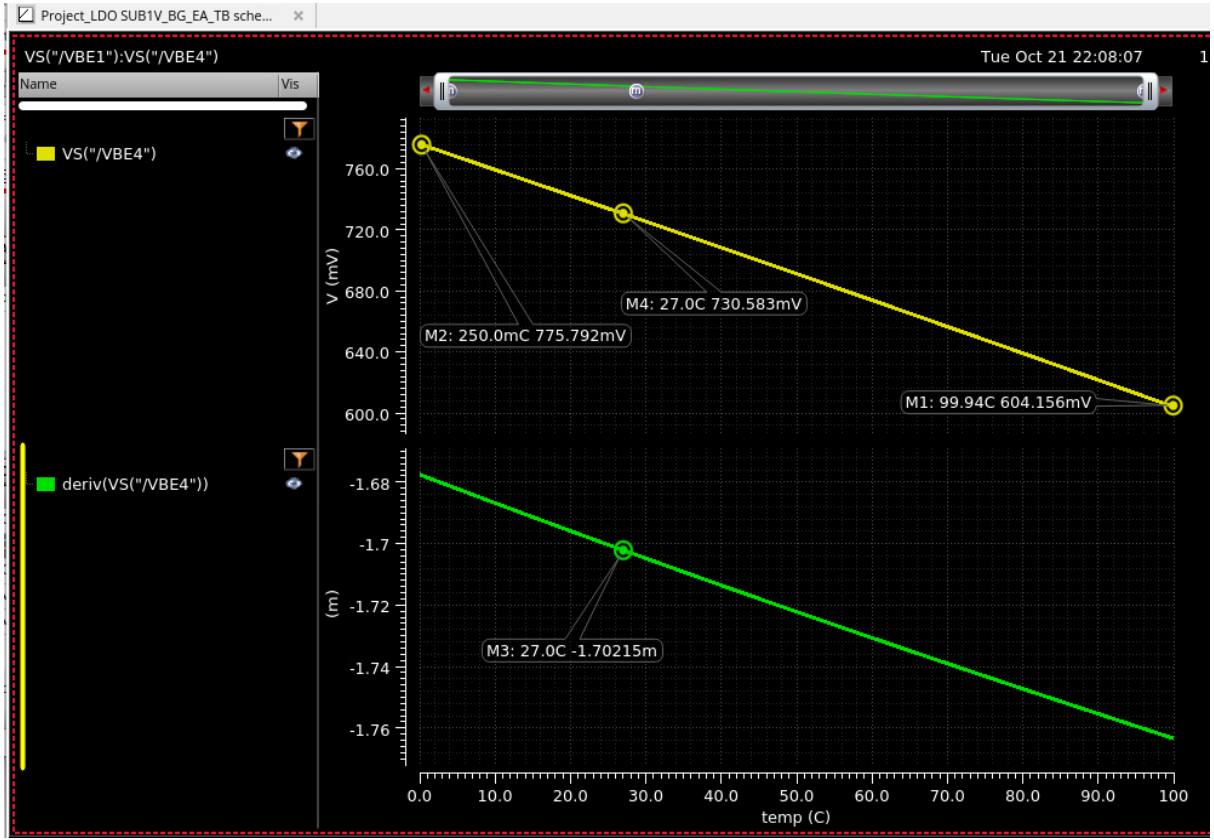
R1=1.5 KΩ
R2 = 14.15 KΩ

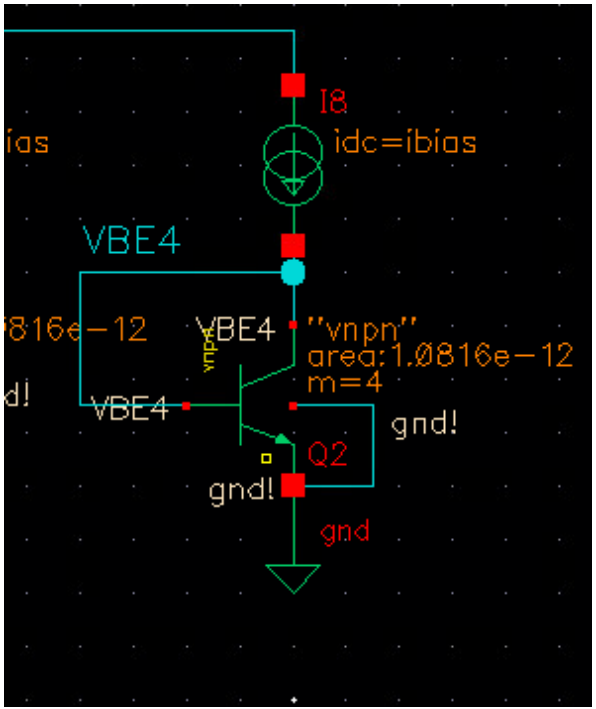
Now for Vbg = 0.3 Volts
RL = 3.416 KΩ

First Cut R numbers are :

R1 : 1.5 KΩ
R2 : 14.15 KΩ
R3 : 3.416 KΩ

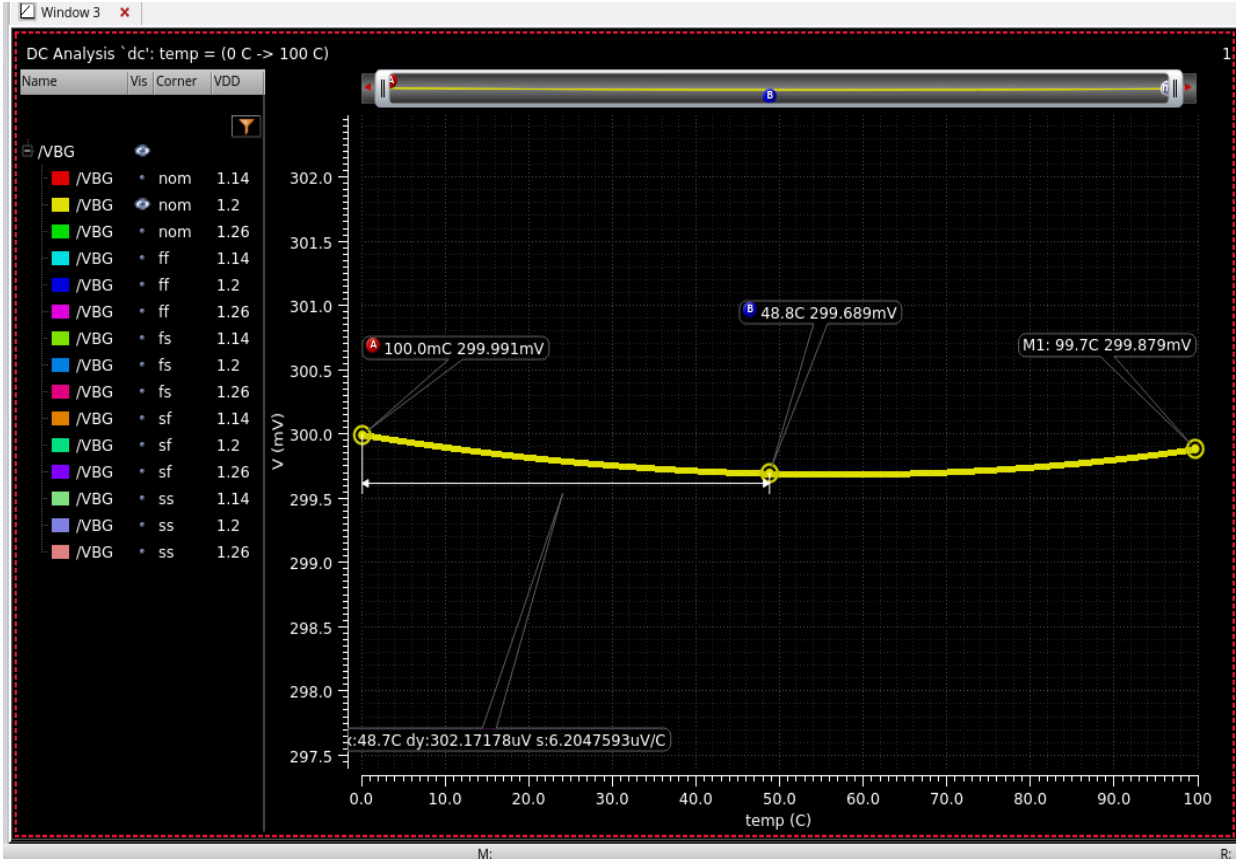
Ibias : 35uA (Vtln(8)/1.5K) assumed R1 : 1.5K



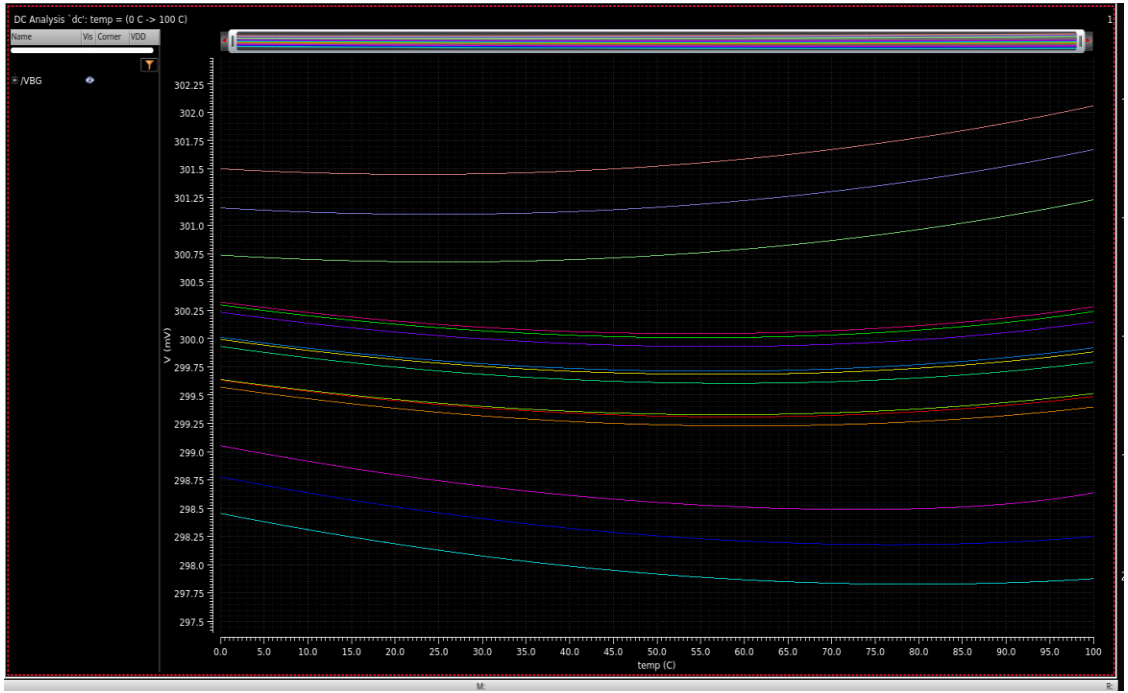


DC Sim (Nominal)

Note : The Handcalculation didn’t give the umbrella curve so using simulation the resistor values were tweaked in order to achieve that



DC Sims Across PVT (5 Process corners, 3 Supply Corners, 3 Temperature points 0,27,100)



We can see that across the process Vbe values changes which changes the effective Vbg value as well, this requires resistor trimming techniques which ensures the slope cancellation and Vbg value maintained at 300mV.

Power Consumption

9/12 rows

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	ff	fs	sf	ss
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
Parameters: VDD=1.14												
1	DCSIM	I_27C	462.7u	< 800u		pass	436.7u	487.3u	487.3u	463.2u	461.9u	436.7u
1	DCSIM	I_100C	460.6u	< 800u		pass	436.7u	483.8u	483.8u	460.9u	459.9u	436.7u
1	DCSIM	I_0C	463.8u	< 800u		pass	437u	489u	489u	464.4u	462.9u	437u
Parameters: VDD=1.2												
2	DCSIM	I_27C	464.5u	< 800u		pass	438.6u	489u	489u	464.9u	463.8u	438.6u
2	DCSIM	I_100C	462.2u	< 800u		pass	438.4u	485.4u	485.4u	462.5u	461.5u	438.4u
2	DCSIM	I_0C	465.7u	< 800u		pass	438.9u	490.8u	490.8u	466.1u	464.9u	438.9u
Parameters: VDD=1.26												
3	DCSIM	I_27C	466u	< 800u		pass	440.2u	490.5u	490.5u	466.4u	465.4u	440.2u
3	DCSIM	I_100C	463.6u	< 800u		pass	439.9u	486.8u	486.8u	463.8u	463u	439.9u
3	DCSIM	I_0C	467.3u	< 800u		pass	440.6u	492.4u	492.4u	467.7u	466.6u	440.6u

Max Power @ 1.2 Volts = 1.2*490uA = 0.58mW
Current Distribution : Around 200uA in Error Amps, 3*(0.3/3.86K) in the three branches : 233uA
And some biasing branches

Why Choose M=8 ?

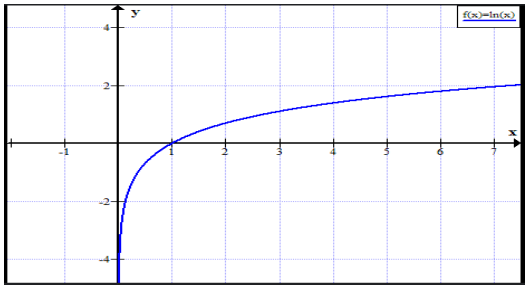
If we have a Vos (input referred offset of the opamp) then Vbg expression comes out to be :

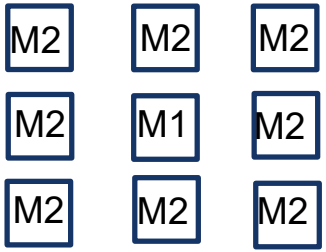
$Vbg = R_L/R_2(Vbe_1 + R_2/R_1 * Vt*\ln(M) – (1+R_2/R_1)*Vos)$

Now to reduce the effect of the offset R_2/R_1 needs to be minimized, to still get the flat Vbg we need to increase value of M so that temperature slopes are cancelled.

But we can't increase the value of M forever as it consumes significant area.

M=2 , ln(2) = 0.693
M=4 , ln(4) = 1.386
M=8, ln(8) = 2.079
M=16 , ln(16) = 2.77

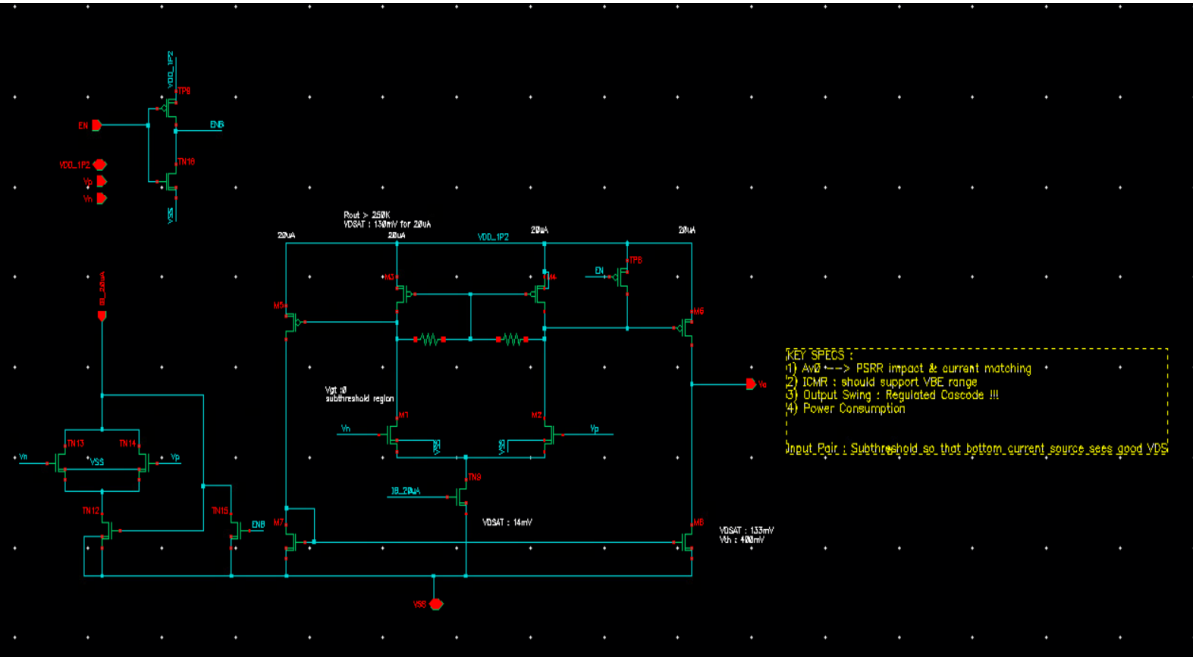




The percentage increase in the values as M increases seems to decrease, so choosing 8 seems to be good Tradeoff.

Error Amp Design

Since the input of the error amp is at voltage level of Vbe1 (Vx) that why the ICMR should be decided by that which is 601mV to 775mV (slide 6) → NMOS input pair based ERROR AMP was chosen.
Current mirror type opamp but with some additional resistors in the first stage which gives boost to DC gain.



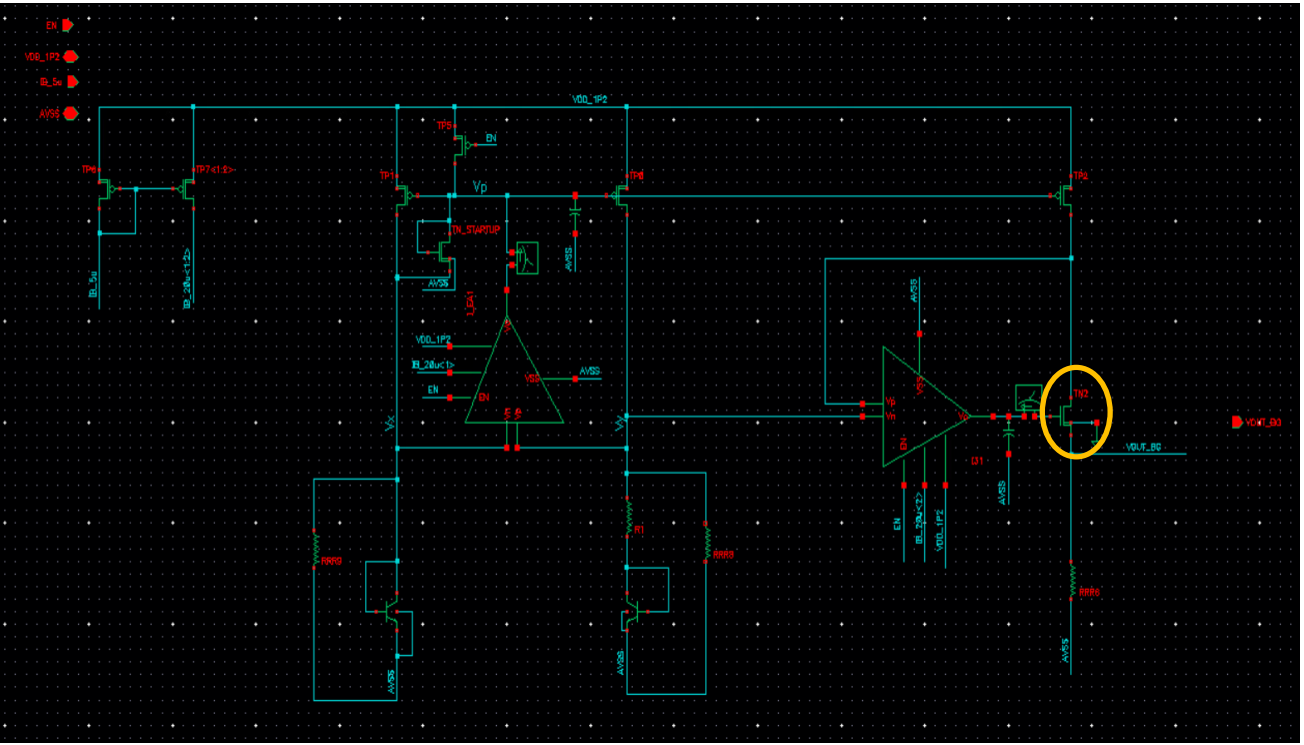
→Gain : Impacts overall accuracy, PSRR

→Should support a ICMR of VBE range across temperature (0.6 to 0.75mV)

→ Its output swing should also include Vbg+Vgs (output stage of the bandgap circuit has a regulated cascode structure)

→ There are two high impedance nodes in this opamp so there was **external cap** used to stabilize the neg-fb loops in which this opamp was used.

Error Amp Design



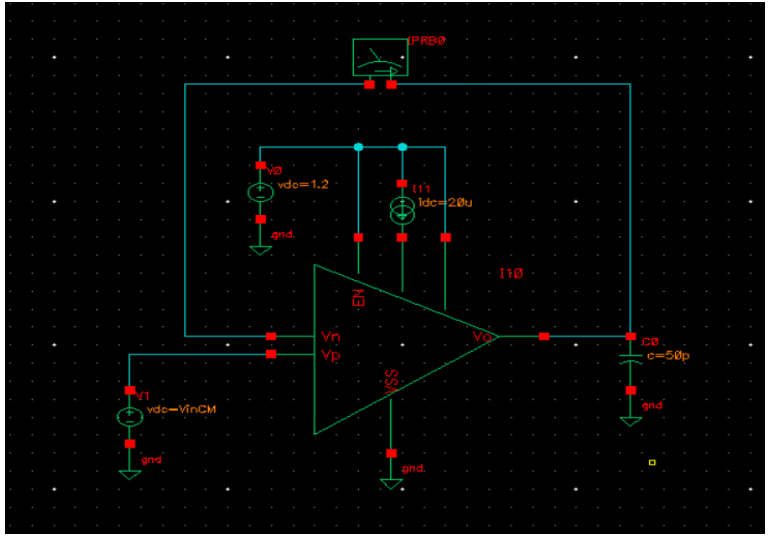
→ Its output swing should also include Vbg+Vgs (output stage of the bandgap circuit has a regulated cascode structure

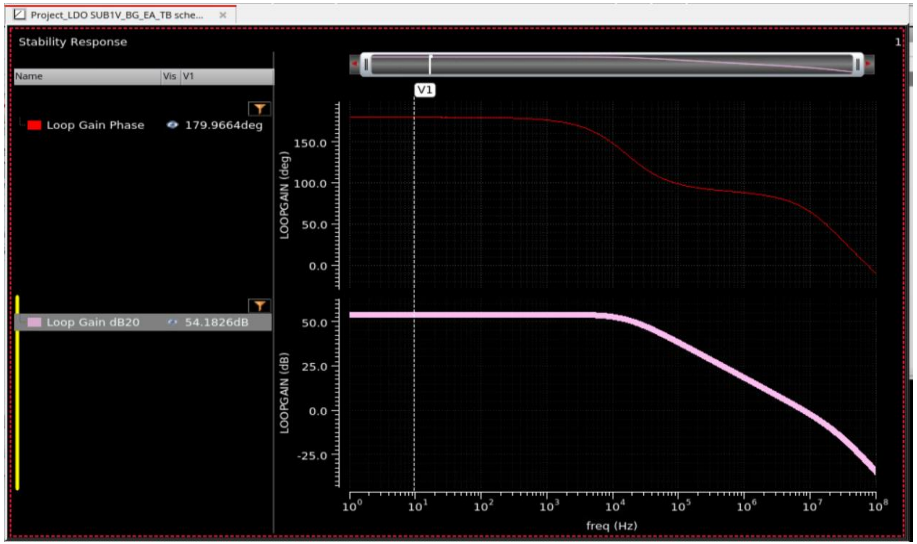
→ At the gate of the encircled transistor voltage will be **Vbg+ Vgs** (and Vgs will be slightly higher than usual due to body effect experienced by TN2)

→ So EA was designed such that output swing includes this point across temperature

Stand-Alone EA Sim Results

EA Current Consumption : 100uA



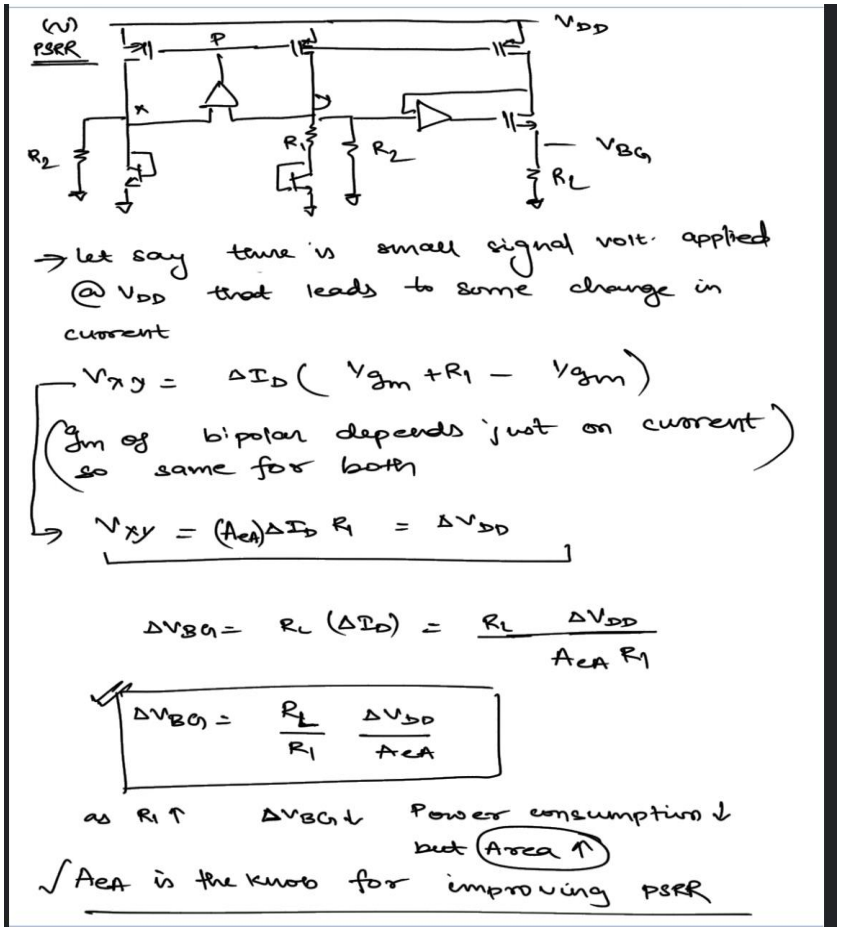


54dB DC gain
50pF output was just kept to ensure output node dominant pole

The –ve fb loop involving error amps uses lesser cap (more details in upcoming slides)

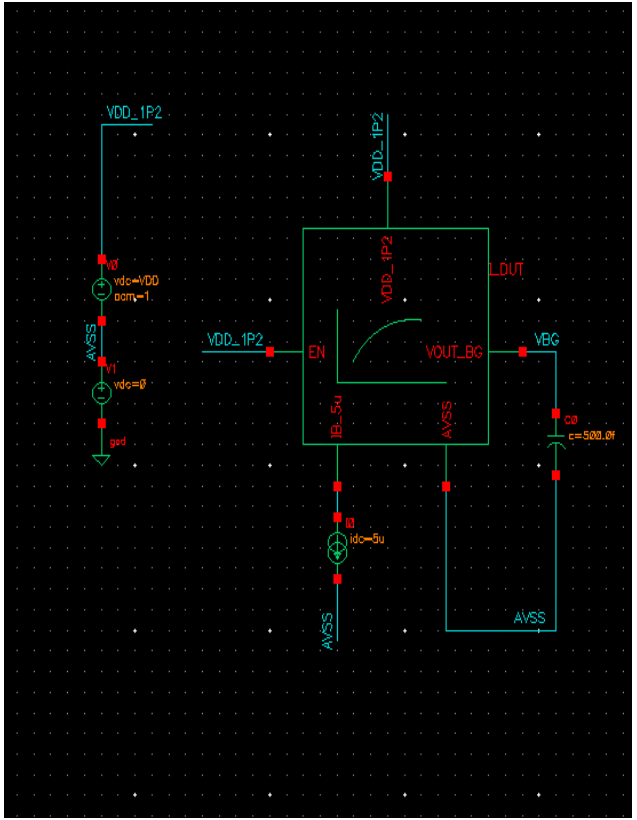
Output node impedance : 192Kohms
First Node Impedance : 30Kohms

PSRR Calculations

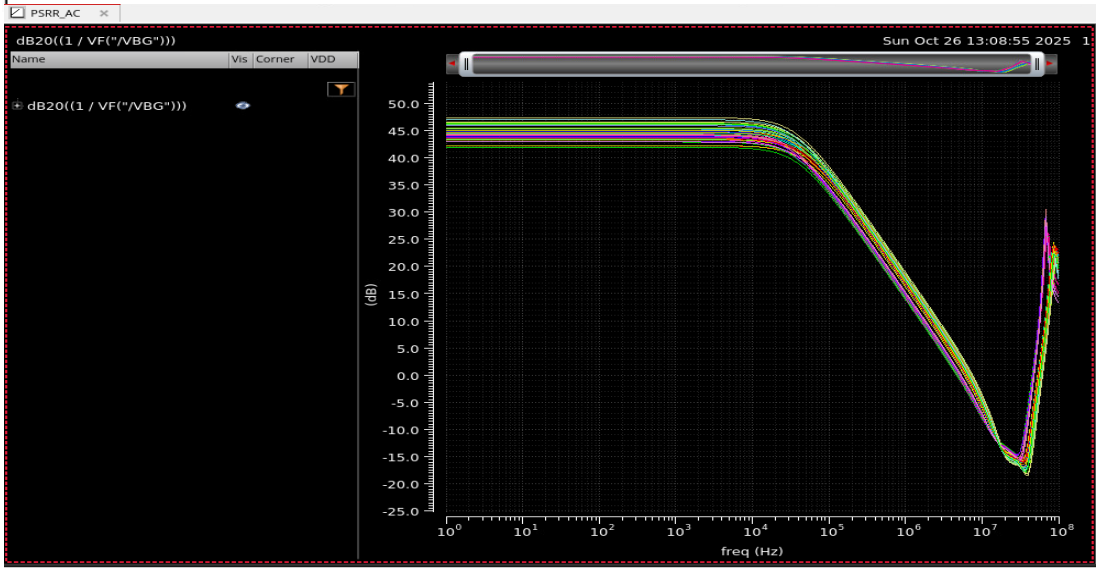


Here its assumed that OPAMP is able to reject all the supply noise, which is indeed the case. PSR of the opamp is high due to the 2 stage structure.

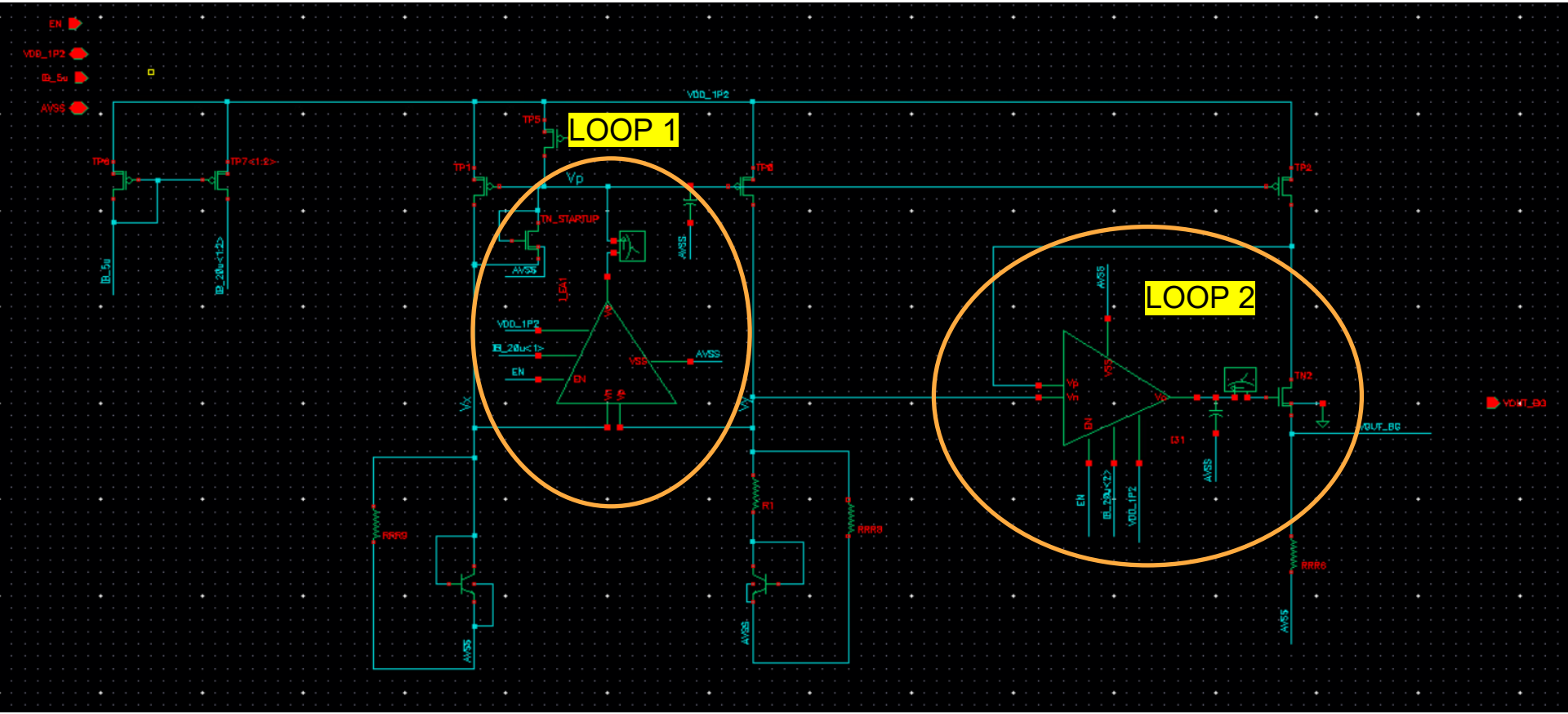
PSRR Sim Results & TB



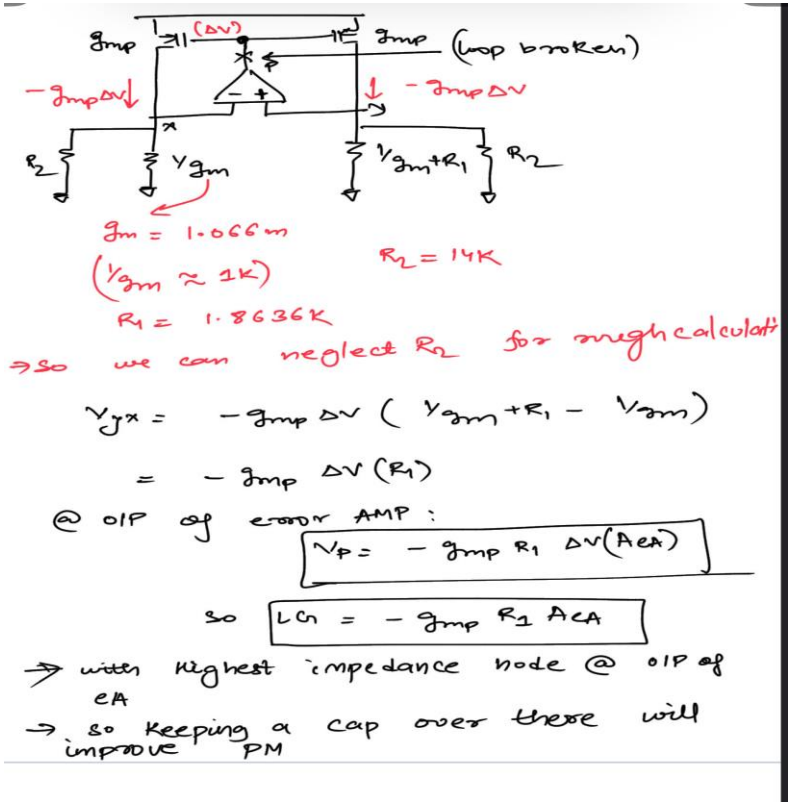
Point	Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
Parameters: VDD=1.2								
1	PSRR_AC	PSR_DC	45.02	> 40		pass	43.26	46.13
Parameters: VDD=1.14								
2	PSRR_AC	PSR_DC	43.53	> 40		pass	41.89	44.62
Parameters: VDD=1.26								
3	PSRR_AC	PSR_DC	46.23	> 40		pass	42.88	47.34



-ve FB loops Stability



Loop1



Gmp.R1 around 1.44 at nominal conditions
LG nearly same as Error AMP gain

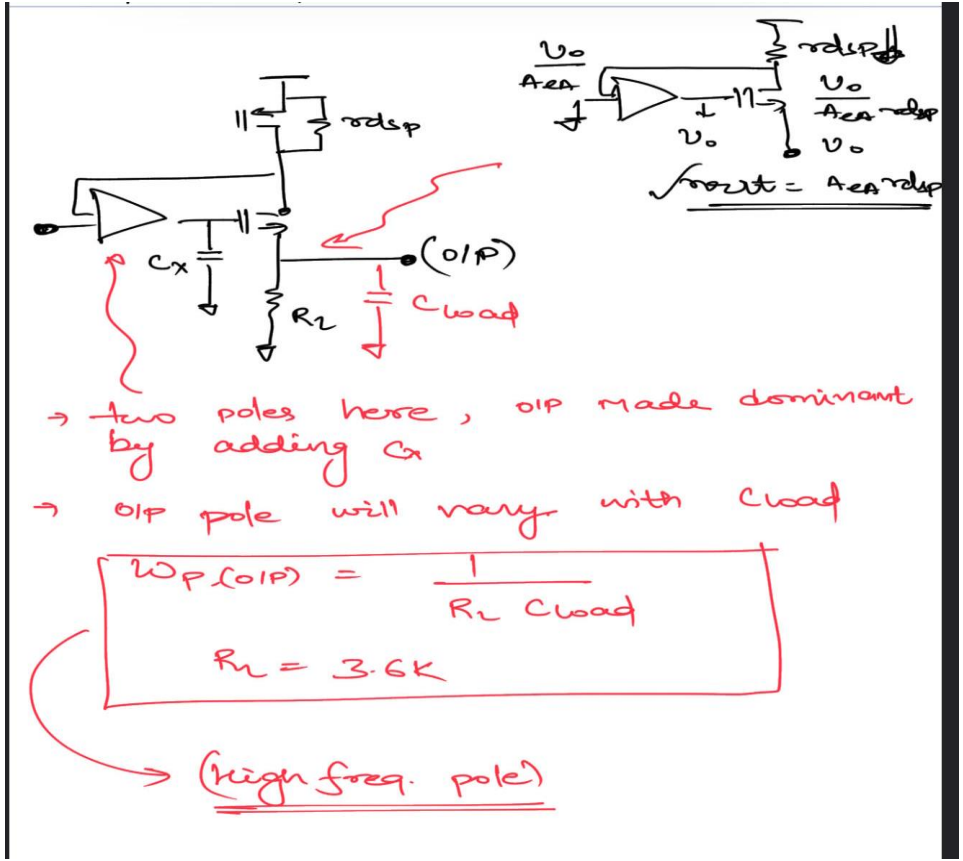
PVT Results across the supply(1.2 + 5% variation)

Parameter	Nominal	ff_0	ff_1	ff_2	fs_0
allModels.scs	tt	ff <unspecified section>	ff <unspecified section>	ff <unspecified section>	fs <unspecified section>
design.scs					
temperature	27	0	27	100	0

12 rows

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	ff_0	ff_1	ff_2	fs_0
Parameters: VDD=1.14												
1	STB_SIM	Loop Gain Phase										
1	STB_SIM	Loop Gain dB20										
1	STB_SIM	Phase Margin	50.91				46.87	59.87	46.87	49.57	57.05	49.3
1	STB_SIM	Av0	52.5				49.88	53.72	53.72	53.04	50.94	52.59
Parameters: VDD=1.2												
2	STB_SIM	Loop Gain Phase										
2	STB_SIM	Loop Gain dB20										
2	STB_SIM	Phase Margin	49.35				45.1	58.84	45.1	48.08	56.08	47.23
2	STB_SIM	Av0	53.45				50.71	54.68	54.68	53.91	51.29	53.74
Parameters: VDD=1.26												
3	STB_SIM	Loop Gain Phase										
3	STB_SIM	Loop Gain dB20										
3	STB_SIM	Phase Margin	48.09				43.69	57.97	43.69	46.87	55.26	45.63
3	STB_SIM	Av0	54.24				50.49	55.49	55.49	54.65	50.49	54.68

Loop 2



Loop gain is higher than Loop here due to which bandwidth will be slightly higher if we keep the same 20pF at the output of the error amp and which leads lower phase margin as compared to the previous loop.

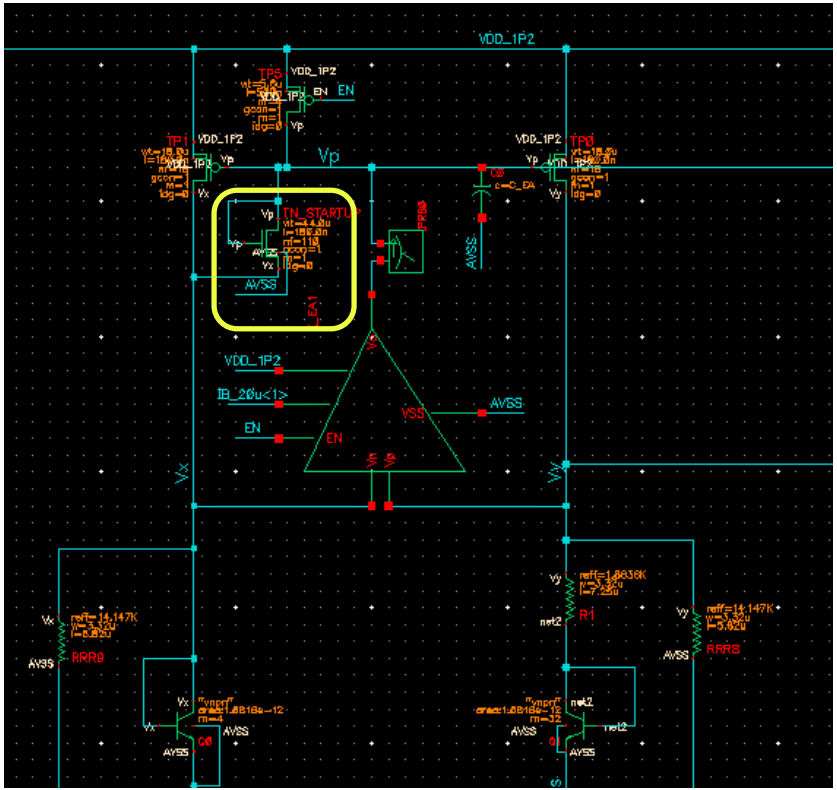
maestro | I_DUT (SUB1V_BG)

Outputs Setup | Results

Summary | Replace | (None)

Test	Output	Min	Max	Mean	Median	Std Dev	Spec	Pass/Fail
STB_SIM	Phase Margin	20.08	29.3	24.85	24.75	2.564		
STB_SIM	Av0	57.66	64.73	61.88	62.32	2.092		

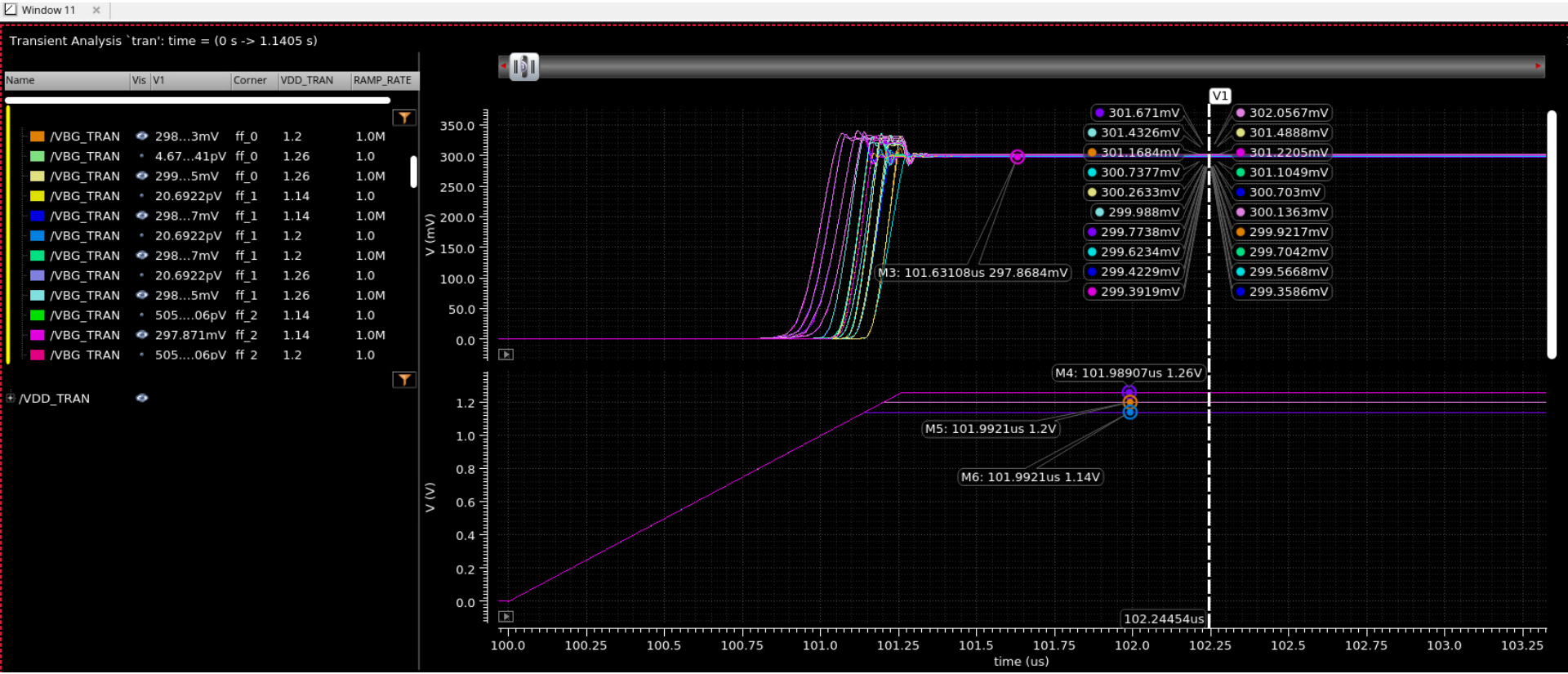
Startup Circuitry



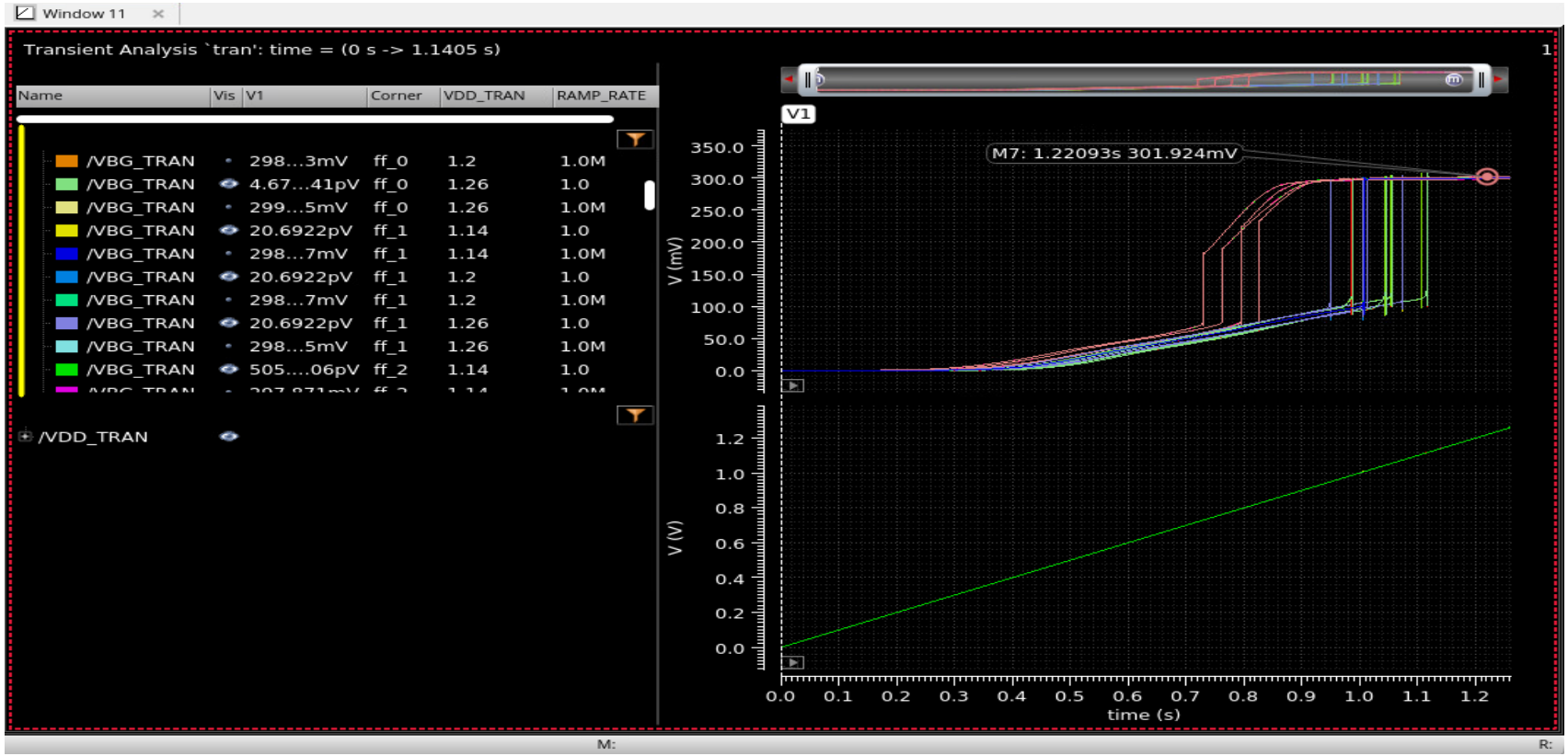
Operation :
So if the startup device was not there than Vx& Vy can just stay at zero with Vp : VDD

Now due to inclusion of this device, it will perturb the node Vx,Vy during the startup and during the steady state it won't be drawing any current so won't be disturbing the normal operation.

StartUP Sims (1M Ramp Rate at the Supply)



1V Ramp Rate at the Supply



SCM

	SPEC	
DC Accuracy	< 1% across temperature	@nominal 302uV Slide 7
PSRR DC	>40dB	Min PSRR achieved : 41.89 dB (across PVT) Slide 15
Power Consumption	<1mW	0.58mW Slide 9