# ECEN 704 VLSI Circuit Design Project

Harshit Gupta, UIN: 735006036

Abstract — A 2-stage Fully Differential Miller compensated OPAMP was designed with the first stage being telescopic in nature for providing more gain and second stage being simple common source stage for providing the adequate output swing. A nulling resistor implemented using MOS transistor in triode region was used to improve the phase margin by making the RHP zero go to LHP and being placed closer to the non-dominant pole. Two CMFB circuits were implemented for setting the 1st stage and 2nd stage output common mode level. Reference for 1st stage common mode was generated internally. Only pads, transistors and capacitors were used in order to realize this.

## I. INTRODUCTION

This project required building a Fully Differential OPAMP with CMFB circuits. The key specs required are tabulated below.

| | | |
|---|---|---|
| **Technology** | IBM 180nm CMOS | |
| **Chip area (including pads)** | 1mm×1mm | |
| **Supply voltage** | 1.8V | |
| **Common-mode level ($V_{CM}$)** | 0.9V | |
| **Power dissipation** | ≤ 3mW | Open-loop |
| **DC gain** | ≥ 60 dB | Open-loop |
| **GBW** | ≥ 120 MHz | Open-loop |
| **Slew rate** | $\geq 75V/\mu s$ | Open-loop |
| **Input-referred noise (1Hz-100MHz)** | $\leq 50\mu V_{rms}$ | Open-loop |
| **IM3 ($1V_{pp}$@1MHz)** | ≤ −60 dB | Closed-loop |
| **Differential phase margin** | ≥ 60° | Closed-loop |
| **CMFB phase margin** | ≥ 60° | Closed-loop |

## II. DESGIN PROCEDURE

### A. Circuit Topology

Potential Topologies for realizing this OPAMP included Folded Cascode Fully Differential OPAMP, 2-Stage Miller Compensated OPAMP, Current Mirror OPAMP. Folded Cascode Fully Differential OPAMP would have slightly better output swing but meeting the gain SPEC was a challenge in this topology, requiring the devices to have larger length which would increase the parasitics capacitances at the internal nodes causing potential instability. Adding a second stage to the OPAMP also requires a miller cap which gives rise to RHP zero which needs to be taken care of by an appropriate compensation scheme. Since output gain is nearly around 10 so swing requirements reduces greatly at the first stage which allows the use of Telescopic 1st Stage.

Another advantage of using Telescopic 1st Stage and 2nd Common Source is that their node impedances are already way far from each other which requires the use of a very small miller cap as compared to not employing cascodes in the first stage.

Main Blocks Planned: Biasing Circuitry, OPAMP CORE (Telescopic + Common Source) + CMFB Circuitry (2 CMFB circuits, one for each stage).

### B. Design Calculations

Tradeoffs: If design is done towards obtaining higher gain by keeping larger input pair hence larger gm_1st this will require to have larger gm for the second stage as well which will increase parasitic caps on the output node (if gm is increased by increasing the device sizes and keeping the power dissipation fixed) hence increase the effective Cload which will require to have larger miller cap hence trading gain with area, power dissipation, stability.

Calculations:

Cload : 2.5pf, Cc was chosen as 0.1*Cload( around 0.274pF) initially (save area) and further steps were done based on that.

Itail (1st stage): 50uA chosen in order to satisfy the slew requirement.

I_2nd Stage: 36*12.5uA, this is chosen so high that 2nd stage W/L's can be relaxed since pmos upCox is 4 times lesser than the unCox.

Adc = A_firstStage * A_ 2ndStage = (gmn*(gmn_cas*rdsn*rdsn ‖ gmp_cas*rdsp*rdsp)) *(gmp*(rdsp‖rdsn))

It was observed that gain requirement was very easily fulfilled just with the first stage gain by using longer length devices which gives more rdsn and rdsp respectively.

Pole Locations: 1/(A_2ndStage*Cc*Z_1stStage), gmp_2ndStage/Cload and zero that is introduced through the resistor was placed close to non-dominant pole.

Zero Location: 1/ {Cc *(1/gmp_2ndStage - Rz)}, to place the zero close to non-dominant pole Rz was chosen as (1/gmp_2ndStage) *(Cload/Cc + 1)

Input pair gmn was chosen to meet the GBW requirement as GBW > 120 MHz which means gmn> 2*π*120MHz*Cc.

To meet the noise requirements, input pair gmn was tried to be maximized and the gmp (first stage pmos mirror) was tried to reduce by keeping them as small as possible (larger Veff). Second stage and cascodes of the first stage don't contribute much to noise.

gmn(input pair) = 615.3uS (W/L = 8*(4u/0.27u)), rdsn around 70KΩ => A_1stStage > 60dB

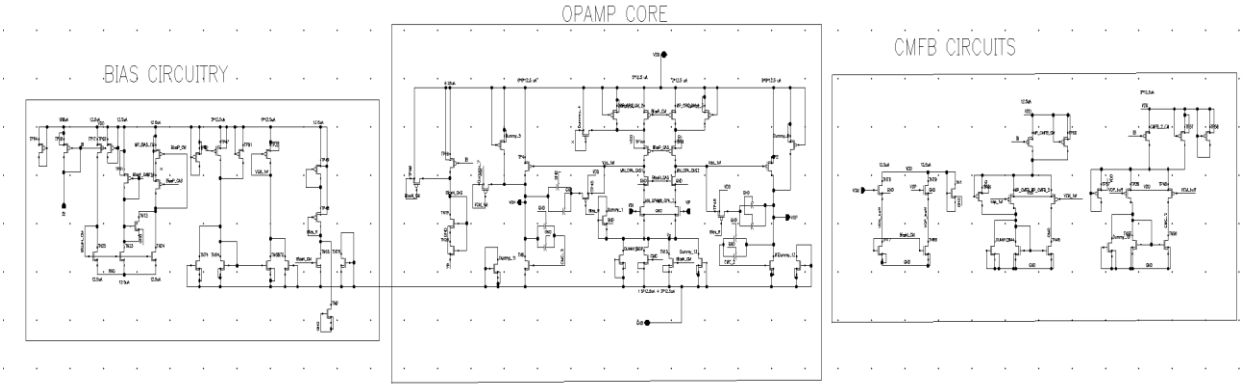
GBW is around gmn/Cc which is way higher than 120MHz so second pole was chosen lesser than GBW as compensation was being provided using Rz as well

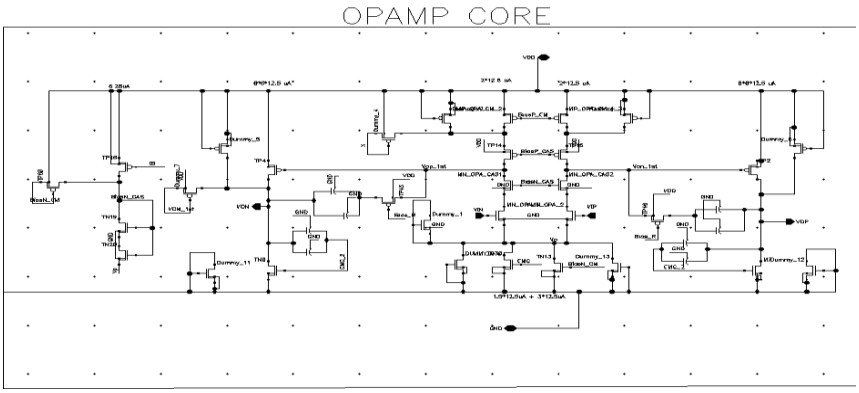
gmp_2ndStage (PMOS) = 2.2mS, non-dominant pole is around gmp/Cload which is around 140MHz (it was lesser than this frequency due to extra parasitics capacitances coming on the Vout node due to pad and output stage mosfets), resistor was placed such that the zero frequency is around this frequency.

Rz = 1/(gmp_2ndStage) * (Cload/Cc + 1) = 5KΩ (Rz was realized using pmos in linear region)
CMFB circuits are used to control the bottom current sources of both stages of OPAMP core for setting the common mode level. The outer CMFB loop consists of two high impedance nodes due to which 500fF was used as pole splitting cap over there.

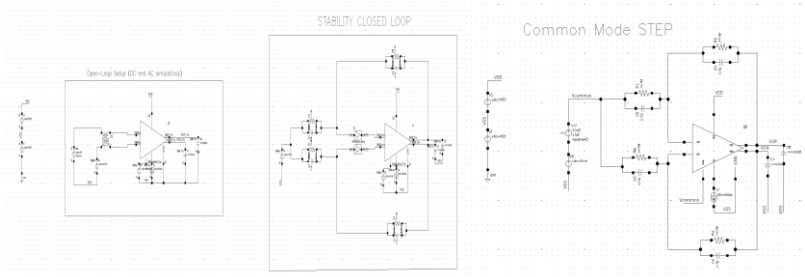
## III. Schematics And Simulation Results

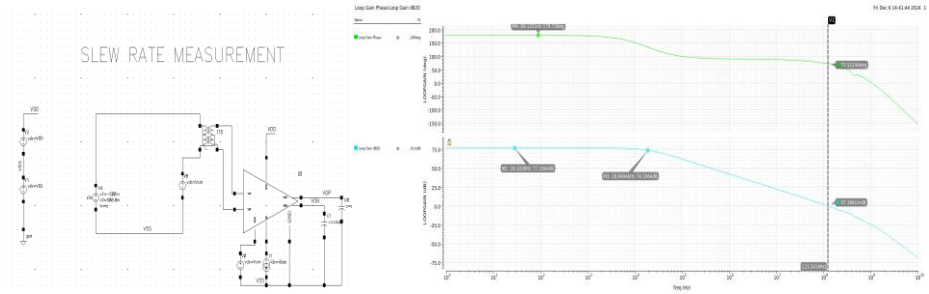
A. Design Schematics and Descriptions: Full Schematics View and Zoomed in OPAMP core

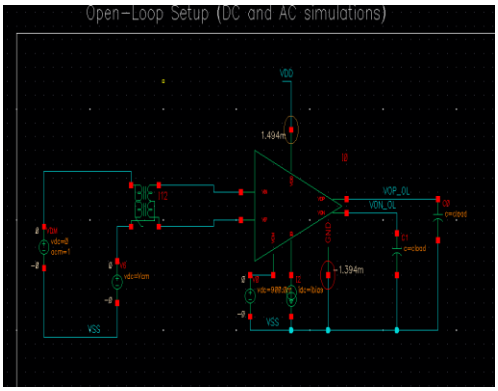



B. Simulation Results: Open loop (DC,AC,Noise,Power dissipation), closed loop(stability,PSS), transient simulations (CMFB stability).
Testbench Details: Purpose of the testbenches is marked in the images below





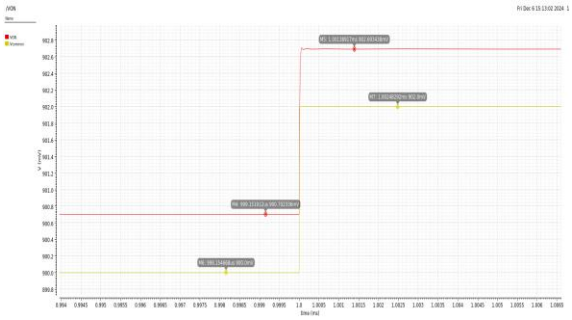



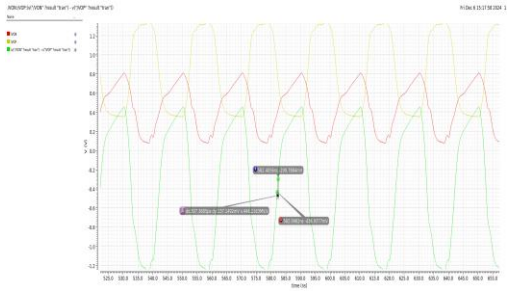

(72-degree Phase Margin, 77.106dB gain, 133MHz GBW)

Power Dissipation: 1.494m*1.8 = 2.68mW

| | | |
|---|---|---|
| 5 | DC Gain | 77.11 |
| 6 | pow(integ((getData("in" ?result "noise")**2) 1 100000000 " ") 0.5) | 81.67u |

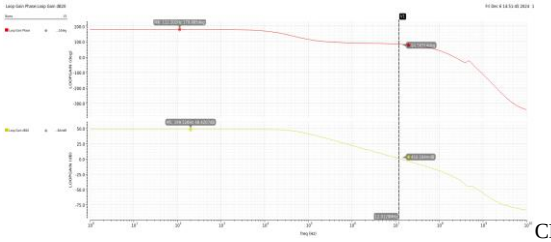
Noise 81.67 uVrms





CMFB Step response (83-degree Phase Margin ,2mV step)

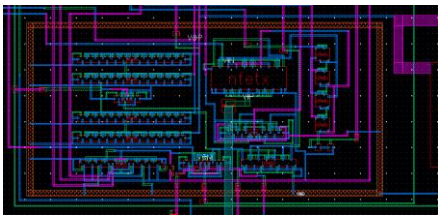
Slew Rate Plot (440MV/s) {d(Vp-Vn)/dt}



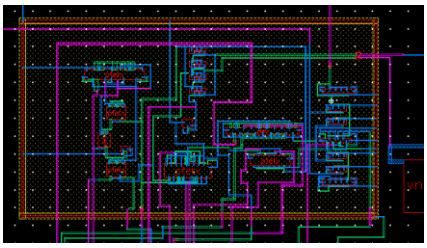
CMFB Loop Stability (48.4207dB Gain, 84 degrees Phase Margin)

## IV. CHIP LAYOUT


Chip Dimenshion : **0.4mm * 0.83 mm**

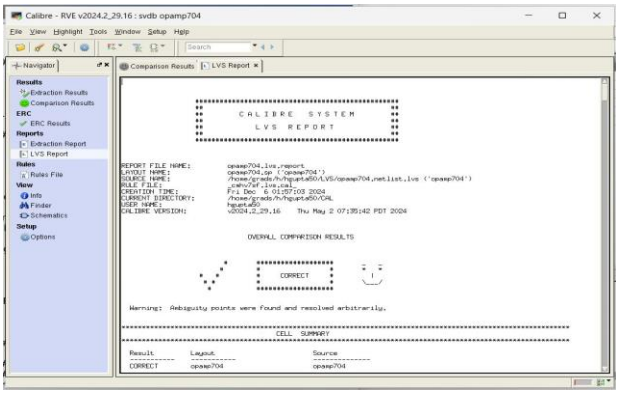


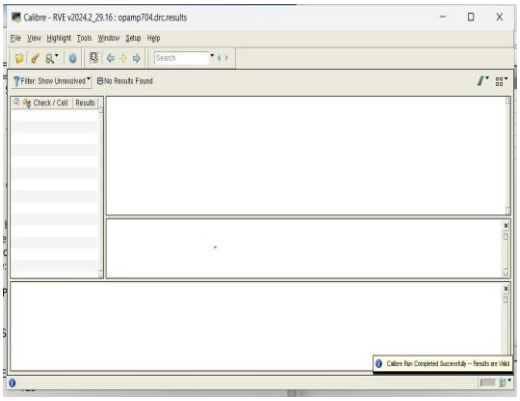
NMOS Section



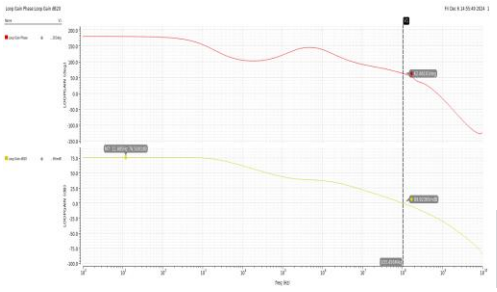
PMOS section Layout

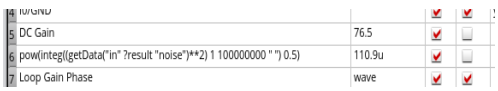
### C. DRC and LVS Reports



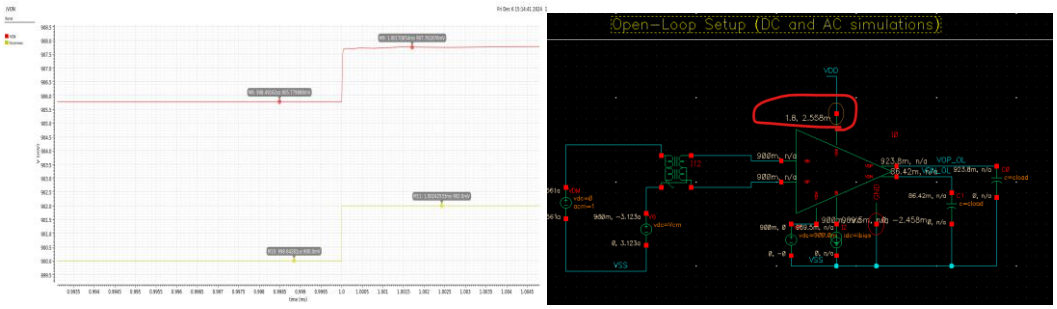




## D. Post Layout Results

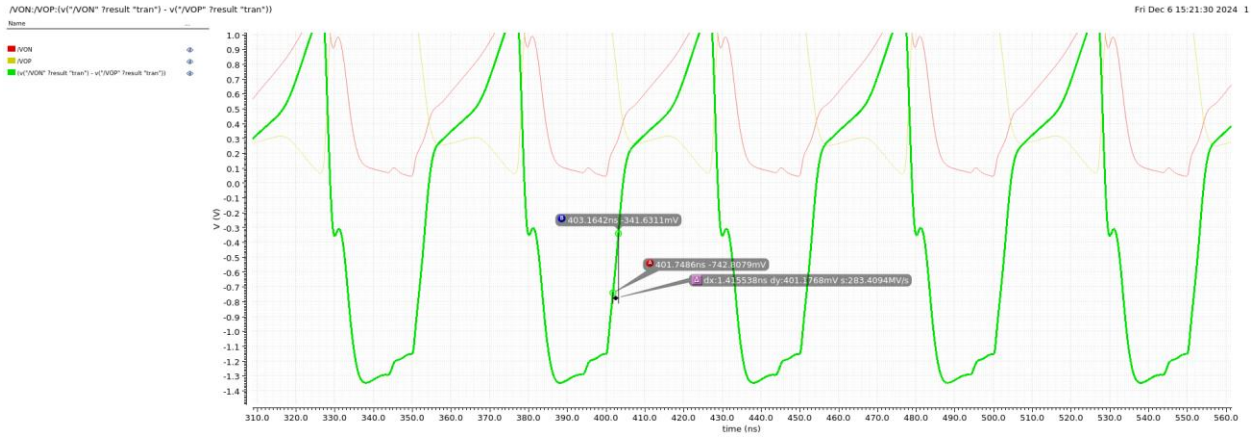





Gain: 76.5001dB, Phase Margin: 62.86 degrees




CMFB response nearly like schematics response (Phase Margin ~ 80 degrees but gain has surely reduced becoz of more error)




## v. CONCLUSION

| | Schematic Results | Post Layout Results |
|---|---|---|
| Area | | 0.4mm * 0.83mm |
| Gain | 77dB | 76 dB |
| Differential Phase Margin | 72 degrees | 62 degrees |
| CMFB Phase Margin | 83 degrees | < 83 degrees (>60 degrees) |
| GBW | 133 MHz | 103 MHz |
| Slew Rate | 440MV/s | 283MV/s |
| Input Referred Noise | 81.67 uVrms | 110.9 uVrms |
| Common Mode Level | 0.9 Volts | 0.905 Volts |
| Power Dissipation | 2.68 mW | 4.60 mW |

A few observations that can be made after viewing the post layout results include the reduction of phase margin frequency and phase margin as well, increase the input referred noise. It can be concluded that post layout capacitances seem to increase at all the nodes which decreases the dominant pole frequency and hence phase margin frequency, also the zero location which was set according to hand calculations is also not accurate which leads to reduction in the phase margin in the post layout simulations as exact pole-zero cancellation is hardly possible.