LDO DESIGN (CHAVA ZERO)

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Reference Used :

C. K. Chava and J. Silva-Martinez, "A frequency compensation scheme for LDO voltage regulators," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 6, pp. 1041-1050, June 2004, doi: 10.1109/TCSI.2004.829239. keywords: {Frequency;Regulators;Paramagnetic resonance;Capacitors;CMOS technology;Low voltage;Topology;Stability;Noise robustness;Nonhomogeneous media},

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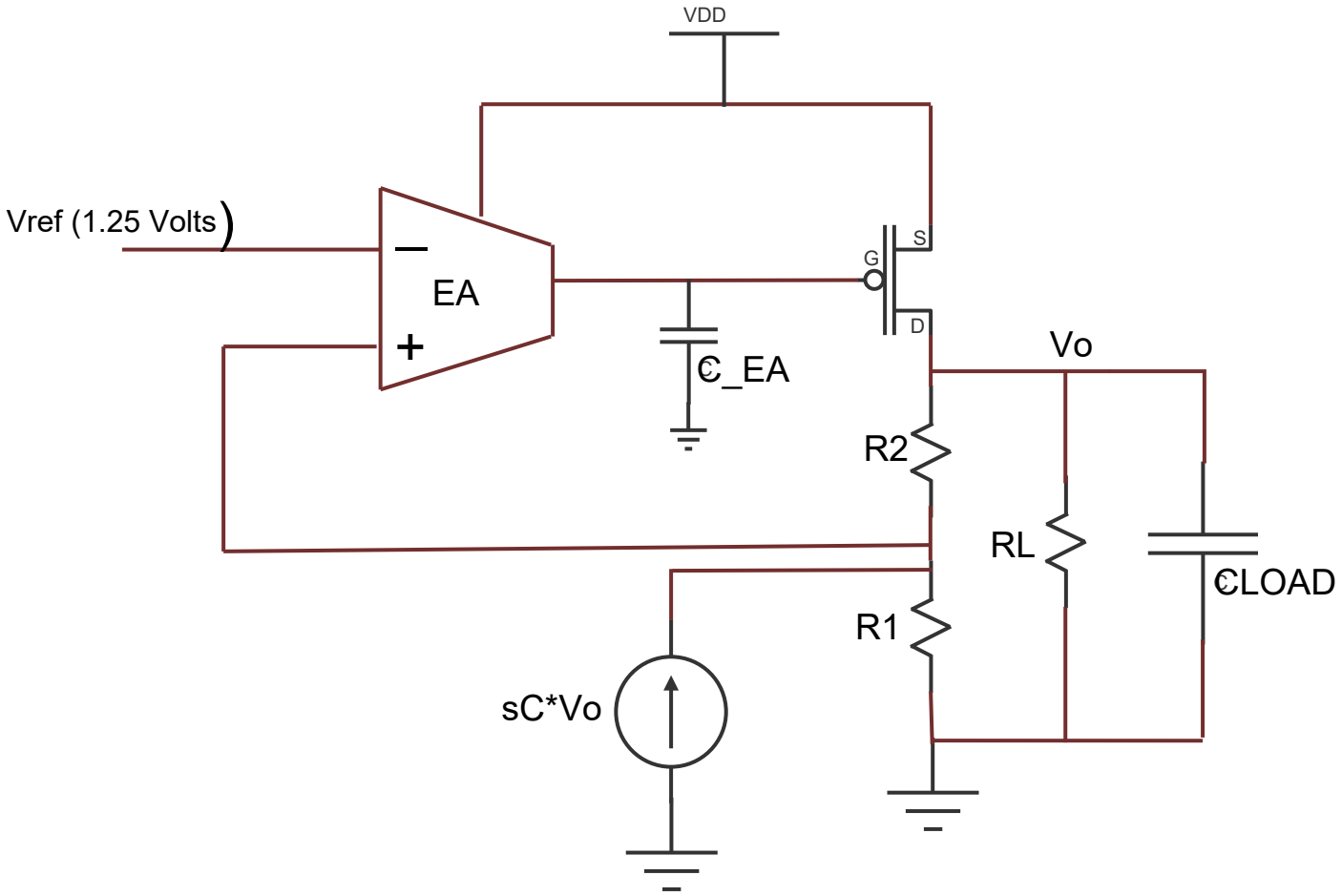
Contents :

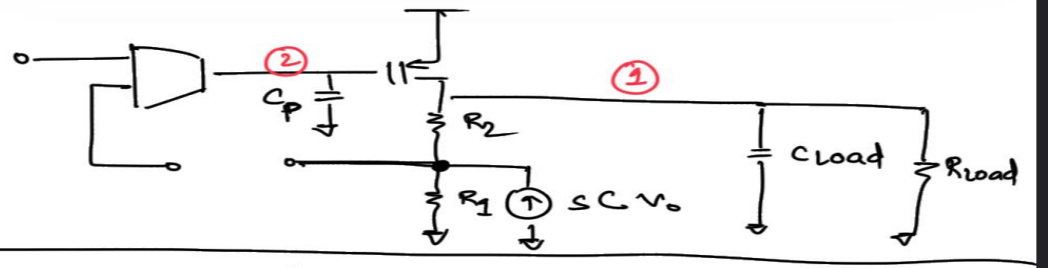
Topological Overview



VDD : 1.8 Volts
Max ILOAD : 70mA
Process : IBM 180nm
Vo : 1.5 Volts
Cload : 1uF

Specs Target :
Power Consumption < 1mW
Phase Margin > 45 degree
LG > 60 dB
PSRR > 50dB
BW >1MHz
Load Transient (1mA to 70mA) OV or UV : 0.5% (7.5mV)
Isc CL : 100mA (nominal)
Startup Slope < 7.5 KV/s (nominal)
Settling Time (Load Transient) < 2us

Stability Analysis



$LG_{(dc)} = (A_{ea}) * (A_{parasfet}) * (\beta)$

$\beta = \frac{R_1}{R_1+R_2}$

$A_{parasfet} = g_{mp} * ((R_1+R_2) \parallel R_{load} \parallel r_{dsparasfet})$

ω_{p_1} (dominant) $= \frac{1}{(R_{load} \parallel r_{ds} \parallel (R_1+R_2))\, C_{load}}$

ω_{p_2} (error AMP Node) $= \frac{1}{(R_{ea})\, C_p}$

→ where $\{ C_p = C_{as} + A_{parasfet} C_{GD} \}$

$\omega_z = \frac{1}{C R_2}$

ω_{p_2} is nearly fixed only variable is $A_{parasfet}$ in expression of C_p so

ω_z should be placed near to ω_{p_2} to cancel non-dominant pole effect

OPAMP used was two-stage current mirror opamp so there were two high-impedance nodes inside it **wp3** is at very high frequency but at high load currents when the BW increases that's when we see degradation in the phase margin

Let say wz and wp2 cancels each other perfectly, then it's a single pole roll-off

GBW = LG(dc)*wp1
= (A(ea) * gmp * Beta)/ Cload

Only thing variable here is gmp factor which increases with the load.

With the increase in load → GBW increases → Phase Margin drops down
Feedback Factor without VCCS (Vfb/Vout): R1/(R1+R2)

Feedback Factor with VCCS (Vfb/Vout) : R1/(R1+R2) * (1+sCR2)

Required C comes out to be very less than Cload (1uF)

R1,R2 Values, PASSFET Sizing , EA consideration

- Vref = 1.25 Volts , Vout = 1.5 Volts so **R1/(R1+R2) = 1.25/1.5 = 5/6**
- **Using some hand calculation & simulations, it was found that wp_EA ~ 1MHz**
- **wz (1/R2*C)should be placed around 1MHz, wz was chosen as 1.5M**
- **Effective C was around 3pF (more details in VCCS section) about how 1pF got multiplied to gives the effect of 3pF. ➔ wz = 1.5M = 1/(2*pi*R2*3p) ➔ R2 = 31.2Kohms ➔ R1 = 156Kohms**

- **Vin = 1.8 Volts , Vout=1.5 Volts , MaxILOAD = 70mA**
- **Vov (passfet) < 300mV for 70mA**
- **Sqrt(2*70m / (50e-06 * (W/L))) < 300mV for the passfet, W/L = 6m/0.2u (PASSFET size used)**

Excel Calculations about PZ Analysis

ILOAD	gm_passfet_Total	RLOAD	rds_PASSFET_TOTAL	A_PASSFET	A_DIVIDER	A_OPAMP	A_overall	wp1	wp2(EA_NODE)	wp3(EA_internal)	wz(VCCS)	GBW	PM	R_OUTPUT
1.00E-03	0.02266	1500	1629.5	**17.69826011**	0.83333333	486.6088464	7176.774944	203.7803352	1.42E+06	5.78E+07		1462485.604	68.05	781.0353092
1.00E-02	0.12432	150	193.5	**10.50476856**	0.83333333	486.6088464	4259.761092	1883.594672	1.06E+06	6.60E+07		8023663.296	50.15	84.49781659
3.50E-02	0.258	42.85714286	51.45	**6.032310838**	0.83333333	486.6088464	2446.146515	6807.206637	9.36E+05	7.30E+07		16651424.79	43.11	23.38104976
5.00E-02	0.306	30	31.67	**4.714295443**	0.83333333	486.6088464	1911.681556	10330.88603	9.11E+05	7.50E+07		19749364.29	40.43	15.40619426
7.00E-02	0.354	21.42857143	18.36	**3.500344679**	0.83333333	486.6088464	1419.415572	16096.27528	8.94E+05	7.70E+07		22847303.79	38.09	9.887979319

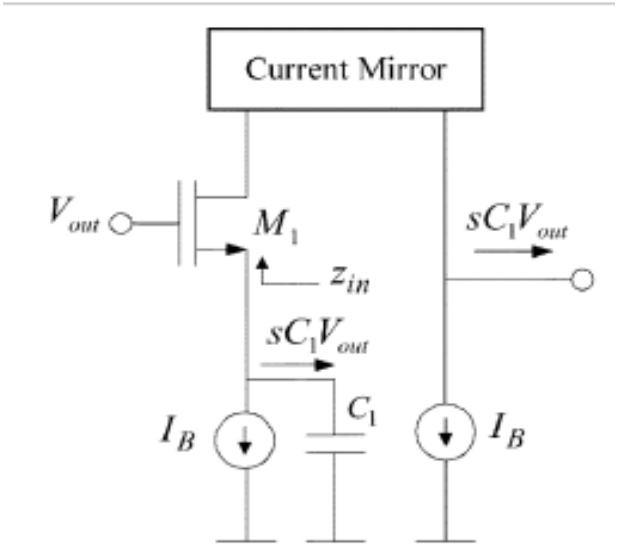
Ideal	Simulations		
A_OVERALL_dB		Max BW	22M
77.11858655	74	Min BW	1.4M
72.58770485	72.11		
67.76964932	68.41		
65.628311	66.56		
63.04219131	64.12		
			RoughNumbers
		wp2	1M
		wp3	65M

Conclusion

As the load increases the gain reduces but dominant pole also increases and its seen that GBW is increasing so it can be predicted that PM drops with ILOAD

Transconductor Design Concept

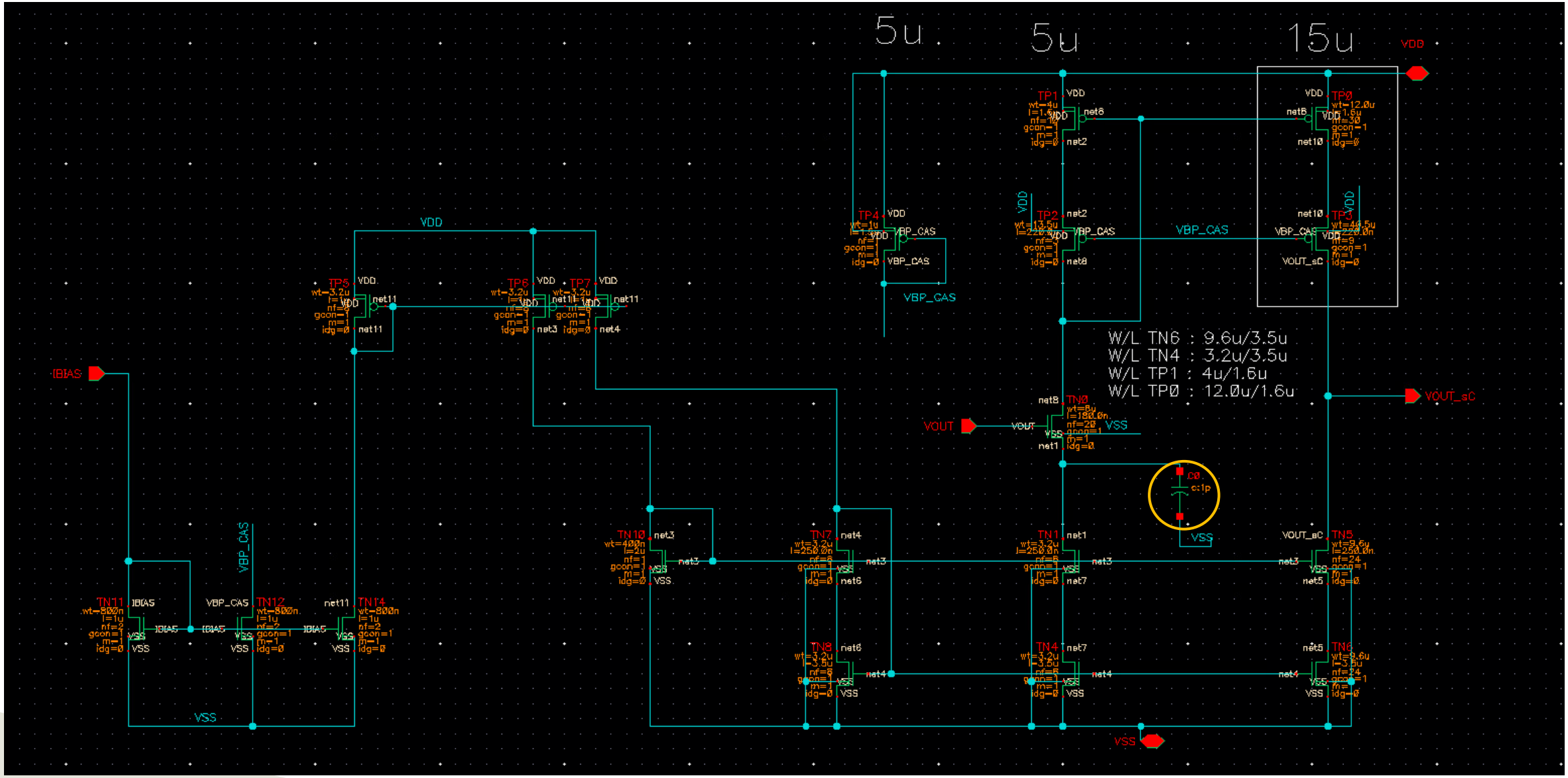
- **Key Consideration :**
- **There must very less mismatch among the top & bottom current sources else its gonna directly impact the output voltage.**
- **Systematic mismatch taken care : ensuring VDS same using low-swing cascode current mirror.**
- **Random Mismatch Taken Care : by ensuring that current mirror devices have higher overdrive (lower gm).**
- **Output impedance >> R1 (as it will impact the loop gain directly)**



$$\frac{i_{out}}{v_{out}} = \frac{sC_1}{1 + \frac{C_1}{g_{m1}}s}.$$

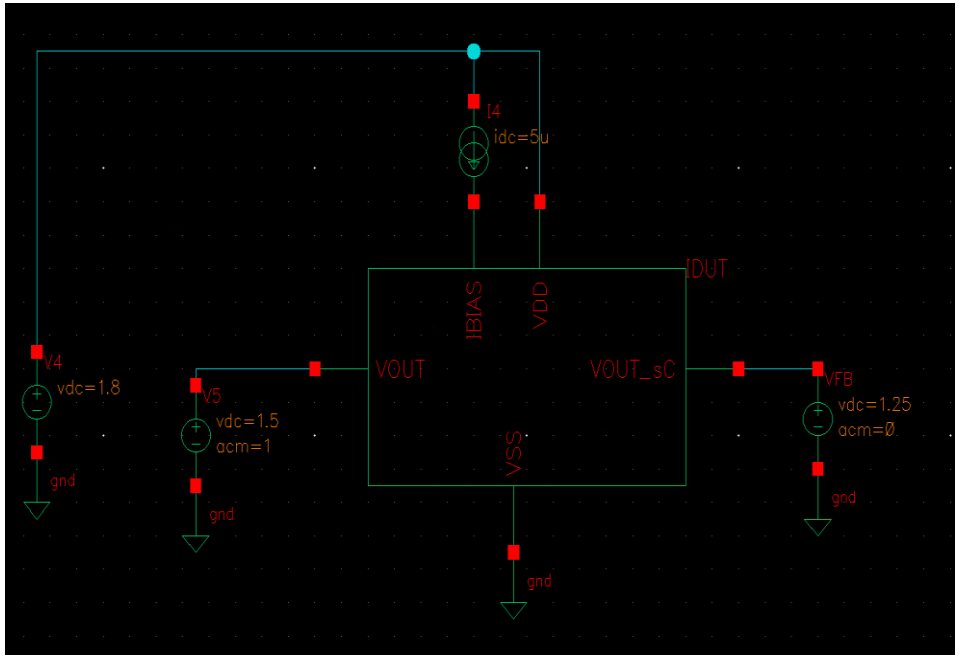
Gm1 is sized such that this pole is also pushed outside the BW.

VCCS Schematics

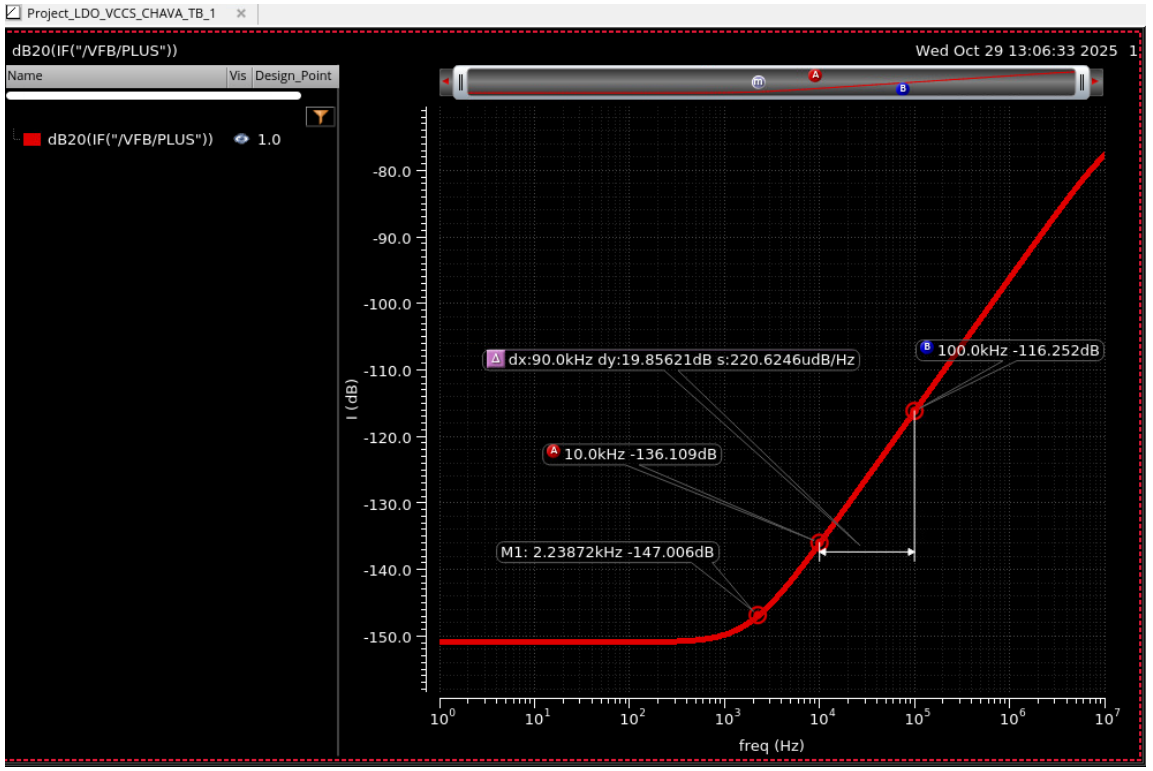


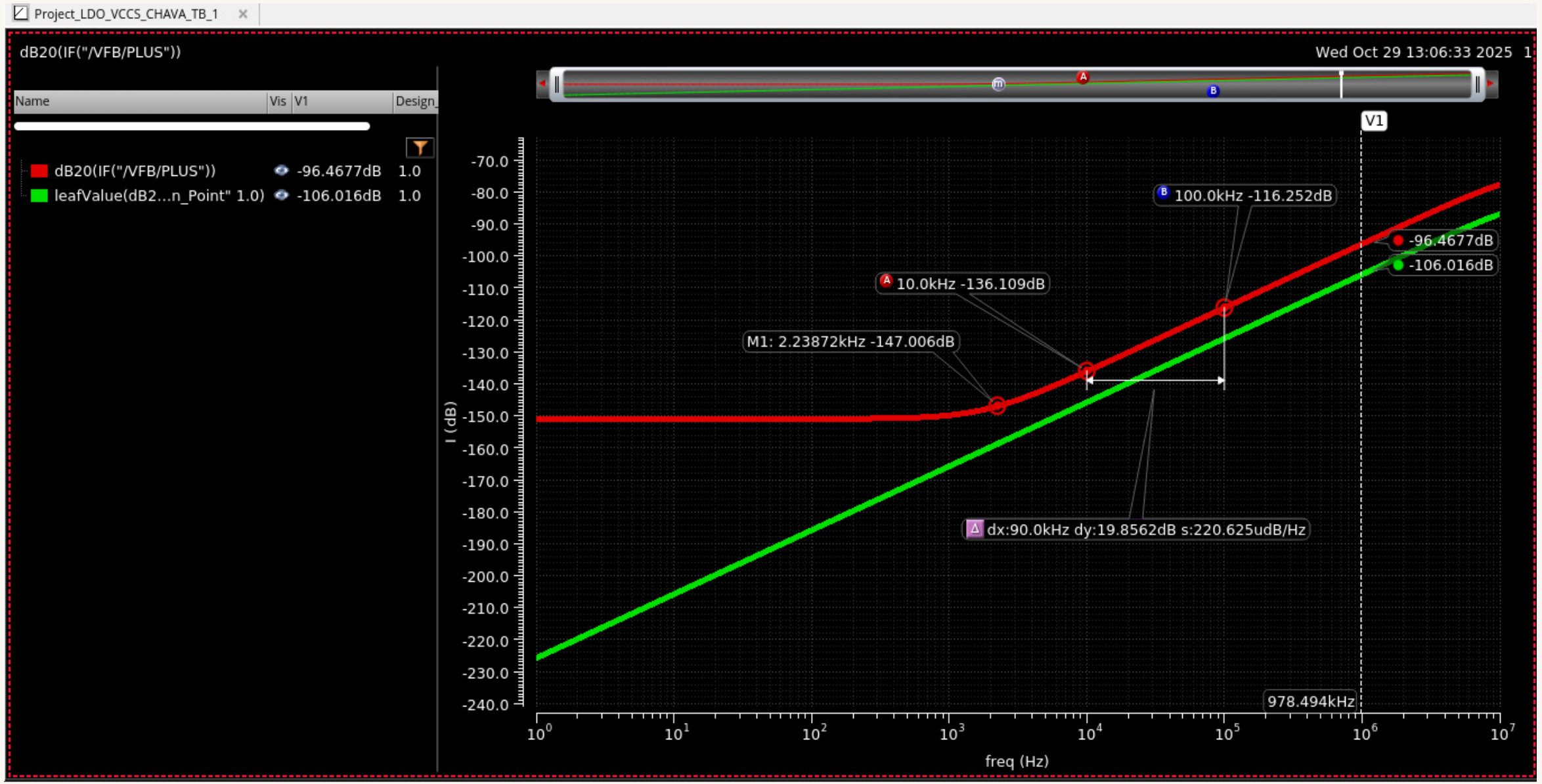
VCCS TB & Sim Result

- There is 3X current multiplication inside so the effective cap will be 3pF & wz in the LDO loop will be at 1/(3p*R2)



Project_LDO_VC...	abs(OP("/IDUT/TP0" "ids"))	16.17u
Project_LDO_VC...	IS("/VFB/PLUS")	-33.79n
Project_LDO_VC...	abs(OP("/IDUT/TN6" "ids"))	16.21u

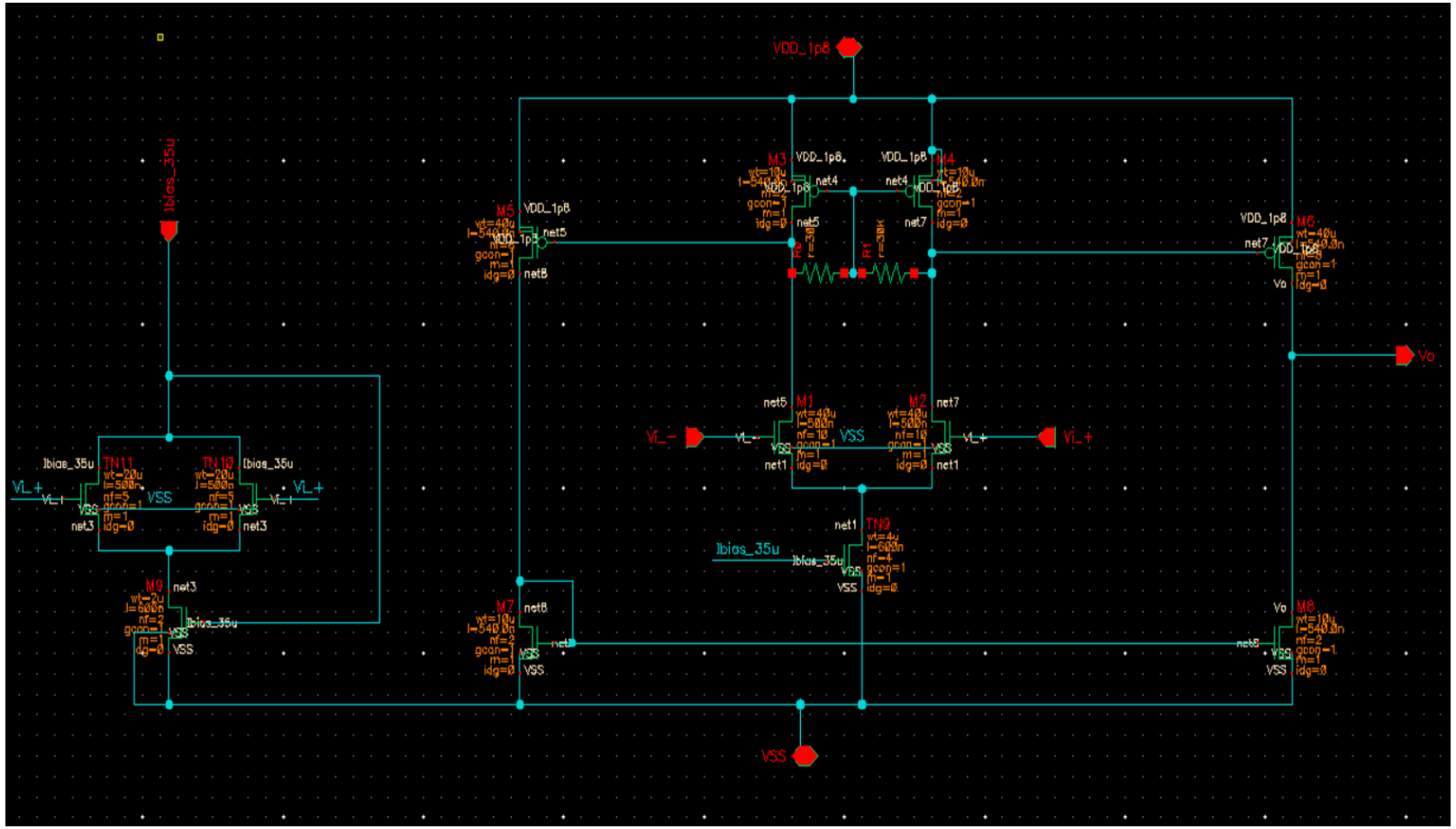



Project_LDO_VCCS_CHAVA_TB_1
dB20(IF("/VFB/PLUS"))
Wed Oct 29 13:06:33 2025
Name
Vis
V1
Design_
dB20(IF("/VFB/PLUS")) -96.4677dB 1.0
leafValue(dB2...n_Point" 1.0) -106.016dB 1.0
V1
100.0kHz -116.252dB
-96.4677dB
-106.016dB
10.0kHz -136.109dB
M1: 2.23872kHz -147.006dB
dx:90.0kHz dy:19.8562dB s:220.625udB/Hz
978.494kHz
I (dB)
freq (Hz)

Explanation : VCCS Result

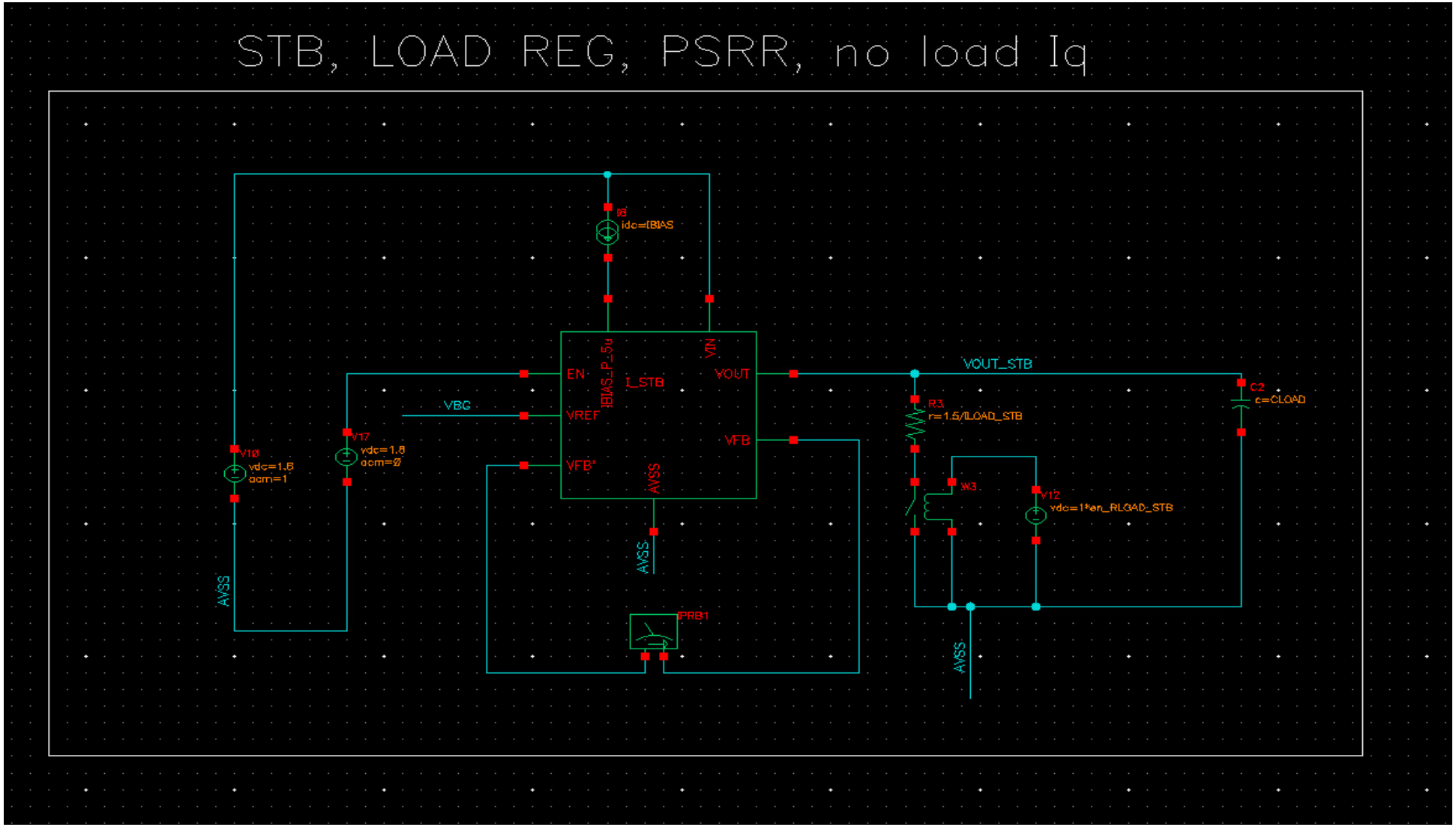
- The current curve seems to have some offset its not exactly (s*3CVo), its coming due to current mismatch between the bottom and top mirror which is around 33nA as shown on previous slide.
- Now **iout = 33nA + s(3p*Vout)** {Vout will also be attenuated due to source follower structure but not by very large amount}
- Zero location : 33nA/(3p*2*pi) ~ **2KHz** (as can be seen in the plot).
- This **offset don't affect the zero location in the LDO loop** a lot.
- Vertical V1 on slide9 marker shows the **20log(3) : 9.54dB** difference between the current flowing at the output vs current in the internal capacitor which depicts the current multiplication.

Error Amp Design

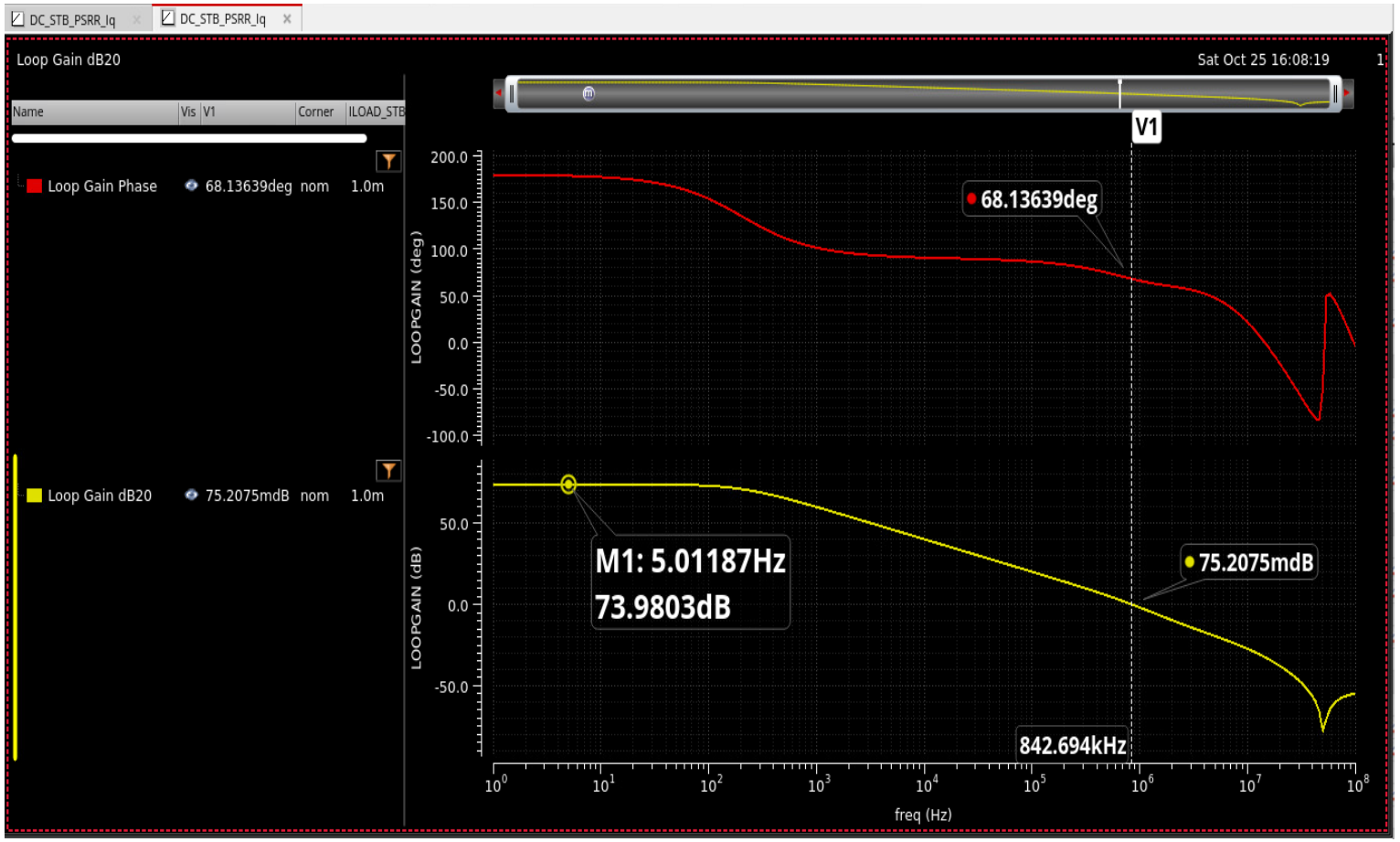


Current mirror based opamp
DC gain : 53dB
Two high impedance nodes but don't require
Pole-splitting as passfet cap (cgs+Acgd) will
Make the output node dominant and internal will be
At a higher frequency.

DC TestBench



DC Nominal Results



At lowest load :
Loop Gain will be Max (74dB) here & bandwidth will be lowest.(0.842 MHz)

So for loop gain spec meeting it was ensured that at max load LG>60dB.

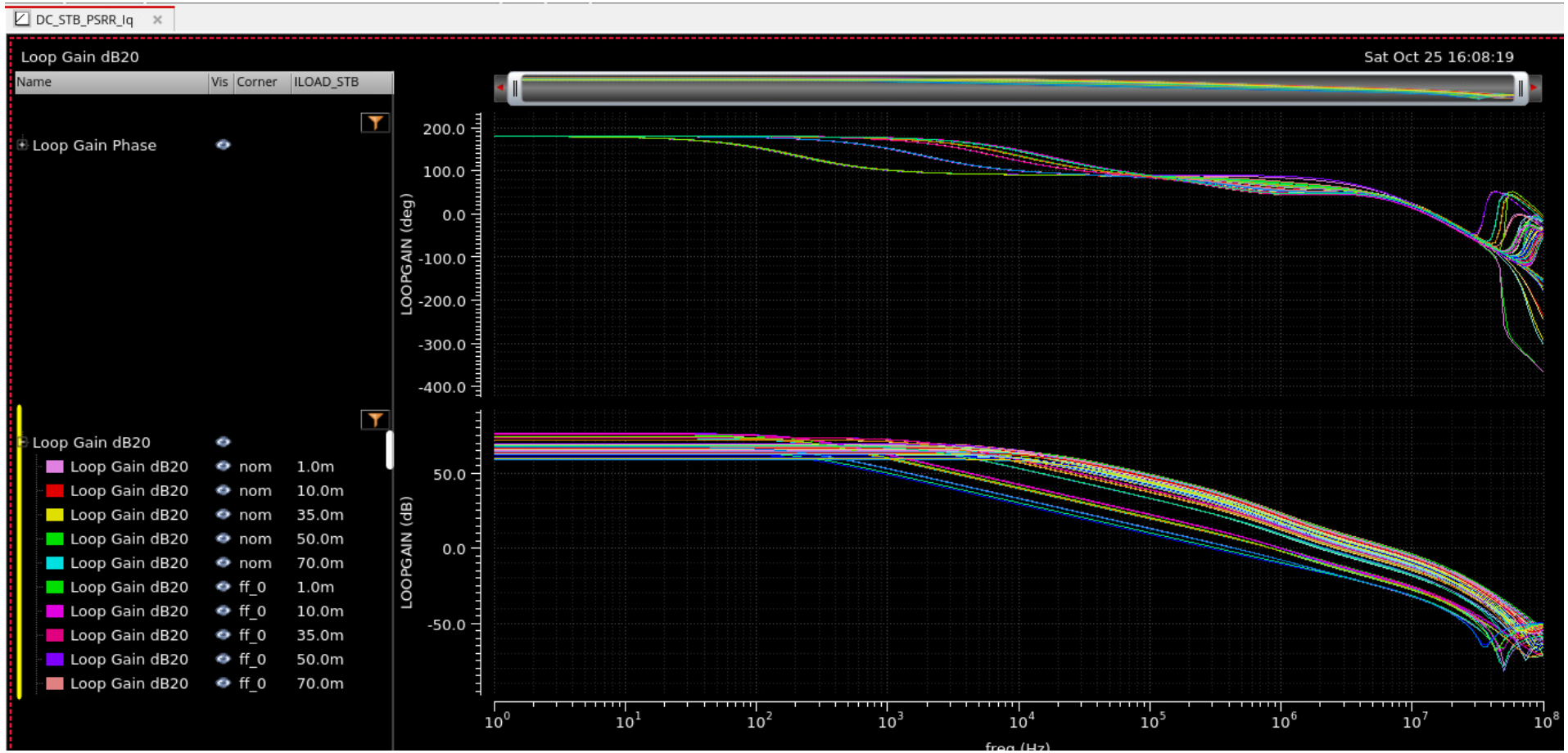
DC Results (Across PVT, Loads (1mA-70mA))

Point	Test	Output	Nominal	Spec	Weight	Min	Max
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
Parameters: ILOAD_STB=1m							
1	DC_STB_PSRR_Iq	DC_LOOPGAIN	73.98			63.17	76.43
1	DC_STB_PSRR_Iq	Phase Margin	68.05			61.47	89.63
1	DC_STB_PSRR_Iq	PSR_DC	43.34			41.96	43.86
Parameters: ILOAD_STB=10m							
2	DC_STB_PSRR_Iq	DC_LOOPGAIN	72.11			67.81	73.54
2	DC_STB_PSRR_Iq	Phase Margin	50.15			48.73	52.36
2	DC_STB_PSRR_Iq	PSR_DC	43.65			42.34	44.14
Parameters: ILOAD_STB=35m							
3	DC_STB_PSRR_Iq	DC_LOOPGAIN	68.41			64.41	69.99
3	DC_STB_PSRR_Iq	Phase Margin	43.11			38.39	46.46
3	DC_STB_PSRR_Iq	PSR_DC	44.04			42.89	44.52
Parameters: ILOAD_STB=50m							
4	DC_STB_PSRR_Iq	DC_LOOPGAIN	66.56			62.17	68.33
4	DC_STB_PSRR_Iq	Phase Margin	40.43			34.67	45.37
4	DC_STB_PSRR_Iq	PSR_DC	44.25			43.22	44.72
Parameters: ILOAD_STB=70m							
5	DC_STB_PSRR_Iq	DC_LOOPGAIN	64.12			59.17	66.16
5	DC_STB_PSRR_Iq	Phase Margin	38.09			31.43	44.52
5	DC_STB_PSRR_Iq	PSR_DC	44.56			43.62	45.13

Lowest BW case (0.27M)

Max BW case (7M)

DC Results (Across PVT, Loads (1mA-70mA))



Monte Carlo Sim (Accuracy & Stb)

Test	Name	Yield	Min	Target	Max	Mean	Std Dev	Cpk	Errors
Yield Estimate: 100 %(75 passed/75 pts)	Confidence Level: <not set>	Filter: <not set>							
	DC_STB_PSRR_Iq								
	DC_LOOPGAIN(summary)	100% (75/75)	71.93	info	72.22	72.06	66.82m		0
	DC_LOOPGAIN	100% (75/75)	71.93	info	72.22	72.06	66.82m		0
	Phase Margin(summary)	100% (75/75)	44.61	info	46.42	45.41	403.6m		0
	Phase Margin	100% (75/75)	44.61	info	46.42	45.41	403.6m		0
	PSR(summary)	0% (0/75)	0	info	0	0	0		75
	PSR_DC(summary)	0% (0/75)	0	info	0	0	0		75
	VS("/VOUT_STB")(summary)	100% (75/75)	1.49	info	1.514	1.502	5.137m		0
	VS("/VOUT_STB")	100% (75/75)	1.49	info	1.514	1.502	5.137m		0
	Iq(summary)	100% (75/75)	-529.4u	info	-451.8u	-484u	14.79u		0
	Iq	100% (75/75)	-529.4u	info	-451.8u	-484u	14.79u		0

Specs vs. Stat Param | Mismatch Contribution | +

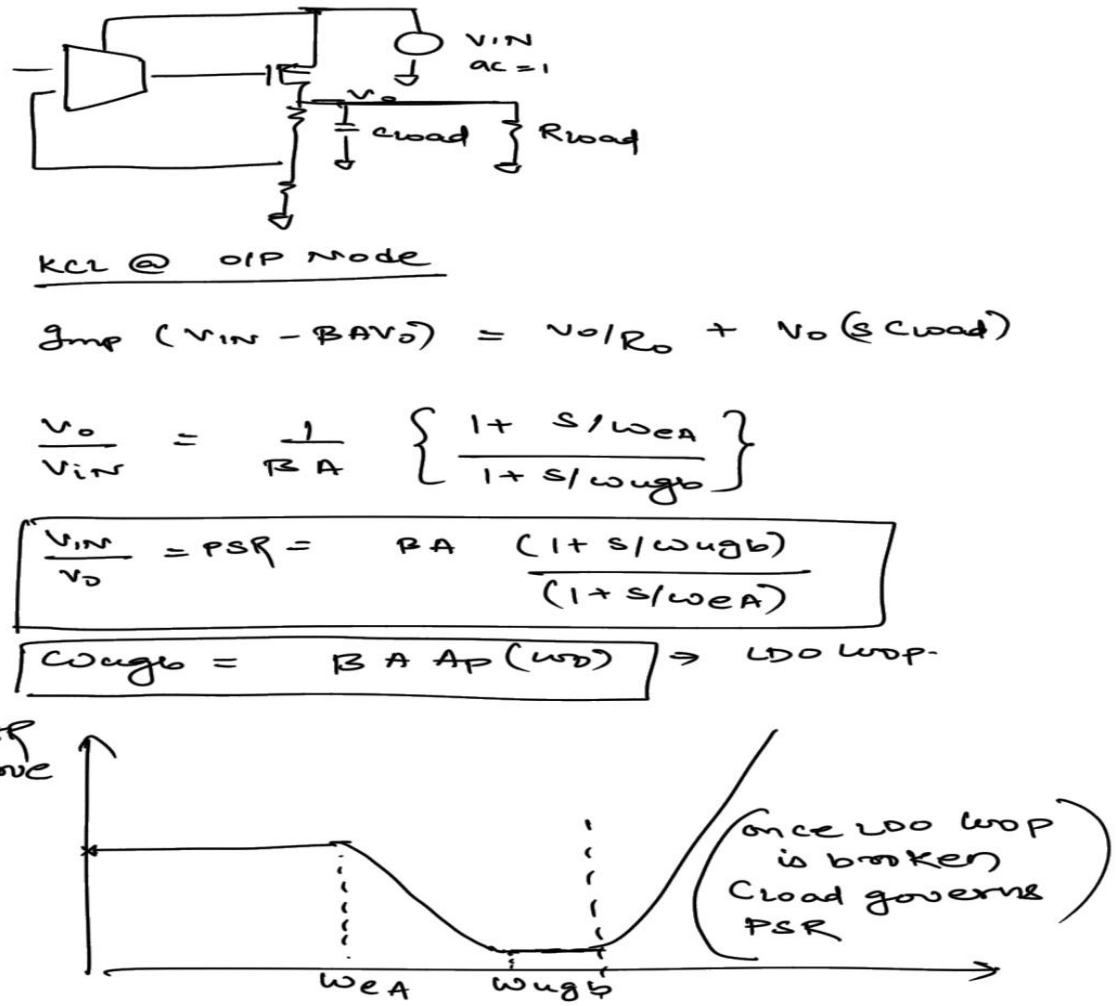
Tests | View | Corners | Plot Mode: Replace

Max Contribution: 1% | Yield: 100% | >>

	Max	DC_LOOPGAIN Nominal Yield = 100.00% R^2 = N.A.	Phase Margin Nominal Yield = 100.00% R^2 = 0.91066	PSR Nominal Yield = 0.00% R^2 = N.A.	PSR_DC Nominal Yield = 0.00% R^2 = N.A.	VS("/VOUT_STB") Nominal Yield = 100.00% R^2 = 0.92456	Iq Nominal Yield = 100.00% R^2 = 0.94031
Top		100%	100%	N.A.	N.A.	100%	100%
/I_STB/I_VCCS/TN4		7%	0%	N.A.	N.A.	44%	0%
/I_STB/I_OTA/M9		7%	21%	N.A.	N.A.	0%	35%
/I_STB/I_VCCS/TP1		4%	0%	N.A.	N.A.	27%	0%
/I_LOAD_TRAN/TN9		21%	0%	N.A.	N.A.	0%	0%

Results @ 1mA Load, just to get the idea of the current mismatch in the VCCS block, the delta current directly shows in the Vout.
Iq : 484uA (nominal) → Power Consumption (nominal) : 0.484mA * 1.8 : 0.87mW

PSRR Analysis

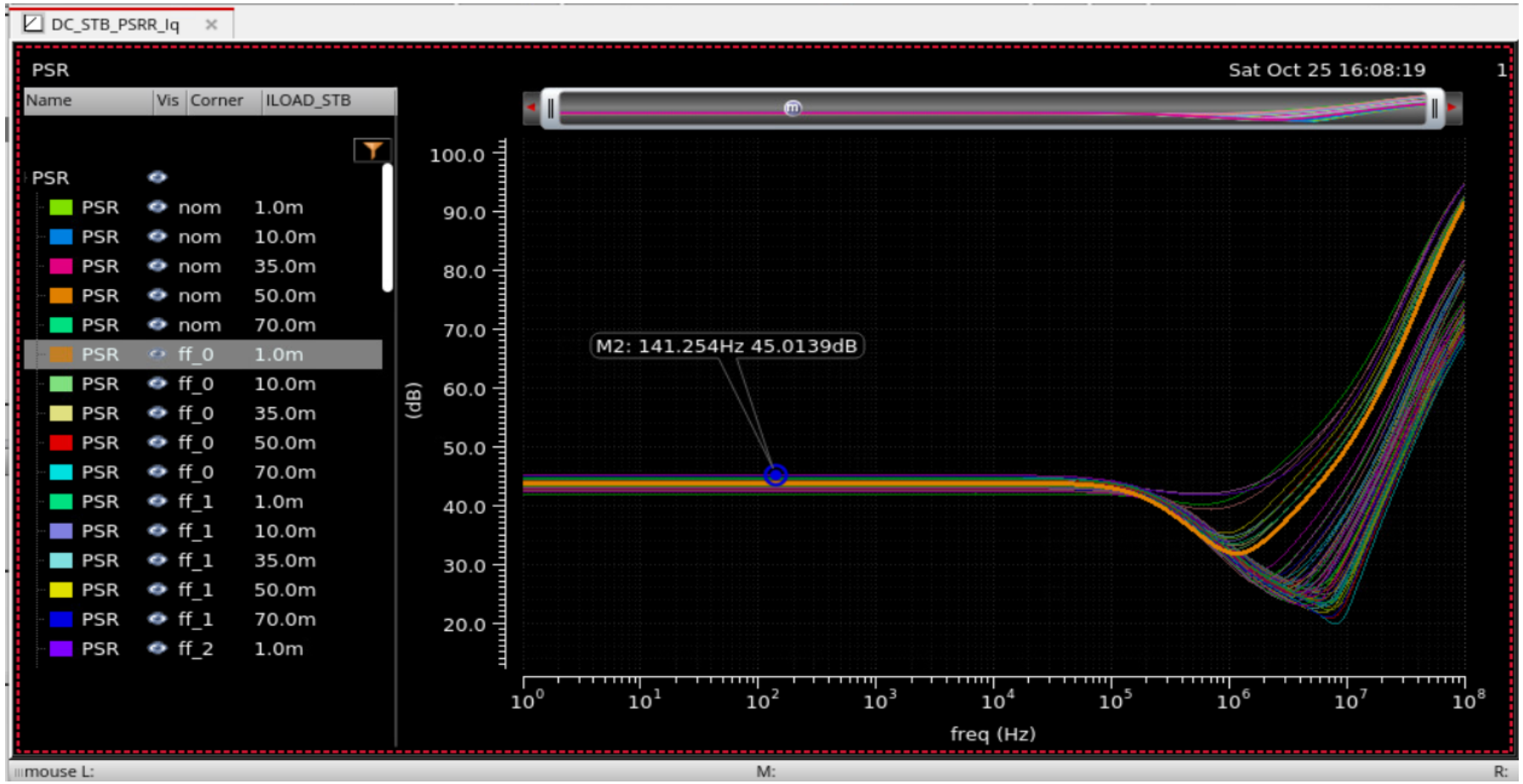


LDO PSR curve with output pole dominant seems to have 3 sections :

1) DC PSR governed by error-AMP gain and beta factor
2) Start falling after the error amp output pole
3) After the LDO loop is broken (loop is dead around LDO loop ugb), the output ripple is governed by the cap.

Across the load the DC PSR will remain nearly the same as its load -independent.
Pole remain same
Only thing that changes across the load is the ugb, the point Where the loop breaks.

PSRR Across Loads



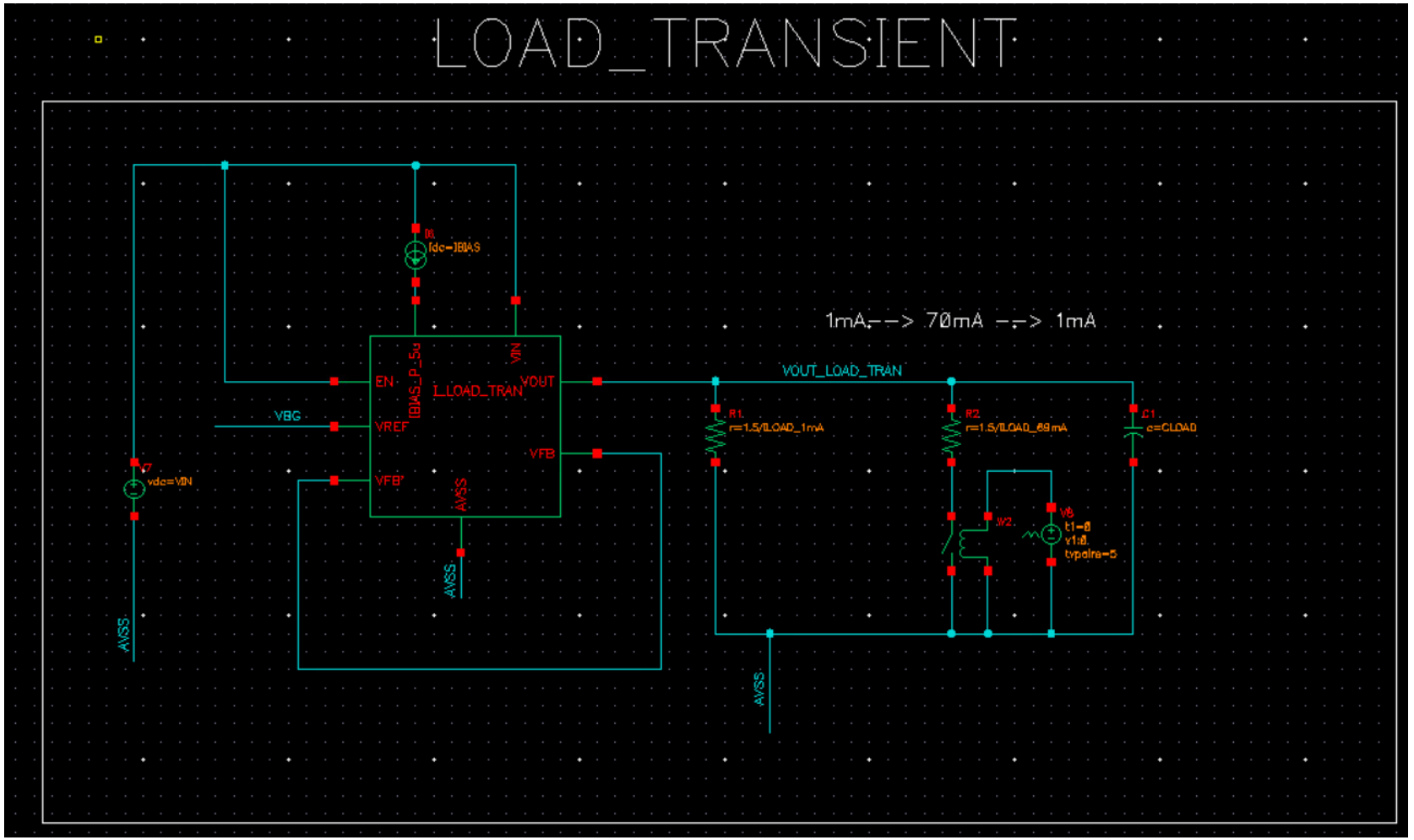
Load Transient Nom Curve

- Load Transient depends on multiple aspects : amount of Cap at the output, bandwidth, how well the error amp can drive the passfet (slew rate), the amount of load change during transient.

- $\Delta Vout = \Delta I/Cload * (1/BW + \Delta Vgs/SR)$

- Testbench Setup : Resistor load was switched to emulate the load-transient effect.

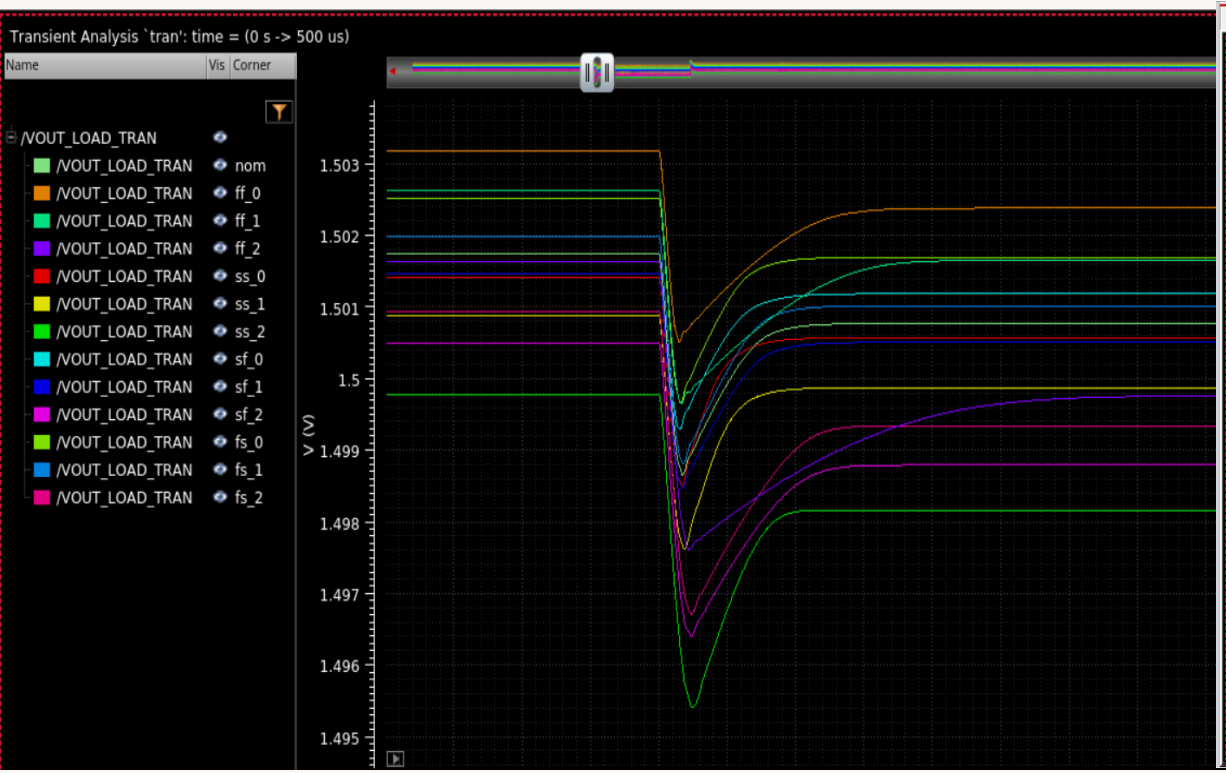
Load-Transient Testbench



Load Transient Across PVT

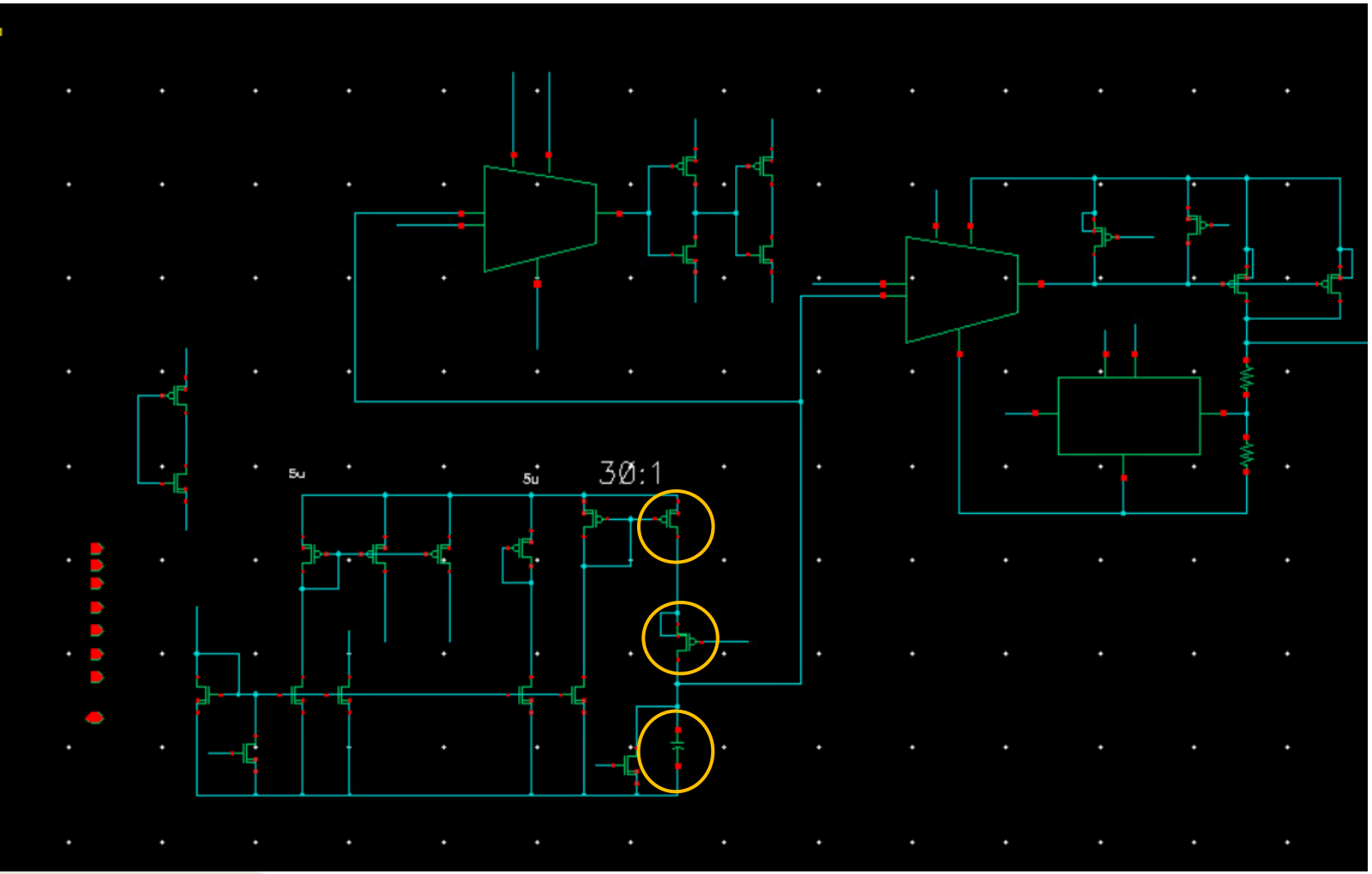
Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max
LOAD_TRANSIENT	I_RES						
LOAD_TRANSIENT	VOUT_1mA	1.502				1.5	1.503
LOAD_TRANSIENT	VOUT_70mA	1.501				1.498	1.502
LOAD_TRANSIENT	LOAD_REG	966.8u				802.4u	1.876m
LOAD_TRANSIENT	ymin_vout	1.499				1.495	1.501
LOAD_TRANSIENT	ymax_vout	1.503				1.501	1.504
LOAD_TRANSIENT	US_VOUT	2.113m	< 0.003			1.868m	2.749m
LOAD_TRANSIENT	OS_VOUT	1.297m	< 3m			1.088m	1.555m
LOAD_TRANSIENT	t_ymin	100.1u				100.1u	100.1u
LOAD_TRANSIENT	t_ymax	152.1u				152.1u	152.1u
LOAD_TRANSIENT	ts_1m_70m	1.225u				327.2n	2.748u
LOAD_TRANSIENT	ts_70m_1m	1.613u				1.381u	3.855u

Settling time when load goes from 70mA to 1mA is generally higher as output is discharged by the resistive ladder whose time constant is higher. On the contrary when load goes from 1mA to 70mA output experiences a dip and settling time is defined by the bandwidth and time it takes to charge the gate node which depends on the error ramp slew rate.


Transient Analysis `tran': time = (0 s -> 500 us)
Name
Vis
Corner
/VOUT_LOAD_TRAN
/VOUT_LOAD_TRAN nom
/VOUT_LOAD_TRAN ff_0
/VOUT_LOAD_TRAN ff_1
/VOUT_LOAD_TRAN ff_2
/VOUT_LOAD_TRAN ss_0
/VOUT_LOAD_TRAN ss_1
/VOUT_LOAD_TRAN ss_2
/VOUT_LOAD_TRAN sf_0
/VOUT_LOAD_TRAN sf_1
/VOUT_LOAD_TRAN sf_2
/VOUT_LOAD_TRAN fs_0
/VOUT_LOAD_TRAN fs_1
/VOUT_LOAD_TRAN fs_2
1.503
1.502
1.501
1.5
1.499
1.498
1.497
1.496
1.495
V (V)


Window 3
Transient Analysis `tran': time = (0 s -> 500 us)
Name
Vis
Corner
/VOUT_LOAD_TRAN
/VOUT_LOAD_TRAN nom
/VOUT_LOAD_TRAN ff_0
/VOUT_LOAD_TRAN ff_1
/VOUT_LOAD_TRAN ff_2
/VOUT_LOAD_TRAN ss_0
/VOUT_LOAD_TRAN ss_1
/VOUT_LOAD_TRAN ss_2
/VOUT_LOAD_TRAN sf_0
/VOUT_LOAD_TRAN sf_1
/VOUT_LOAD_TRAN sf_2
/VOUT_LOAD_TRAN fs_0
/VOUT_LOAD_TRAN fs_1
/VOUT_LOAD_TRAN fs_2
M1: 152.1203us 1.504289V
1.505
1.504
1.503
1.502
1.501
1.5
1.499
1.498
1.497
1.496
1.495
V (V)
137.5
140.0
142.5
145.0
147.5
150.0
152.5
155.0
157.5
160.0
162.5
165.0
167.5
time (us)

Soft-Start Schematic

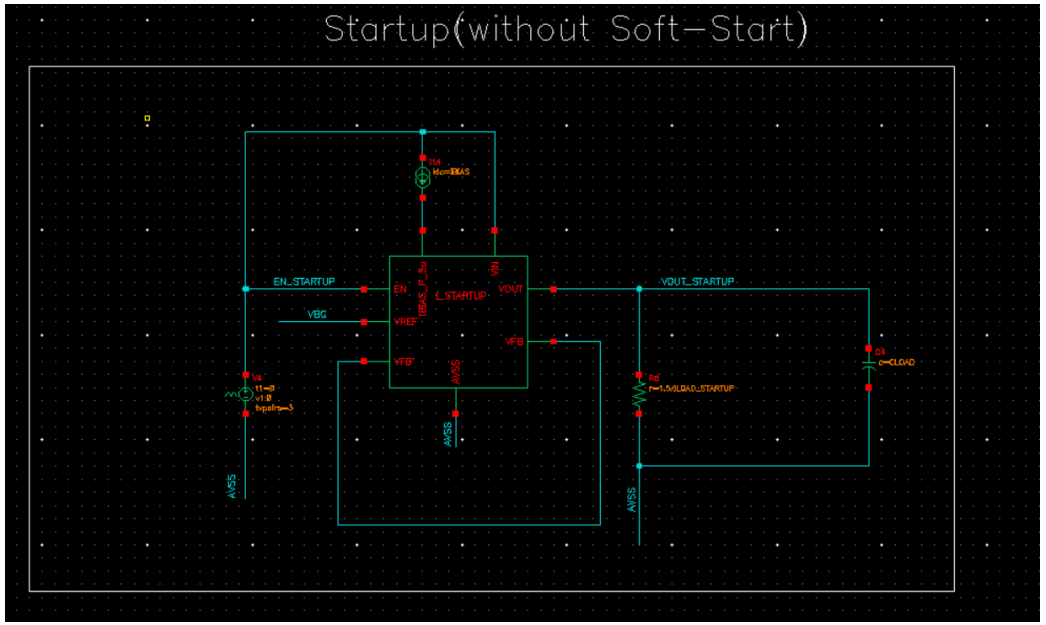


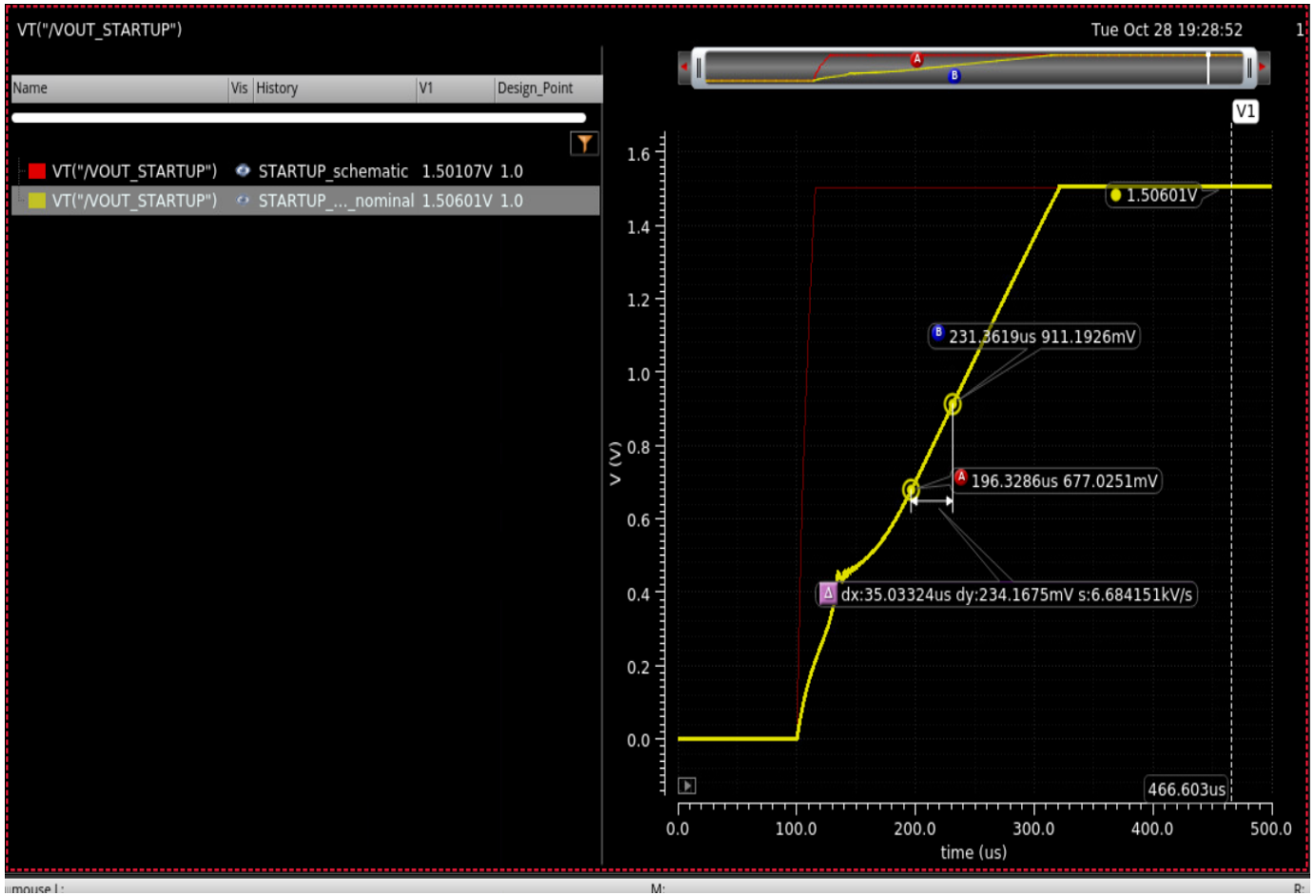
Concept :
As the LDO is enabled reference to the LDO will start to ramp instead of being present from the start which drives the passfet very strong.
Small Current (Topmost circle)
Charges the capacitor slowly and reference is simultaneously compared with 1.25 Volts as well, so as the LDO_REF becomes equal to 1.25 Volts the comparator which is used open the path to charge the capacitor and LDO continues with usual operation.

d(Vout)/dt = (6/5) * d(Vref)/dt

d(Vref)/dt = Ibias/C
To control the ramp rate the current can be made even smaller.

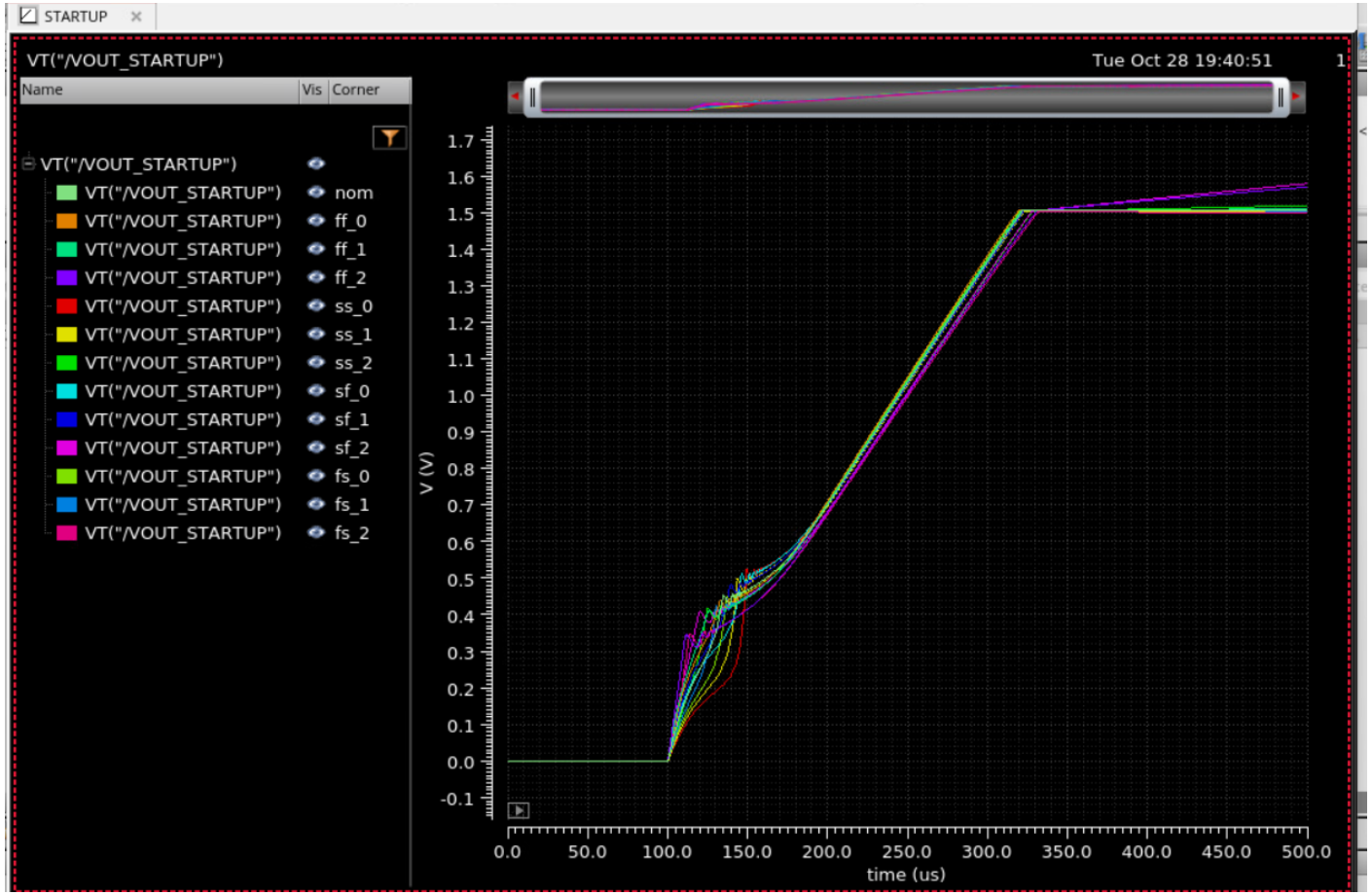
StartUP Sims



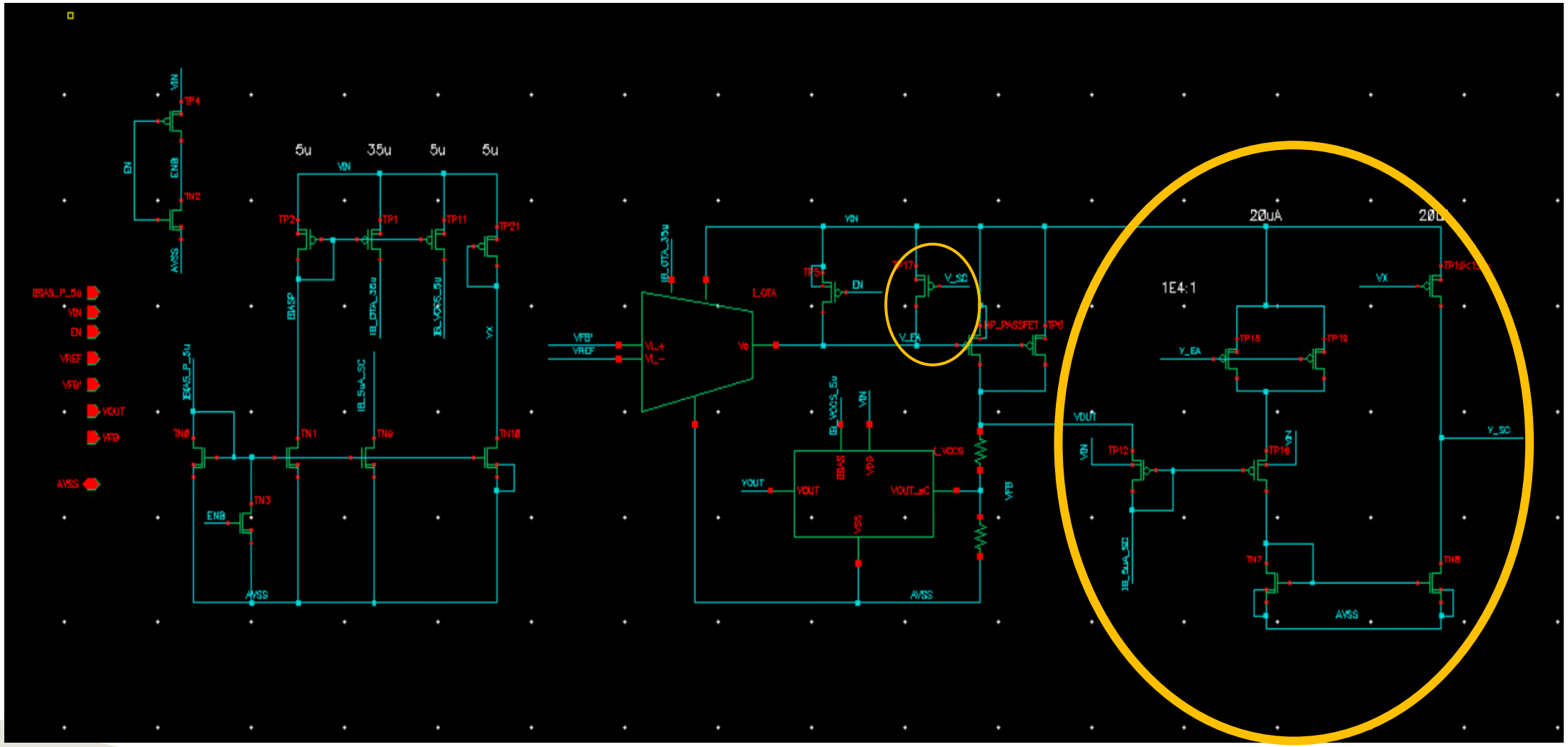


Yellow Curve represents the soft-start enabled startup

StartUP Sims (Across Process)



Short Circuit Limit Circuit



Short CKT CL TestBench

- Load Transient testbench was used with load switching between 1mA and 200mA equivalent resistor.

- Since short circuit was set to 100mA (nominal), passfet gate node was clamped to higher voltage and LDO couldn’t provide the current and LDO was out of regulation.

Short Circuit CL Results (Process & Temp)

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max
C_CL	I_RES						
C_CL	VOUT_1mA	1.502				1.5	1.503
C_CL	VOUT_70mA	784.7m				683.2m	977.1m
C_CL	I_SC_CL	105.1m				91.54m	130.9m

Summary

		SPEC		
Parameter	MIN	TYP	MAX	Notes
Loop Gain (dB)	59.17		76.43	Min occurs at max load condition
Phase Margin	31.43		89	Min occurs at max load condition
UGB (MHz)	0.28		7.29	Max occurs at max load condition at fast corner, min at min load 0 degree
PSR (dB)	42			
Load-Transient (OV) mV	1.088	1.297	1.555	
Load-Transient (UV) mV	1.868	2.113	2.749	
StartUP Slope		6.28 KV/s		
SC Current Limit	91.54mA	105mA	130.9mA	
Power Consumption		0.87mW		
ts settling time 1mA -->70mA		1.225us		
ts settling time 70mA -->1mA		1.613us		

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THANK YOU