A 10Gb/s SEGMENTED VOLTAGE-MODE TRANSMITTER WITH 3-TAP HIGH RESOLUTION EQUALIZATION

A Project Final Report

by

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Abstract

This document is a final report of our final project for the ECEN 720 High Speed Serial Links Circuits and Systems class. Transmitters are important components of an I/O chip, and a good design can help us administer higher data rates through a lossy channel as well as reduce the complexity of the receiver. Equalization is the most effective measure to counter the effects of Inter-Symbol Interference (ISI) and the complexity cost to implement it on the transmitter side is relatively low. The two common transmitter topologies are voltage-mode and a current-mode logic (CML) design. Throughout the report, we will be describing the design of a high-swing voltage-mode transmitter with a 3-tap FIR equalization with a good resolution to compensate for the ISI effects for the B1, C4 and T20 channels.

ACKNOWLEDGEMENTS

We would like to thank our instructor, Dr Palermo for teaching this course and allowing us an in-depth exposure to high-speed I/O, both at the circuits and system level. The knowledge gained in the class has enabled us to complete this project. We also wish to thank our TA, Srujan Kumar Kaile, who was very helpful and patient towards the discussions we had with him regarding projects and labs.

A sincere thanks also goes to our parents for their support and the class peers for engaging in insightful brainstorm sessions to counter any problems we faced.

NOMENCLATURE

ISI	Inter-Symbol Interference
CML	Current-Mode Logic
LUT	Look-Up Table
CTLE	Continuous Time Linear Equalizers
TX	Transmitter
RX	Receiver
ADS	Advanced Design System (software)
BER	Bit Error Rate
DAC	Digital-to-Analog Converter
PWM	Pulse-Width Modulation

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CHAPTER I

INTRODUCTION

Power dissipation in I/O chips continues to increase and with the scaling data rates, the aim is that the power budget should not increase by the same rate. The rapid development of various computation and communication platforms has driven the need for wireline links to support significantly higher per-pin I/O bandwidths. As data rates scale, the equalization circuit complexity increases. Equalization on the transmitter side is a simple way to improve the signal eye height without going into receiver side timing complexities or noise/jitter amplification (from CTLEs).

There are multiple benefits to TX side equalization. It can be implemented using simple FIR filters with pre/post cursor weights. We describe this in detail in the upcoming sections.

Motivation

The pursuit of higher energy efficiency in serial links has popularized the use of voltage-mode transmitter over CML ones, despite the latter being less complex in terms of design. Voltage-mode transmitters ideally have 4x lower power consumption as compared to the CML counterpart. These transmitters need to support the impedance matching and de-emphasis as well as amplitude control to enable reduce power on clean channels.

For our design, we aim to maintain a close balance between design complexity and power dissipation. From our initial simulation results (next chapter) we concluded that a 3-tap equalization (1-pre, 1-main, 1-post) is enough to compensate for the ISI in the three channels. We list the key specifications we aim to achieve in the table below.

Table 1 Target Specifications for the design

Specification	*Value*
Channels	B1, C4 & T20

Data rate	10 Gb/s
Transmitter output swing	900mV
Receiver sensitivity (at BER=10^{-12})	$20mV_{ppd}$
Timing margin (at BER=10^{-12})	0.3UI
Power Consumption	-

Project Overview

This project describes the design of a 3-tap 10Gb/s voltage-mode transmitter for 3 lossy channels (C4, B1 and T20). Equalization is much easier to implement in a current mode transmitter by adding current weights which flow through the TX termination. However, if we want the low power benefits of a voltage-mode transmitter, we need to deal with the complexity it comes with. This project is going to discuss a particular segmented voltage driver approach to cancel pre and post cursor ISI. The format of this report is as follows: Chapter I introduces the concept and explains the motivation behind this topic. Chapter II summarizes previous work, any inspirations drawn from already existing architectures and a summary of the pros and cons of each architecture. Chapter III focuses on the proposed architecture and the design choices made and deals with some initial simulation results such as channel characterization, finding tap weights and ADS system simulations to check achievable eye heights and bit error rates (BER) for each channel. Chapter IV discusses the simulation results proving the working and theory of your design.

CHAPTER II

LITERATURE SURVEY

There are multiple topologies for implementing equalization in a voltage mode transmitter. In this section, we will briefly discuss a few approaches that we considered while making the design choice.

Hybrid Voltage-Mode Transmitter with Current-Mode Equalization

Most voltage mode drivers are implemented using a segmented DAC approach which requires multiple segments of the same driver and additional predriver circuitry. The hybrid voltage-mode transmitter [1] aims to solve the problem of sophisticated equalization using current mode drivers. In contrast with voltage mode drivers that require significant circuit complexity and overhead as the number of taps and the resolution increases, with the current mode logic (CML) driver, we're able to implement high resolution equalization without all the complexity. Similar to a CML transmitter, the tap weights are set using tail-current source digital-to-analog converters (DACs).

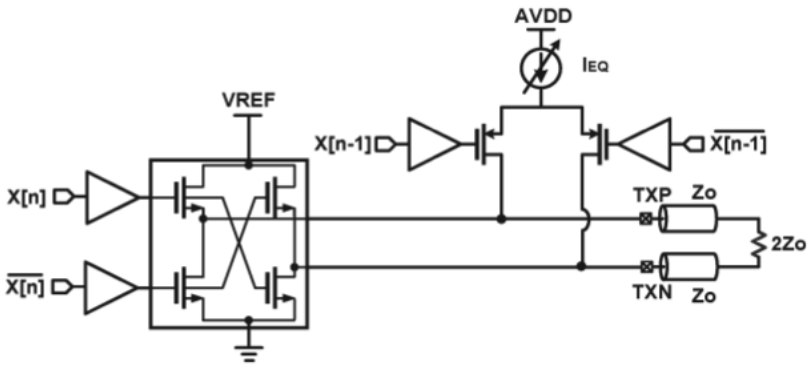

Figure 1 2-tap FIR equalization in hybrid voltage transmitter with CML equalization [1]

The main cursor bit driver is still the voltage mode transmitter, which allows us to retain the low power benefits of a voltage-mode driver as shown in Fig. 1.

Energy Efficient Voltage-Mode Transmitter Using Time-Based De-Emphasis

The voltage-mode transmitter has excellent benefits in terms of power consumption but is not particularly suited for de-emphasis-based equalization. This approach [2] views de-emphasis as a time-based technique rather than impedance-based control in [4] [6]. A pulse-width modulated (PWM) pulse with a duty cycle D, can be expressed as,

$$p_{pwm}(t) = u(t) - 2u(t - DT) - u(t - T)$$

where T is the bit period, and u(t) is a step function. According to [3] the intersymbol interference (ISI) due to channel loss can be minimized by choosing D between 0.5 and 1. This is intuitive because in time domain, a bit is a step response that lasts for one bit period. If we reduce the duty cycle of the bit, we are essentially shrinking the width of the impulse response, hence minimizing the intersymbol interference. This is evident from Fig. 2.

Even though this promises a simple way to reduce ISI in high loss channel, this technique is very susceptible to clock jitter and skew. As we decrease pulse width, we also need to consider the setup and hold time for the output pulse to the slicer on the RX side for proper quantization. The effectiveness of PWM equalization at higher data rates will be low as pulse widths get narrower in smaller feature length technologies.

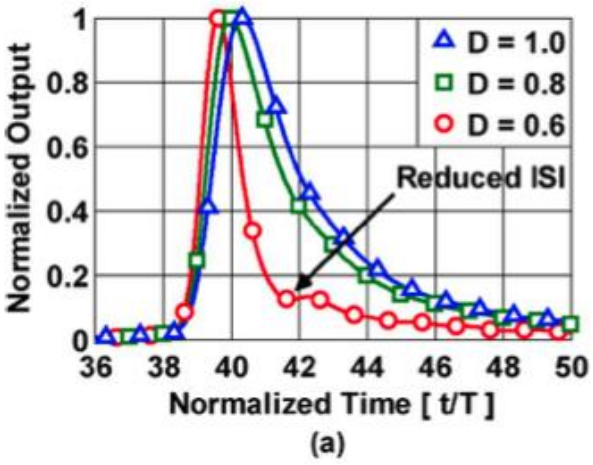

Figure 2 Normalized impulse response of a channel to PWM pulses for different duty cycles [2]

Fully Digital Segmented Transmit Equalizer with Dynamic Impedance Modulation

This architecture [4] [5] involves having multiple segments for the TX driver, depending on the resolution we want to achieve. These segments are connected in parallel and to the same input of the channel. The equalization taps inputs (pre/post cursor) are connected to a few numbers of these segments, which is decided by the tap weight and the majority drivers have their input as the main cursor. For the post cursor the polarity is opposite (depending on the sign of the weight). For de-emphasis, when these drivers driven by pre and post cursor turn on, they steal some of the current that would flow through the channel, effectively shunting the main driver and reducing the swing. For alternating bit pattern (Nyquist frequency), these equalization tap drivers emphasize the swing and improve the channel response by emulating a high-pass filter.

This is the topology we are going to focus on this report, and there will be detailed description in the next chapter.

Voltage-Mode Transmitter with Analog Impedance Modulation

The impedance modulated voltage-mode transmitter [6] is a non-segmented implementation which has controlled impedances in series with the driver transistors. The control input for these impedances is the pre or post cursor tap input.

For the transmitter output swing during transition to be maximum, the blue path is on (Fig 3.). A global impedance control circuit controls the gates VzmeqUP/DN and VZceqUP/DN.

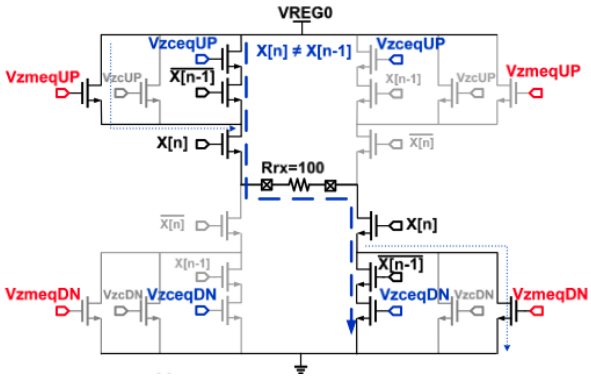

Figure 3 Maximum transmitter output swing during a transition bit [6]

For a >1 run length, the red path is on to provide de-emphasis, as show in Fig. 4.

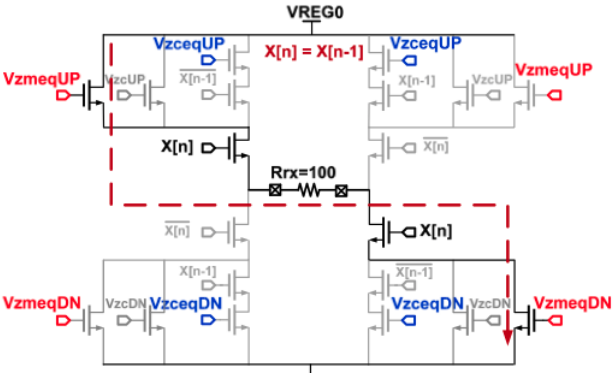

Figure 4 De-emphasis transmitter output swing for run length>1 [6]

Table 2 Transmitter Performance Comparison

Specification	**[1]**	**[2]**	**[4]**	**[6]**
Technology	90nm CMOS	90nm	90nm CMOS	65nm
Data rate	2-6Gb/s	5Gb/s	4Gb/s	8Gb/s
Supply Voltage	0.8 – 1.2 V	1 – 1.25 V	1.15 V	0.5 – 0.75 V
TX swing	100-400mVppd	400mV	400mV	100-300mV
Equalization	2-tap FIR	PWM (VM)	4-tap FIR	2-tap FIR
Eye-height	146mV	78mV	128mV	55mV
Timing Margin	150ps	0.3UI	113ps	45ps
Energy/Power Efficiency	1.26pJ/bit @6Gb/s	3.1mW/Gbps	2pJ/bit @4Gb/s	1.05pJ/bit

CHAPTER III

ARCHITECTURE

A SEGMENTED HIGH-SWING VOLTAGE-MODE TRANSMITTER WITH DYNAMIC DIGITAL IMPEDANCE MODULATION

Introduction

As discussed in the literature review, the segmented driver approach is a good architecture to implement a moderate resolution with transmitter. Although it is more complex than the hybrid architecture, it is better in terms of power efficiency as the taps in hybrid still have a static power dissipation. The segmented approach is not very susceptible to process variations like analog impedance control transmitter or the PWM approach.

In the initial simulation results, we concluded that the loss for T20 channel cannot be compensated through 3-tap FIR with a low swing (<400mVppd). Hence as an improvement on our initial proposed solution, we have chosen the **High-Swing Voltage Mode Driver** as our transmitter segments.

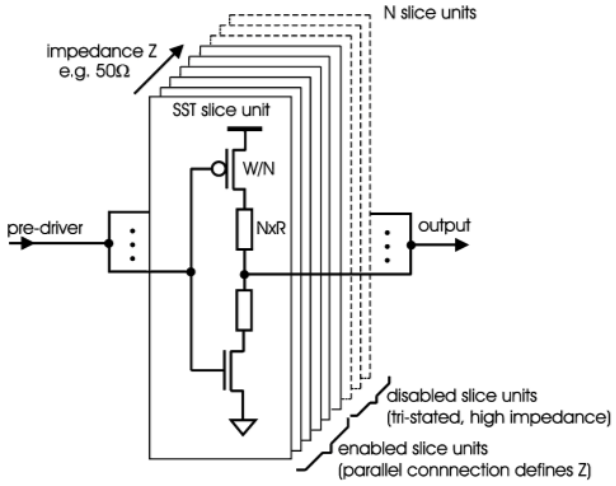

Figure 5 High-swing voltage mode driver [9]

The High -Swing Voltage-Mode Transmitter Segment

For the main transmitter, we are using a high-swing driver. The main reason for this choice is the channel loss for C4 and T20 channels being more than 20dB. We also considered the shortcomings of a high swing topology such as output impedance variance due to process changes and additional reflections. It was verified in ADS simulations that a swing of 900mV was enough to meet the eye height specification for the lossy T20 channel.

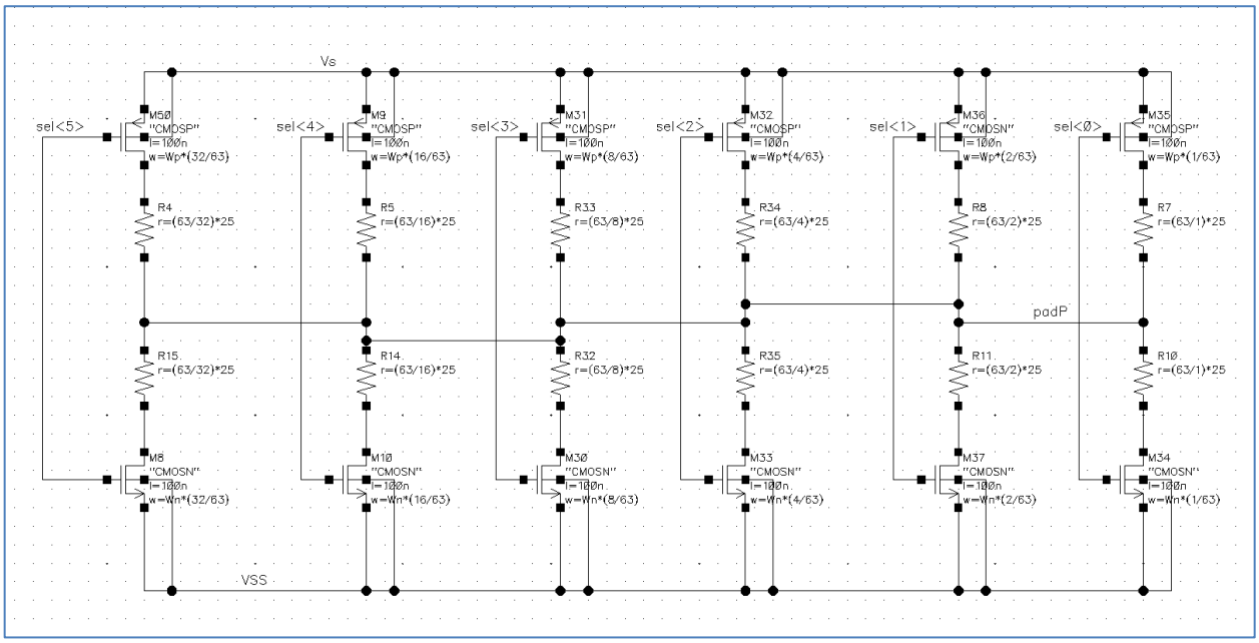

Figure 6 High-Swing Voltage-Mode Driver segments (Only 1 of the 2 shown)

The segment size of each NMOS/PMOS device of the i^{th} segment is given by $W*(2^i/32)$ to realize a resistance of $(32/2^i)*25$ Ohms. These segments are weighted to achieve the de-emphasis based on the equalization codes. Similarly, the resistances are also weighted the same way, 50% resistance component from MOS and other 50% from resistor. Wp & Wn are the sizes of the PMOS, NMOS from the replica bias.

Table 3 Transistor sizes

Size	Value
Wp	145µ/0.1µ
Wn	50µ/0.1µ

Table 4 Resistance value of each segment

P/NMOS Transistors	Sizes	Resistance Realized (ohms)
Replica Bias MOS	W(p/n)/L	25
Segment_0	(W(p/n)/L) *(1/63)	25*63 = 1575
Segment_0	(W(p/n)/L) *(1/63) *(2)	25*63*0.5 = 787.5
Segment_2	(W(p/n)/L) *(1/63) * (4)	25*63*0.25=393.75
Segment_3	(W(p/n)/L) *(1/63) * (8)	25*63*0.125=196.875
Segment_4	(W(p/n)/L) *(1/63) * (16)	25*63*0.0625=98.4375
Segment_5	(W(p/n)/L) *(1/63) * (32)	25*63*0.03125=49.21875

Equalization & Segment Select Logic

For a run length >1, the pre/post curser driver transistors turn on in the polarity opposite to main cursor. This implements a de-emphasis through a GND shunting path which can help in realizing multiple different voltages required by the FIR filter while maintaining constant 50 Ohms impedance (Fig. 6.).

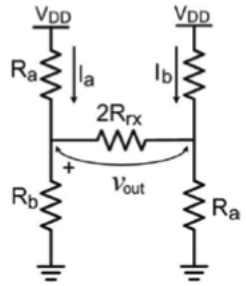

Figure 7 De-emphasis through GND shunting for run length >1 [5]

For this design, we have chosen to implement 3-tap FIR equalization (1 pre, 1 main and 1 post cursor or 1-main, 2-post) with a 6-bit resolution. In the preliminary report, we have presented our ADS system simulation results with B1, C4 and T20 channels and we concluded that we meet the eye-height specification for the B1 and C4 channels at 10Gb/s.

The segments of the voltage-mode transistor are driven by the main or the pre/post cursor taps. This setting is maintained by a pre-driver logic which selects which segment belong to which cursor or tap. This is a configurable setting and comprises of digital-to-analog converter (DAC) [7].

For our design, we chose a look-up table-based (LUT) approach which will allow equalization. We have implemented Verilog-A models to for the LUT and the pre-driver segment selection logic. The Verilog-A code can be found in the Appendix.

Table 5 6-bit resolution tap calculation for B1 channel @10Gb/s

	B1-channel		
	Pre-cursor Tap	*Main-cursor Tap*	*Post-cursor Tap*
Tap values	-0.0476	0.7143	-0.2063
Tap values for 6-bit resolution (multiplied by $2^6 - 1$)	(-) 3	45	(-) 15
Binary code	000011	101101	001111

Table 6 6-bit resolution tap calculation for C4 channel @10Gb/s

	C4-channel		
	Main-cursor Tap	*Post-cursor 1 Tap*	*Post-cursor 2 Tap*
Tap values	0.6349	-0.3492	+0.0159
Tap values for 6-bit resolution (multiplied by $2^6 - 1$)	40	(-) 22	(+) 1
Binary code	101000	010110	000001

Table 7 6-bit resolution tap calculation for T20 channel @10Gb/s

	T20-channel		
	Pre-cursor Tap	*Main-cursor Tap*	*Post-cursor Tap*
Tap values	-0.1905	0.5714	-0.2381
Tap values for 6-bit resolution (multiplied by $2^6 - 1$)	(-) 12	36	(-) 15
Binary code	001100	100100	001111

Table 8 B1 channel equalization lookup table @10Gb/s

Pre	***Main***	***Post***	***A5***	***A4***	***A3***	***A2***	***A1***	***A0***

0	***0***	***0***	*0*	*1*	*0*	*0*	*1*	*0*
0	***0***	***1***	*0*	*0*	*0*	*0*	*1*	*1*
0	***1***	***0***	*1*	*1*	*1*	*1*	*1*	*1*
0	***1***	***1***	*1*	*1*	*0*	*0*	*0*	*0*
1	***0***	***0***	*0*	*0*	*1*	*1*	*1*	*1*
1	***0***	***1***	*0*	*0*	*0*	*0*	*0*	*0*
1	***1***	***0***	*1*	*1*	*1*	*1*	*0*	*0*
1	***1***	***1***	*1*	*0*	*1*	*1*	*0*	*1*

Table 9 C4 channel equalization lookup table @10Gb/s

Main	***Post-1***	***Post-2***	***A5***	***A4***	***A3***	***A2***	***A1***	***A0***
0	***0***	***0***	*0*	*1*	*0*	*1*	*1*	*0*
0	***0***	***1***	*0*	*1*	*0*	*1*	*1*	*1*
0	***1***	***0***	*0*	*0*	*0*	*0*	*0*	*1*
0	***1***	***1***	*0*	*0*	*0*	*0*	*0*	*0*
1	***0***	***0***	*1*	*1*	*1*	*1*	*1*	*1*
1	***0***	***1***	*1*	*1*	*1*	*1*	*1*	*0*
1	***1***	***0***	*1*	*0*	*1*	*0*	*0*	*0*
1	***1***	***1***	*1*	*0*	*1*	*0*	*0*	*1*

Table 10 T20 channel equalization lookup table @10Gb/s

Pre	***Main***	***Post***	***A5***	***A4***	***A3***	***A2***	***A1***	***A0***
0	***0***	***0***	*0*	*1*	*1*	*0*	*1*	*1*
0	***0***	***1***	*0*	*0*	*1*	*1*	*0*	*0*
0	***1***	***0***	*1*	*1*	*1*	*1*	*1*	*1*
0	***1***	***1***	*1*	*1*	*0*	*0*	*0*	*0*
1	***0***	***0***	*0*	*0*	*1*	*1*	*1*	*1*
1	***0***	***1***	*0*	*0*	*0*	*0*	*0*	*0*
1	***1***	***0***	*1*	*1*	*0*	*0*	*1*	*1*
1	***1***	***1***	*1*	*0*	*0*	*1*	*0*	*0*

The weights A0-A5 were obtained by multiplying the tap weight by $2^6 - 1$ according to the bit resolution. In the *blue* section, in the above tables describe maximum de-emphasis happens when the main cursor is of the same sign as the pre or the post cursors. In orange rows, the maximum frequency transition (Nyquist) bit combinations are mentioned, and all 6-bit resolution tap weights are of the same sign as main cursor, basically putting all the weight on main cursor for maximum transition. For run lengths greater than 1, weights are added to the pre/post taps based on the

combination for de-emphasis. The results prove that these equalization tables work very well for the channels.

Global Impedance Control

The circuits to generate the supply voltages for pre-driver stage and the transmit driver are shown in the figure below. Voltage Vr adjusts the transmitter swing based on a reference voltage seen on the left in the figure below. Replica bias circuits are used to generate voltage Vs, which is the supply voltage of the transmitter.

The replica bias was modified for a high swing transmitter segment by replacing the NMOS from a PMOS and ensuring the resistance is 25 Ohms. This mean increasing the sizes of the driver transistors, which in turn means better pre-driver segments to drive a higher load capacitance.

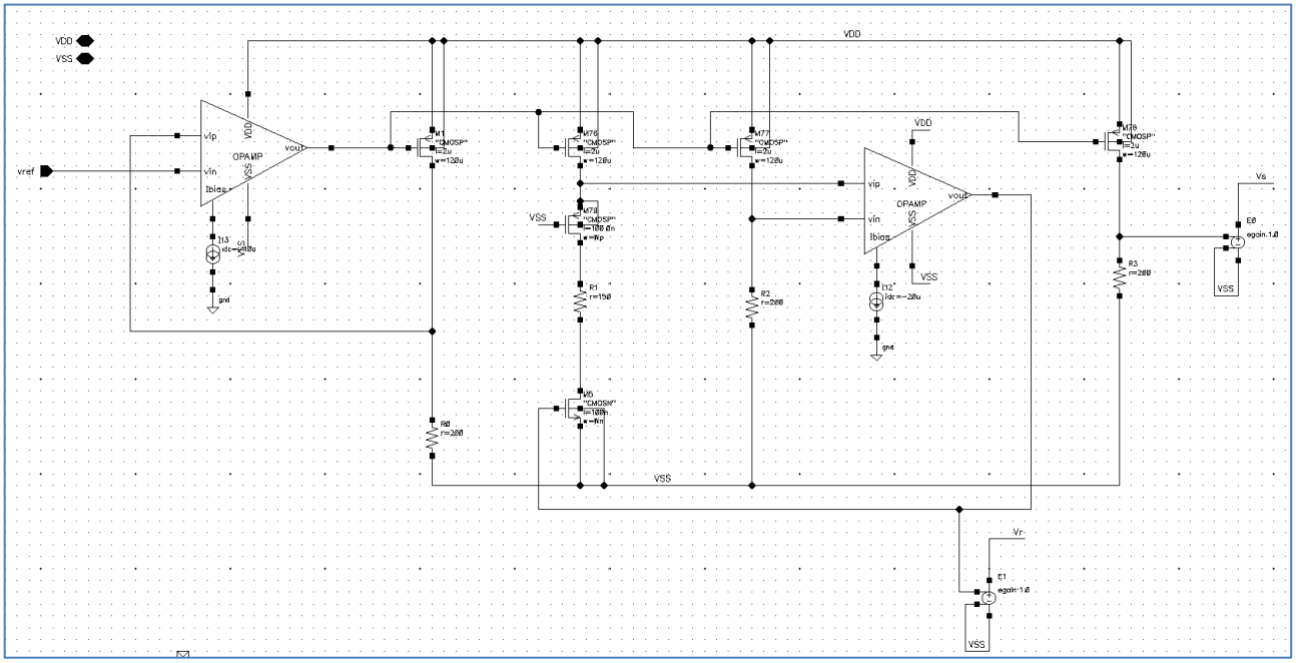

Figure 8 Global Impedance Control for the Transmitter Segments

Weighted Pre-driver Segments

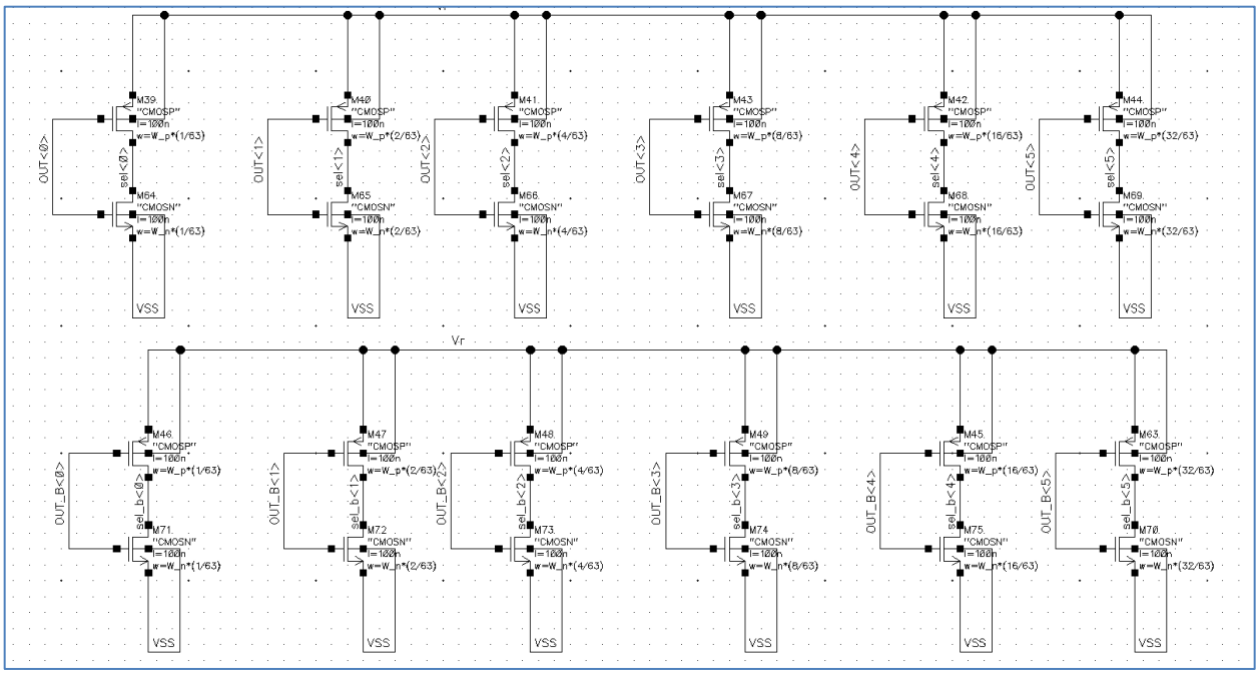

Figure 9 Weighted Pre-driver segments

Due to each high-swing transmitter segment being sized according to the binary weights, every pre-driver driving the signal from the pre-driver logic sees a different load capacitance. This induces a mismatch in the MOS resistor turn ON time, which can lead to reflections.

We have sized the pre-drivers in the same binary weighted fashion, to keep the rise/fall times of all 6 segment select logic outputs similar. In the results below, we can see this in our simulations.

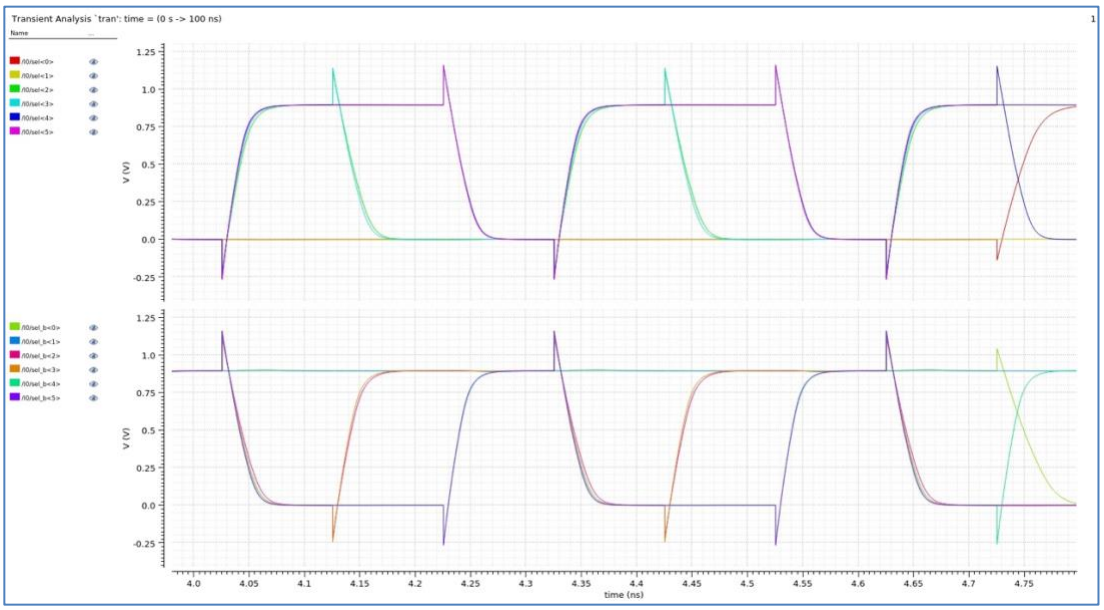

Figure 10 Pre-driver outputs

Complete Transmitter Schematic

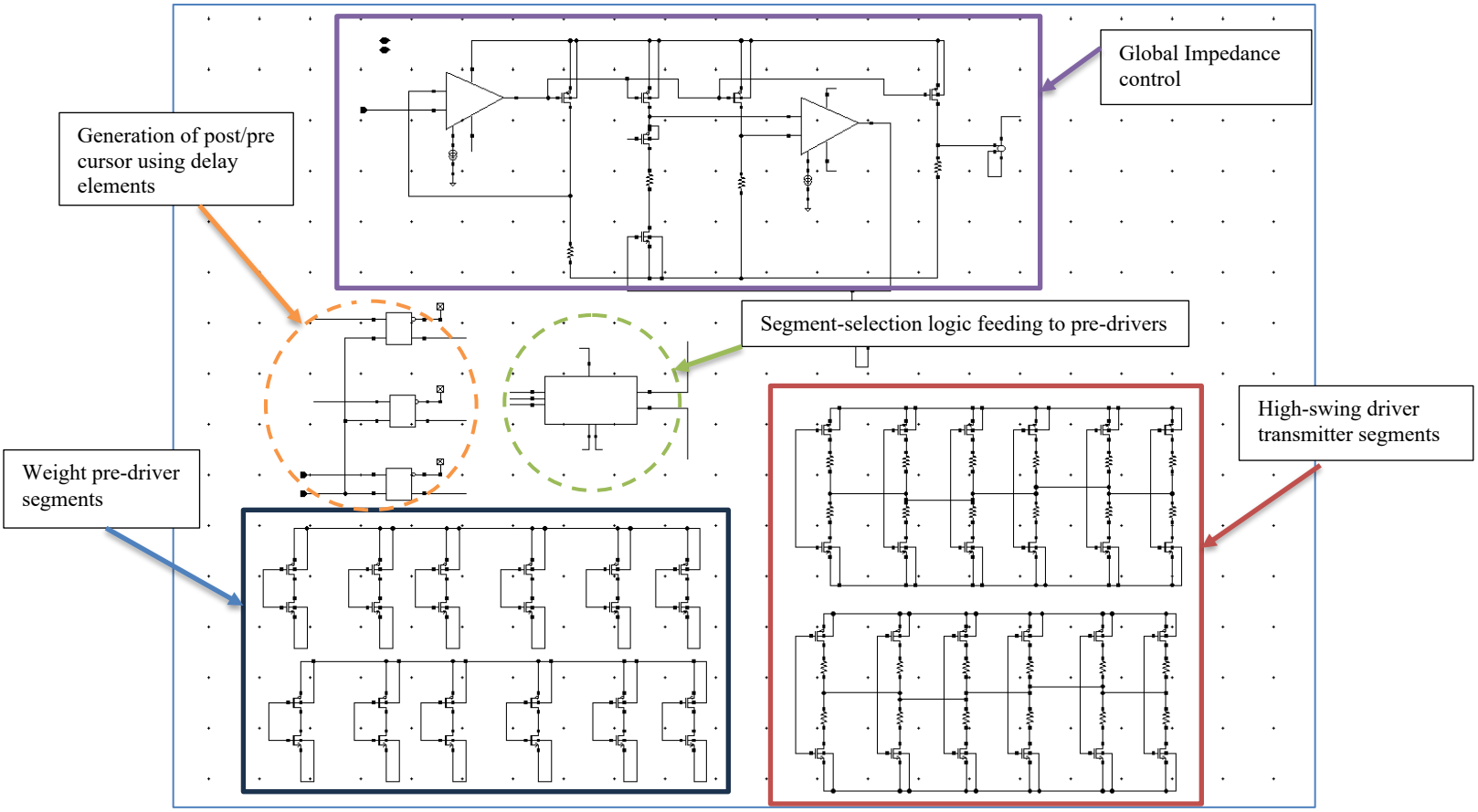

Figure 11 Complete High-Swing Transmitter schematic

Initial simulation results

Channel Frequency Response (MATLAB)

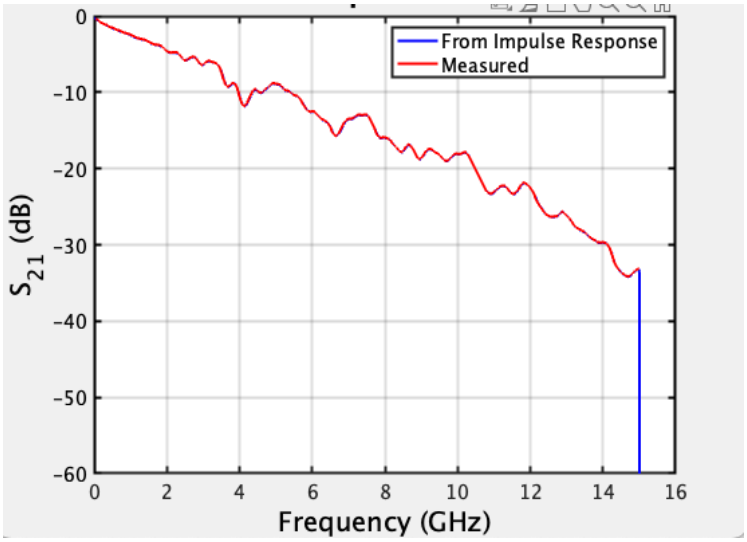

Figure 12 B1 channel

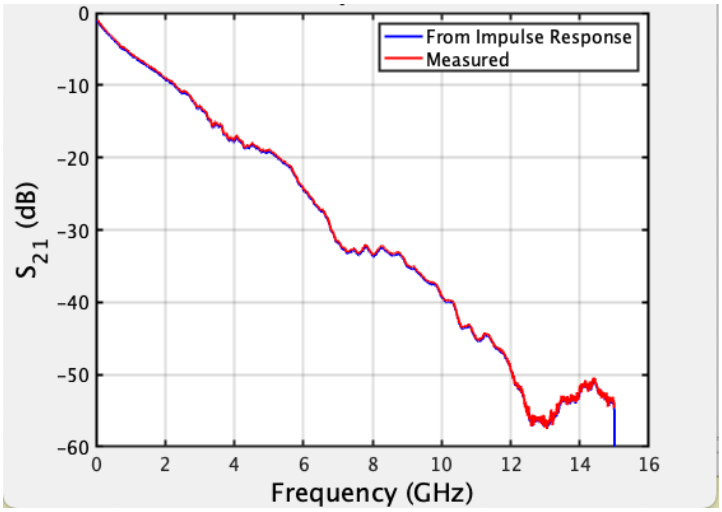

Figure 13 C4 channel

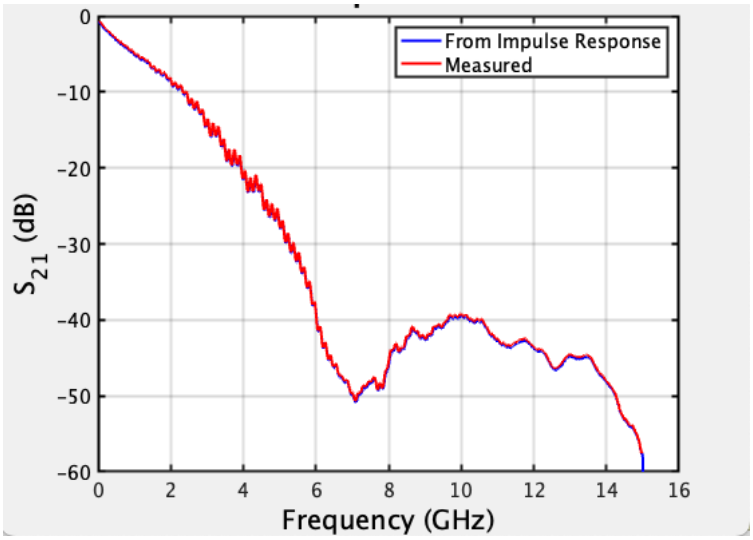

Figure 14 T20 channel

Table 11 Channel Loss at Nyquist = 5GHz

Channel name	Channel loss at Nyquist frequency
B1	8.87 dB
C4	19.15 dB
T20	27.6 dB

CHAPTER IV

SIMULATION RESULTS

Overview

We present the following simulation results as a proof of our work:

1. Eye Diagram plots at RX for equalized and unequalized channel response at 10Gb/s
2. Bathtub plots to measure timing margin at a BER of 1e-12
3. Power consumption of the transmitter for the three channels.
4. Simulation results showing the maximum data rate achievable for a receiver sensitivity of 20 mVppd.

Testbench for Simulations

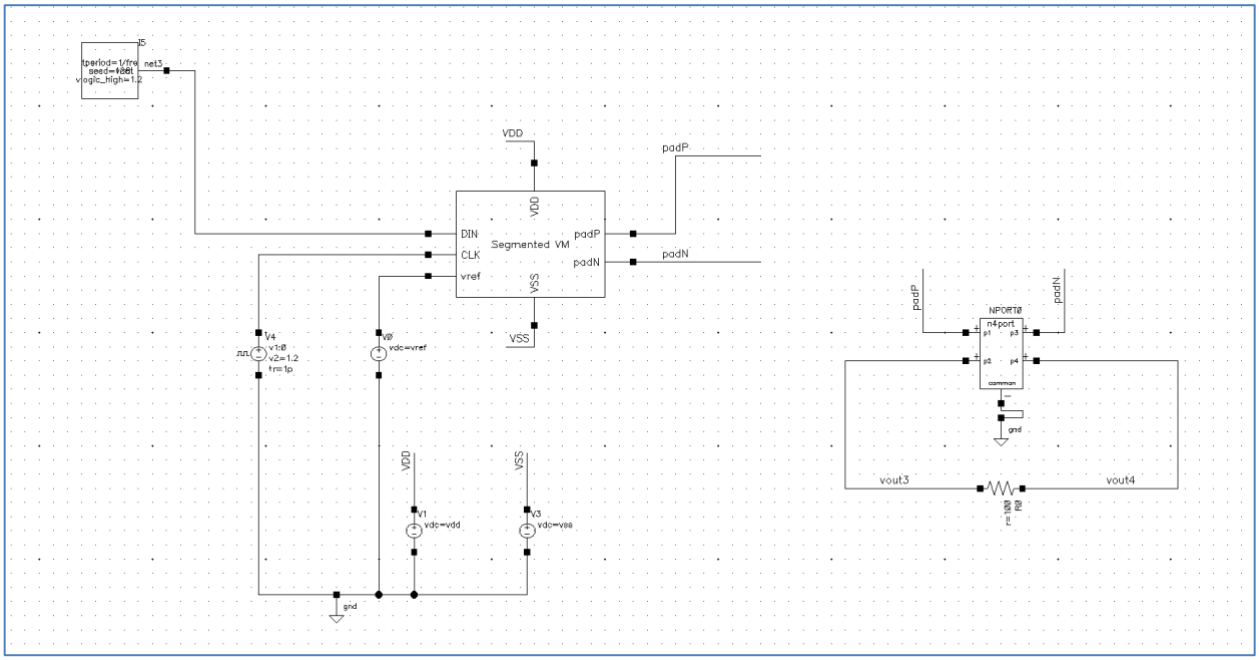

Figure 15 Testbench for simulation for the three channels

Eye Diagram at 10Gb/s

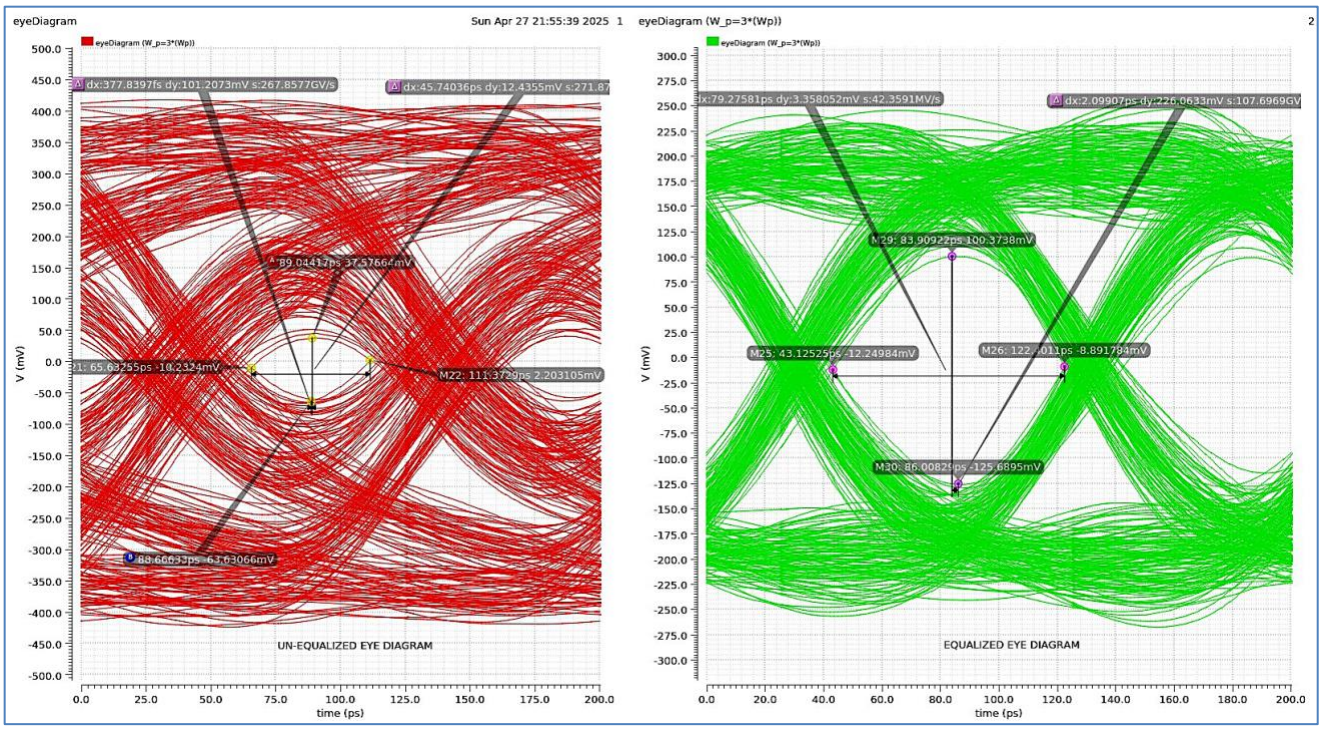

Figure 16 Unequalized (in red) and Equalized (in green) eye heights for B1 channel@10Gb/s

Table 12 B1 channel - Parameters

Parameter	**Unequalized**	**Equalized**
Data-rate	10 Gb/s	
Channel-loss	8.87dB @ 5GHz	
Eye-height	101.2mV	226.06mV
Eye-width	45.74ps	79.28ps

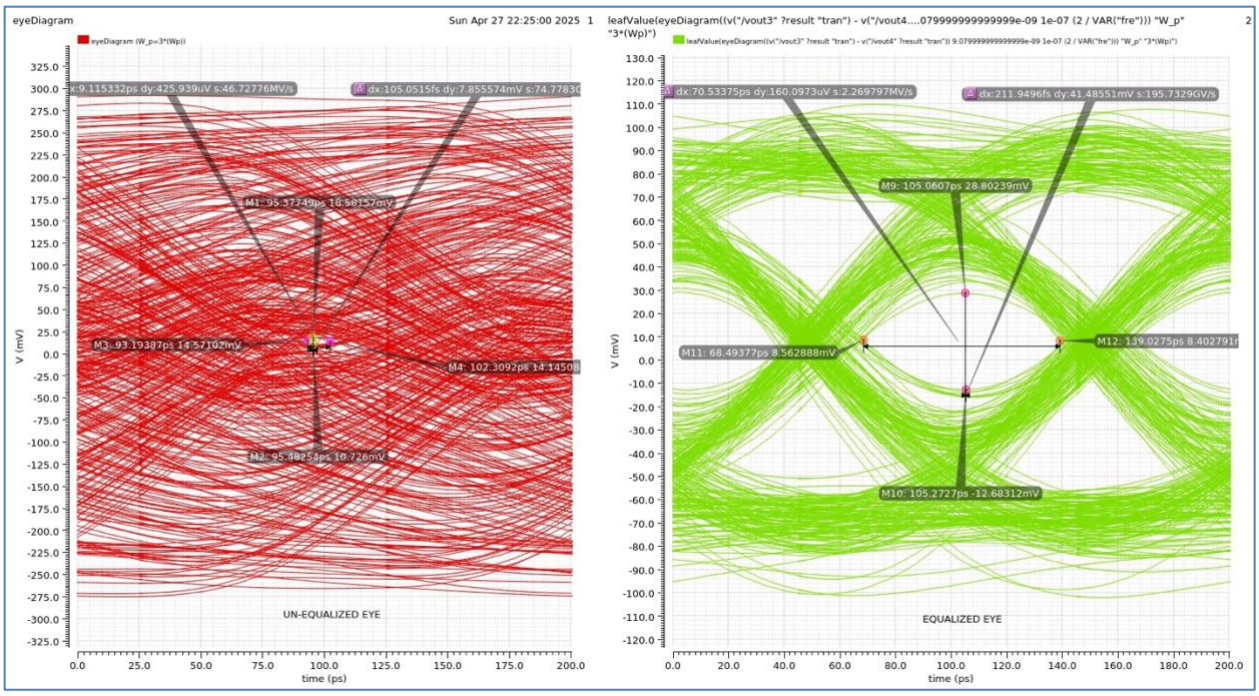

Figure 17 Unequalized (in red) and Equalized (in green) eye heights for C4 channel@10Gb/s

Table 13 C4 channel - Parameters

Parameter	Unequalized	Equalized
Data-rate	10 Gb/s	
Channel-loss	19.15dB @ 5GHz	
Eye-height	7.8mV	41.48mV
Eye-width	9.16ps	70.53ps

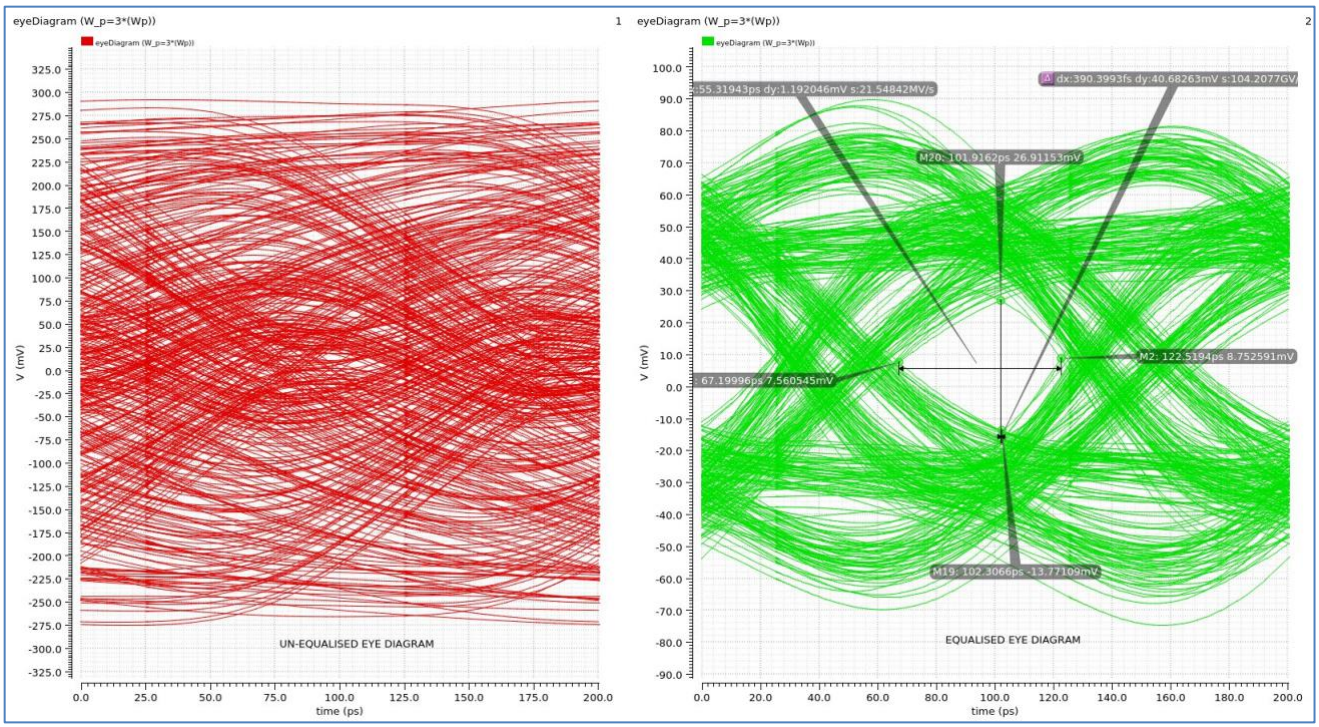

Figure 18 Unequalized (in red) and Equalized (in green) eye heights for T20 channel@10Gb/s

Table 14 T20 channel - Parameters

Parameter	Unequalized	Equalized
Data-rate	10 Gb/s	
Channel-loss	27.6dB @ 5GHz	
Eye-height	Eye not open	40.68mV
Eye-width	Eye not open	55.32ps

Bathtub plots at 10Gb/s to measure timing margin at a BER of 1e-12

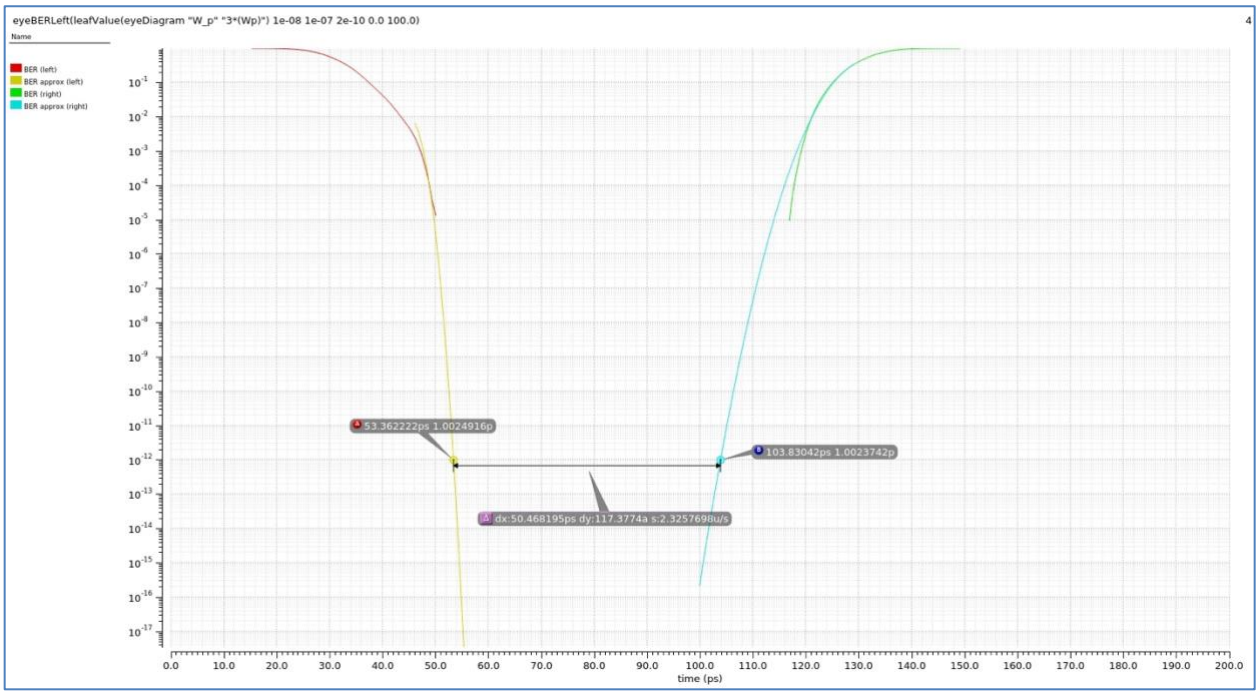

Figure 19 B1 channel: Timing margin @BER=1e-12 = 0.505UI

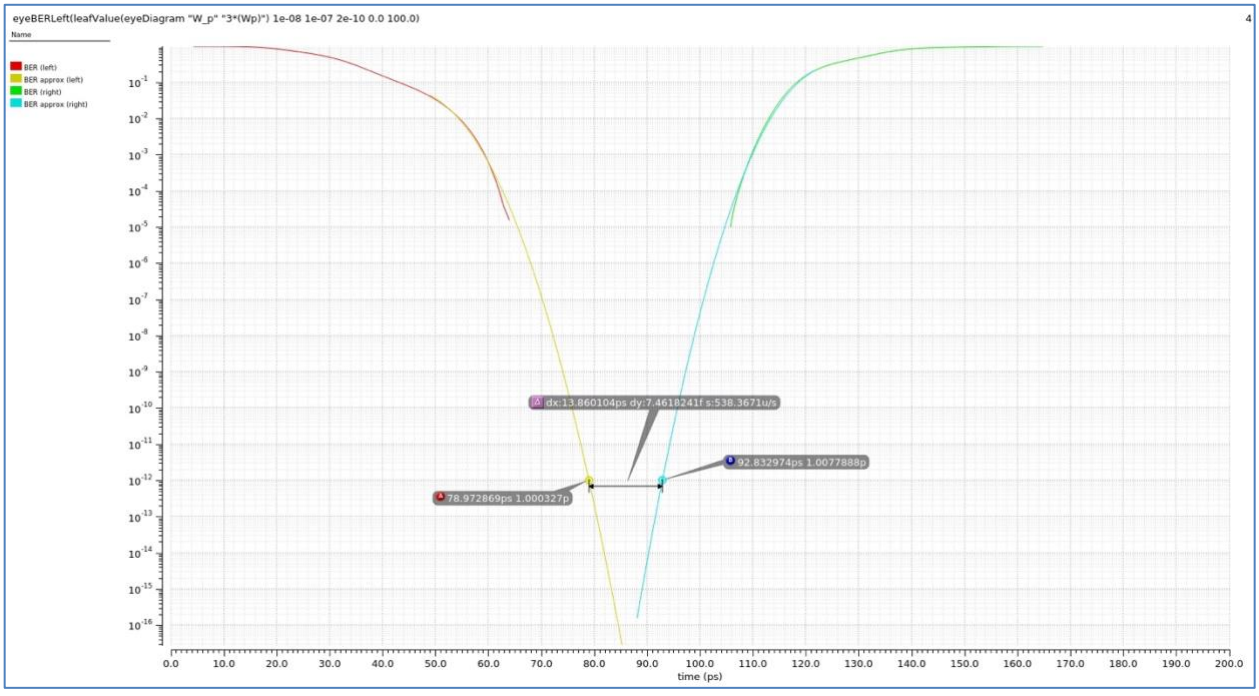

Figure 20 C4 channel: Timing margin @BER=1e-12 = 0.14UI

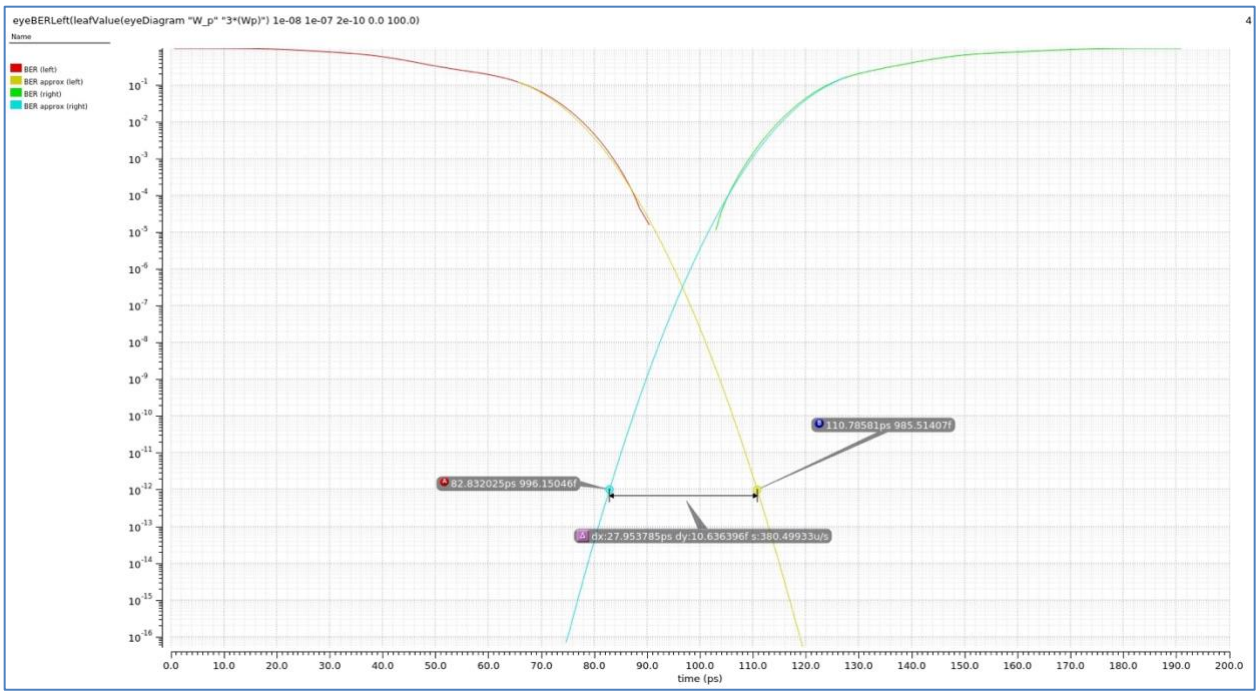

Figure 21 T20 channel: Timing margin @BER=1e-12 = -0.28UI

Table 15 Summary of equalized eye height and widths for the three channels

Parameter	**B1 channel**	**C4 channel**	**T20 channel**
Equalized eye height	226.06mV	41.48mV	40.68mV
Equalized eye width	79.28ps	70.53ps	55.32ps

Power consumption

Average Power Consumption (similar for all channels)	**23.34 mW**

Maximum data-rate achievable for RX sensitivity=20mVppd & timing margin=0.3UI at BER=1e-12

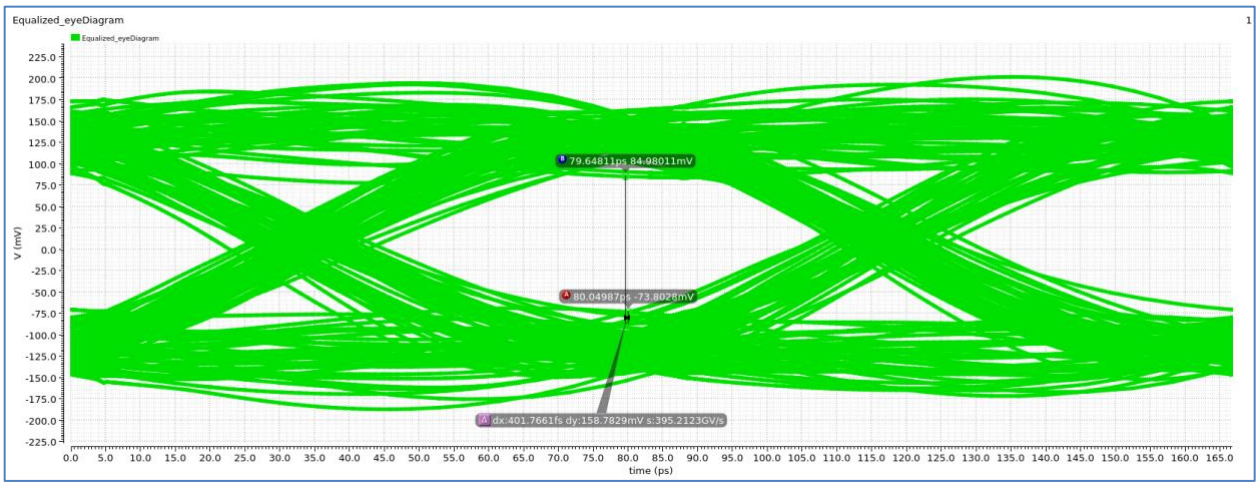

Figure 22 Eye diagram for B1 channel @12Gb/s, RX sensitivity = 158.79 mVppd

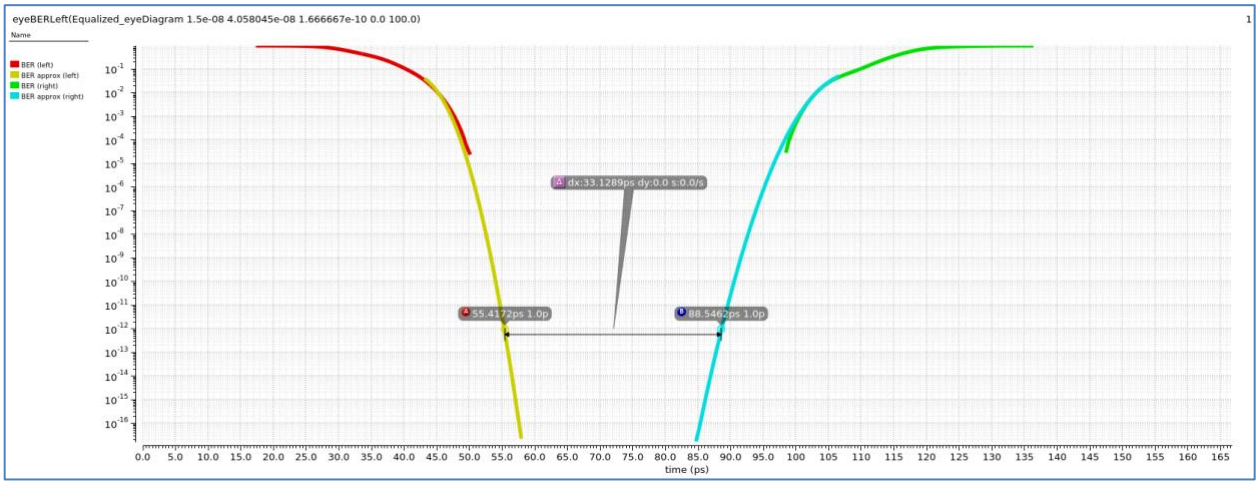

Figure 23 B1 channel Bathtub curve @12Gb/s timing margin = 33.13ps

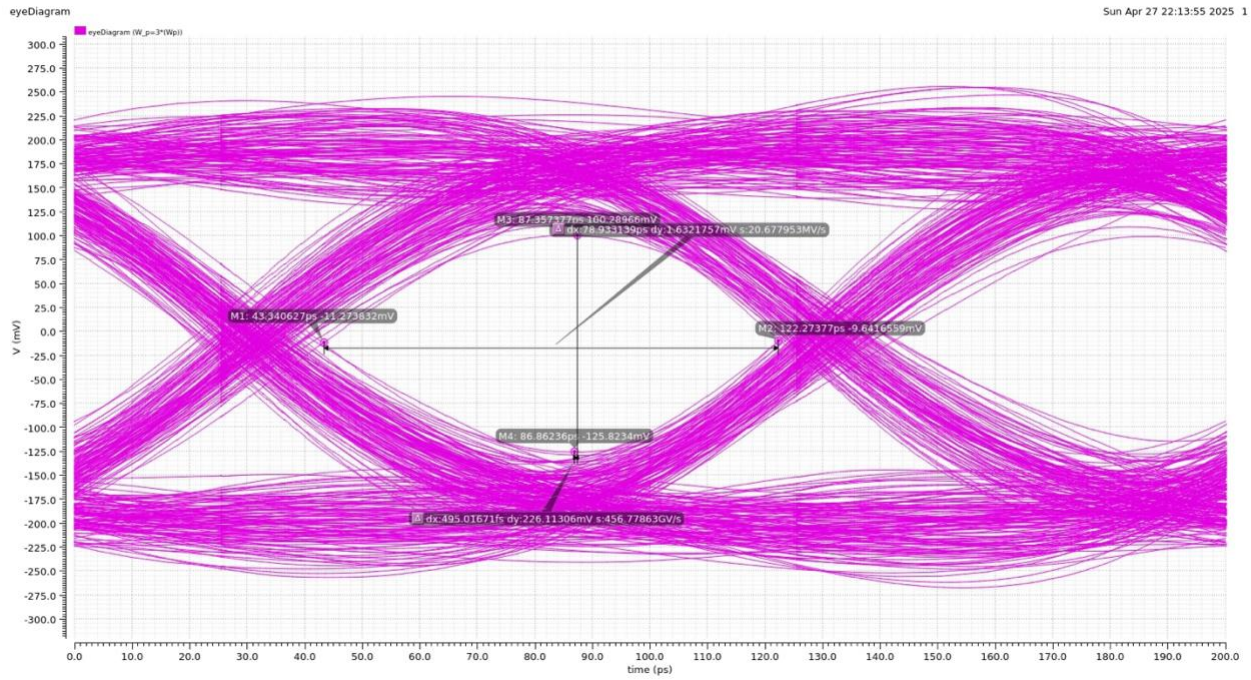

Figure 24 Eye diagram for C4 channel @8Gb/s, RX sensitivity = 226.11 mVppd

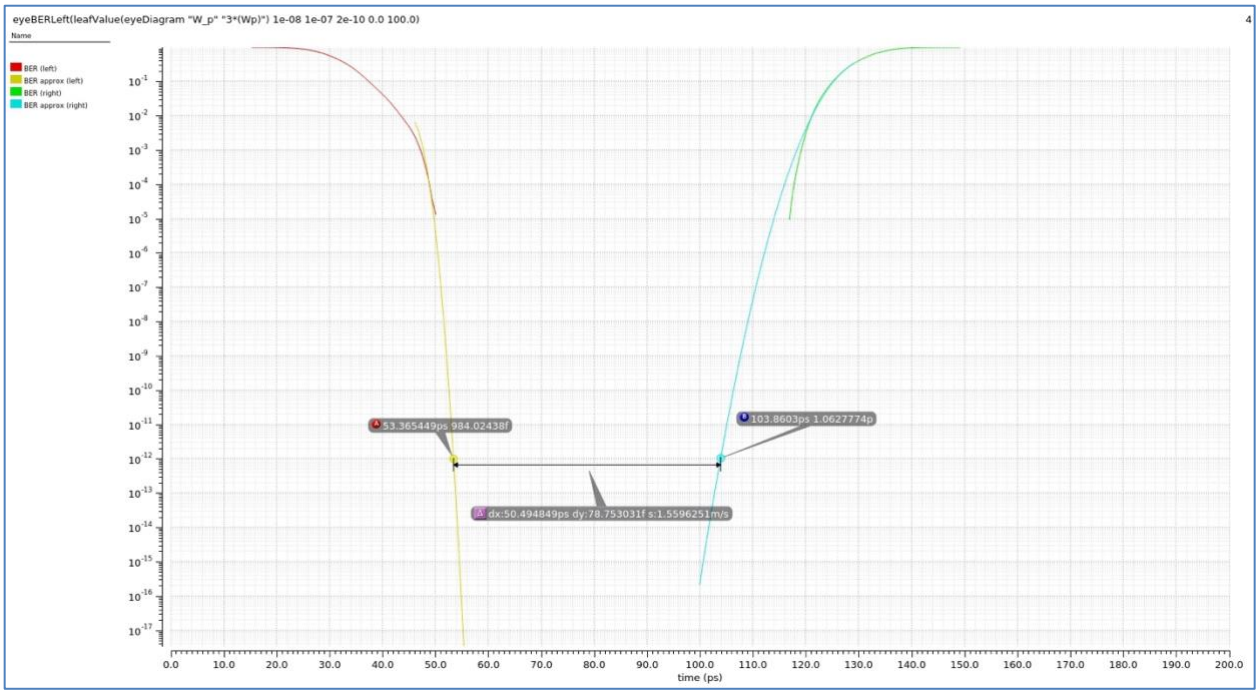

Figure 25 C4 channel Bathtub curve @8Gb/s timing margin = 50.5ps

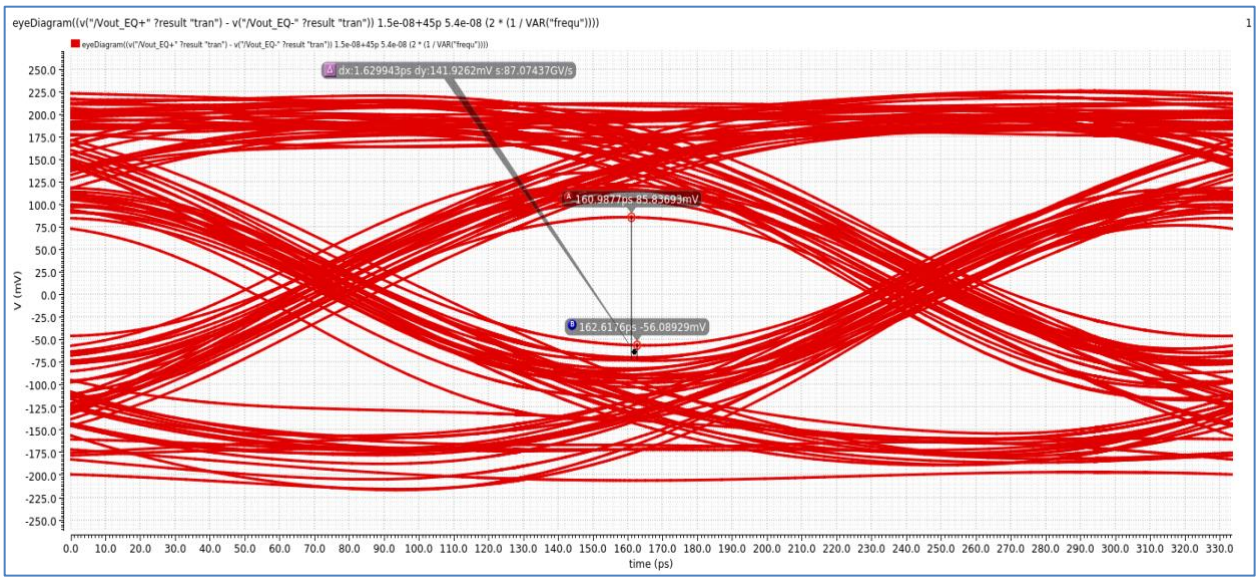

Figure 26 Eye diagram for T20 channel @8Gb/s, RX sensitivity = 141.9 mVppd

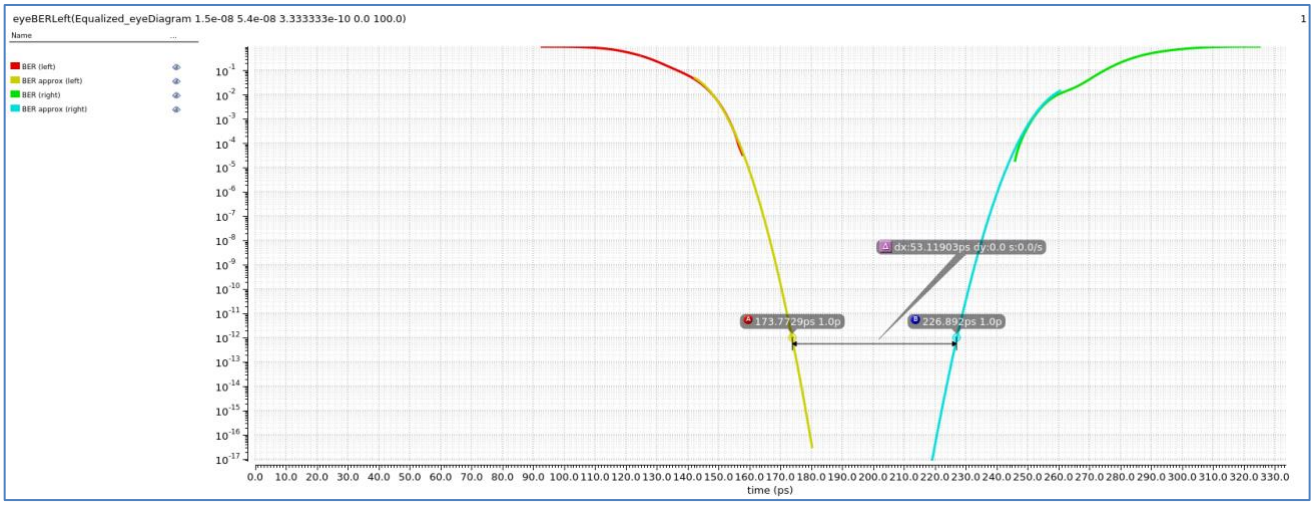

Figure 27 T20 channel Bathtub curve @8Gb/s timing margin = 53.11ps

Table 16 Max data rate, timing margin and RX sensitivity at BER=1e-12 for the three channels

Channel	**Max data rate**	**RX sensitivity @BER=1e-12**	**Timing margin @BER=1e-12**
B1	12Gb/s	158 mVppd	0.396 UI

C4	8Gb/s	226 mVppd	0.404 UI
T20	6Gb/s	141.9 mVppd	0.318 UI

Comparison with current references

Table 17 Comparison of results for B1 channel with other low loss channel

Parameter	This Work B1 Channel	[5]	[10]
Data Rate	10Gb/s	4Gb/s	7.4Gb/s
Technology	90nm	90nm	45nm
TX Swing (at 10Gbps)	900mVppd	1Vppd	800mVppd
Supply Voltage	1.2 V	1.15V	1.08V & 0.93V
Channel Loss @Nyquist Frequency	8.87dB	10dB	-
No. of FIR Taps	3	2	2
Eye Height	226 mVppd	107 mVppd	-
Power Consumption	23.344 mW	8mW	32mW
Energy Efficiency	2.3 pJ/bit	2pJ/bit	4.32pJ/b
Max Data Rate (for RX sensitivity=20mV and timing margin>0.3UI at BER=1e-12)	12 Gb/s	-	-

Parameter	This Work:C4 Channel	This Work: T20 Channel	[6]
Data Rate	10Gb/s	10Gb/s	16Gb/s
Technology	90nm	90nm	65nm
TX Swing (at 10Gbps)	900mVppd	900mVppd	100mV-300mVppd
Supply Voltage	1.2 V	1.2	1V
Channel Loss @Nyquist Frequency	19.15 dB	27.6 dB	15.5 dB
No. of FIR Taps	3	2-Tap FIR	2-Tap FIR
Eye Height	41.48mVppd	40.68mVppd	55mV ppd
Eye Width	70.53 ps	55.32 ps	33.4ps
Power Consumption	23.34 mW	23.34 mW	16.8mW
Energy Efficiency	2.3pJ/bit	2.3pJ/bit	1.05pJ/b
Max Data Rate (for RX sensitivity=20mV and timing margin>0.3UI at BER=1e-12)	8Gb/s	6Gb/s	-

Conclusions & Learnings

1. From our results, we can conclude that TX FIR 3-tap resolution is a good equalization technique for channels with losses up to 15 dB
2. As seen in channels C4 and T20 with losses 20dB and beyond, more equalization, either at the receive side, or more taps at the input might be needed to achieve a good bit error rate at data rates of 10Gb/s.
3. The high swing transmitter is a very good option for a driver as it displayed significantly better results than a low-swing variant, which we tried to test in our preliminary report. It can be used to implement a PAM-4 modulation.
4. We understand that the shortcomings of high-swing driver will be seen in the form of reflections in PVT simulations.
5. To get the maximum achievable data rate for a BER=1e-12 and RX sensitivity > 20mVppd, we had to resort to lower data rates for the C4 and T20 channel. This meant that we had to modify the equalization taps for the newer data rates, which then gave us good results.
6. We concluded that equalization taps are also data rate dependent because we aim to equalize for the channel loss at Nyquist. If we go to a different data rate, the Nyquist frequency changes as well, hence the loss that we need to equalize for, also changes.
7. Using weighted drivers helped us improve the eye heights by reducing reflections.
8. Overall we were able to successfully equalize the high swing transmitter to remove the ISI for a good BER for all the three (B1, C4 & T20) channels.

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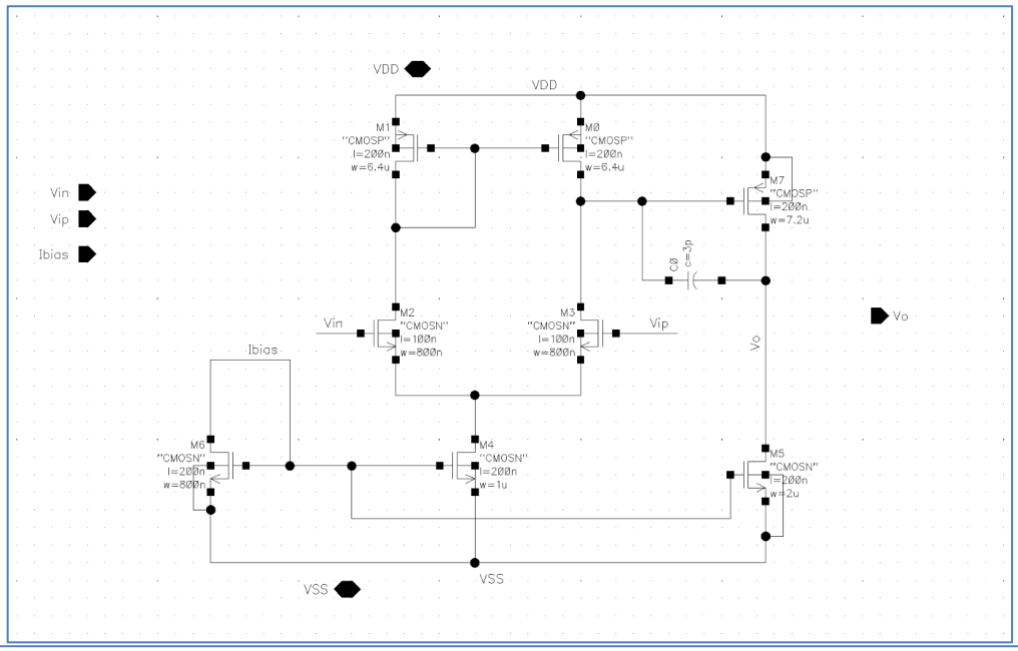
APPENDIX

- Verilog-A code for segmentation selection logic

```
// VerilogA for project_720, segment_select, veriloga

`include "constants.vams"
`include "disciplines.vams"
// B1 channel
// equalization: pre || main || post
module segment_select_B1(CLK, sig_main, sig_cur1, sig_cur2, OUT, OUT_B, VDD, VSS);

input CLK, sig_main, sig_cur1, sig_cur2;
output [5:0] OUT;
output [5:0] OUT_B;
inout VDD, VSS;

electrical CLK, sig_main, sig_cur1, sig_cur2, VDD, VSS;
electrical [5:0] OUT;
electrical [5:0] OUT_B;


parameter clk_thresh = 0.5;
parameter data_thresh = 0.5;
parameter td = 1f;
parameter tr = 1f;

integer data_bits[2:0];
integer out_sel[5:0];

analog begin

    @(cross(V(CLK) - clk_thresh, +1)) begin

        data_bits[1] = V(sig_main, VSS) > data_thresh ? 1 : 0; // main cursor
        data_bits[0] = V(sig_cur1, VSS) > data_thresh ? 1 : 0; // cursor 1 (pre, or post 2)
        data_bits[2] = V(sig_cur2, VSS) > data_thresh ? 1 : 0; // cursor 2 (post 1)


if (data_bits[0] == 0 && data_bits[1]==0 && data_bits[2]==0) begin // 000

    $display("flag 000");
        out_sel[5] = 0;
        out_sel[4] = 1;
        out_sel[3] = 0;
        out_sel[2] = 0;
        out_sel[1] = 1;
        out_sel[0] = 0; end
    else if (data_bits[0]==0 & data_bits[1]==0 & data_bits[2]==1) begin // 001
$display("flag 001");
        out_sel[5] = 0;
        out_sel[4] = 0;
        out_sel[3] = 0;
        out_sel[2] = 0;
        out_sel[1] = 1;
        out_sel[0] = 1; end
    else if (data_bits[0]==0 && data_bits[1]==1 && data_bits[2]==0) begin // 010
$display("flag 010");
        out_sel[5] = 1;
        out_sel[4] = 1;
        out_sel[3] = 1;
        out_sel[2] = 1;
        out_sel[1] = 1;
        out_sel[0] = 1; end
    else if (data_bits[0]==0 && data_bits[1]==1 && data_bits[2]==1) begin // 011
$display("flag 011");
        out_sel[5] = 1;
        out_sel[4] = 1;
        out_sel[3] = 0;
        out_sel[2] = 0;
        out_sel[1] = 1;
        out_sel[0] = 1; end
    else if (data_bits[0]==1 && data_bits[1]==1 && data_bits[2]==1) begin // 011
$display("flag 011");
        out_sel[5] = 1;
        out_sel[4] = 1;
        out_sel[3] = 0;
        out_sel[2] = 0;
        out_sel[1] = 1;
        out_sel[0] = 1; end
    else if (data_bits[0]==1 && data_bits[1]==0 && data_bits[2]==0) begin // 100
$display("flag 100");
        out_sel[5] = 0;
        out_sel[4] = 0;
        out_sel[3] = 1;
        out_sel[2] = 1;
        out_sel[1] = 1;
        out_sel[0] = 1; end
    else if (data_bits[0]==1 && data_bits[1]==0 && data_bits[2]==1) begin // 101
$display("flag 101");
        out_sel[5] = 0;
        out_sel[4] = 0;
        out_sel[3] = 0;
        out_sel[2] = 0;
        out_sel[1] = 0;
        out_sel[0] = 0; end
    else if (data_bits[0]==1 && data_bits[1]==1 && data_bits[2]==0) begin // 110
$display("flag 110");
        out_sel[5] = 1;
        out_sel[4] = 1;
        out_sel[3] = 1;
        out_sel[2] = 1;
        out_sel[1] = 0;
        out_sel[0] = 0; end
    else if (data_bits[0]==1 && data_bits[1]==1 && data_bits[2]==1) begin // 111
$display("flag 111");
        out_sel[5] = 1;
        out_sel[4] = 0;
        out_sel[3] = 1;
        out_sel[2] = 1;
        out_sel[1] = 0;
        out_sel[0] = 1; end


end

V(OUT[0], VSS) <+ V(VDD)*transition(out_sel[0], td, tr);
V(OUT[1], VSS) <+ V(VDD)*transition(out_sel[1], td, tr);
V(OUT[2], VSS) <+ V(VDD)*transition(out_sel[2], td, tr);
V(OUT[3], VSS) <+ V(VDD)*transition(out_sel[3], td, tr);
V(OUT[4], VSS) <+ V(VDD)*transition(out_sel[4], td, tr);
V(OUT[5], VSS) <+ V(VDD)*transition(out_sel[5], td, tr);

V(OUT_B[0], VSS) <+ V(VDD)*transition((1-out_sel[0]), td, tr);
V(OUT_B[1], VSS) <+ V(VDD)*transition((1-out_sel[1]), td, tr);
V(OUT_B[2], VSS) <+ V(VDD)*transition((1-out_sel[2]), td, tr);
V(OUT_B[3], VSS) <+ V(VDD)*transition((1-out_sel[3]), td, tr);
V(OUT_B[4], VSS) <+ V(VDD)*transition((1-out_sel[4]), td, tr);
V(OUT_B[5], VSS) <+ V(VDD)*transition((1-out_sel[5]), td, tr);

end


endmodule
```

- Miller Opamp used



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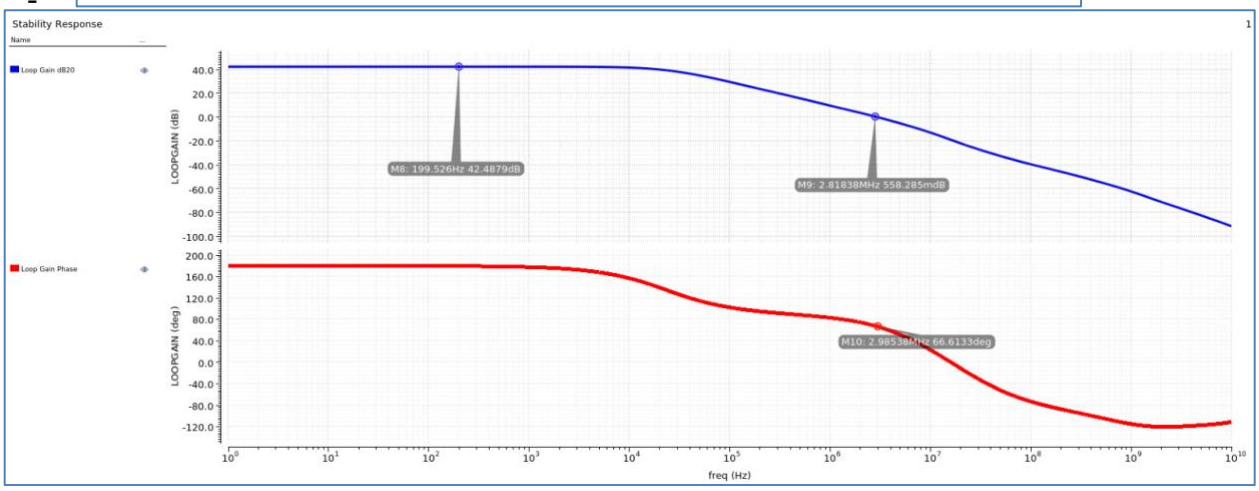

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- DC gain=42.487 dB , PM: 66 degrees