SUB 1V BG Design

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Reference Used : B. Razavi, "The Design of a Low-Voltage Bandgap Reference [The Analog Mind]," in *IEEE Solid-State Circuits Magazine*, vol. 13, no. 3, pp. 6-16, Summer 2021, doi: 10.1109/MSSC.2021.3088963. keywords: {Integrated circuits;Low voltage;Photonic band gap;Perturbation methods;Switches;Voltage control;Transient analysis;Operational amplifiers;Resistors;Low-pass filters},

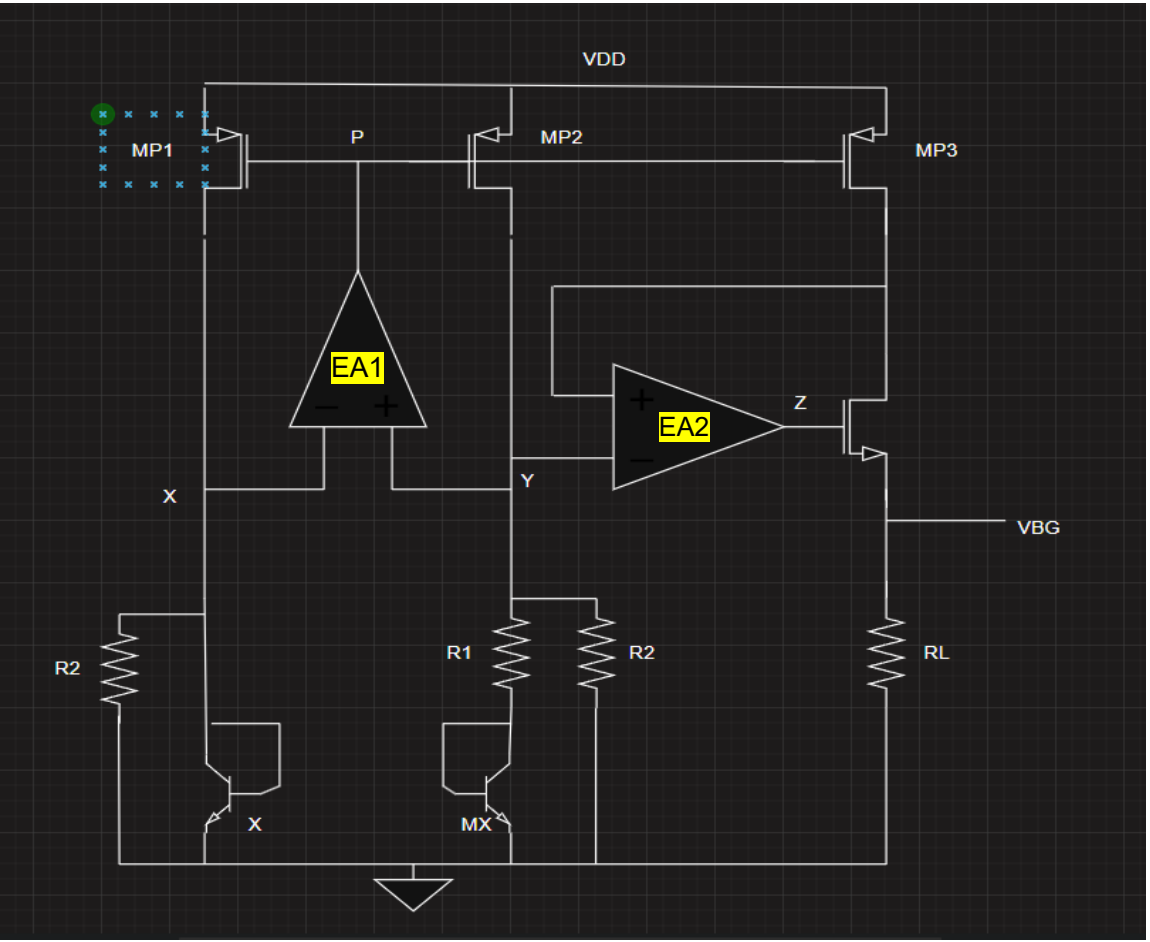
Contents :

1) SPEC Table
2) Topology Used
3) Basic Operation (First Hand Calculation)
4) DC Sims across PVT
5) Why Choose M=8?
6) Error Amp Design
7) PSRR calculations and Sims
8) -ve FB Loop in the Bandgap circuit
9) Startup Circuit, TRAN SIM (Slow and Fast Ramp Rate)
10) Final Spec Table

Target Specs

Output Voltage : 0.3 Volts
Output Voltage Variation < 1 % (0 ℃ to 100 ℃)
Sigma @ 27 < 5mV
Supply Rejection > 40 dB
Power Consumption < 1 mW
Supply Voltage : 1.2 Volts ± 5 % (1.14 to 1.26 Volts)

Topology Used



Note :
Startup circuit is included later in the schematics section

Both Error Amps have the same input common mode range but gain of EA2 was reduced to improve the stability of loop2.

Basic Operation

→ OPAMP Ensures Vx = Vy
⇒ Vbe1 = Vbe2 + I_R1*R1
⇒ I_R1 = Vt*ln(M)/R1

Now I_MP2 = I_MP1 (their W/L is same)
So I_MP = Vt*ln(M)/R1 + Vbe1/R2

Vbg = RL*(I_MP)

Vbg = RL/R1 *(Vt*ln(M) + (R1/R2)*Vbe1)

Now resistors are sized such that tempco is zero (just at 27 degree centigrade)

- We can't cancel the tempco at all the temperatures since the slope also changes with temperature but cancelling the tempco just at 27 would give good accuracy.

Vbg = RL/R1 * (PTAT + NTAT)

Slope (Vt*ln(M)) = (-1)*Slope(R1/R2 * Vbe1)
0.087*ln(M) = 1.702*(R1/R2)
→ Cancellation is done only at 27 ℃
→ Slope of Vbe is confirmed from the simulation (slide 6)

M=8
R1/R2 = 0.106

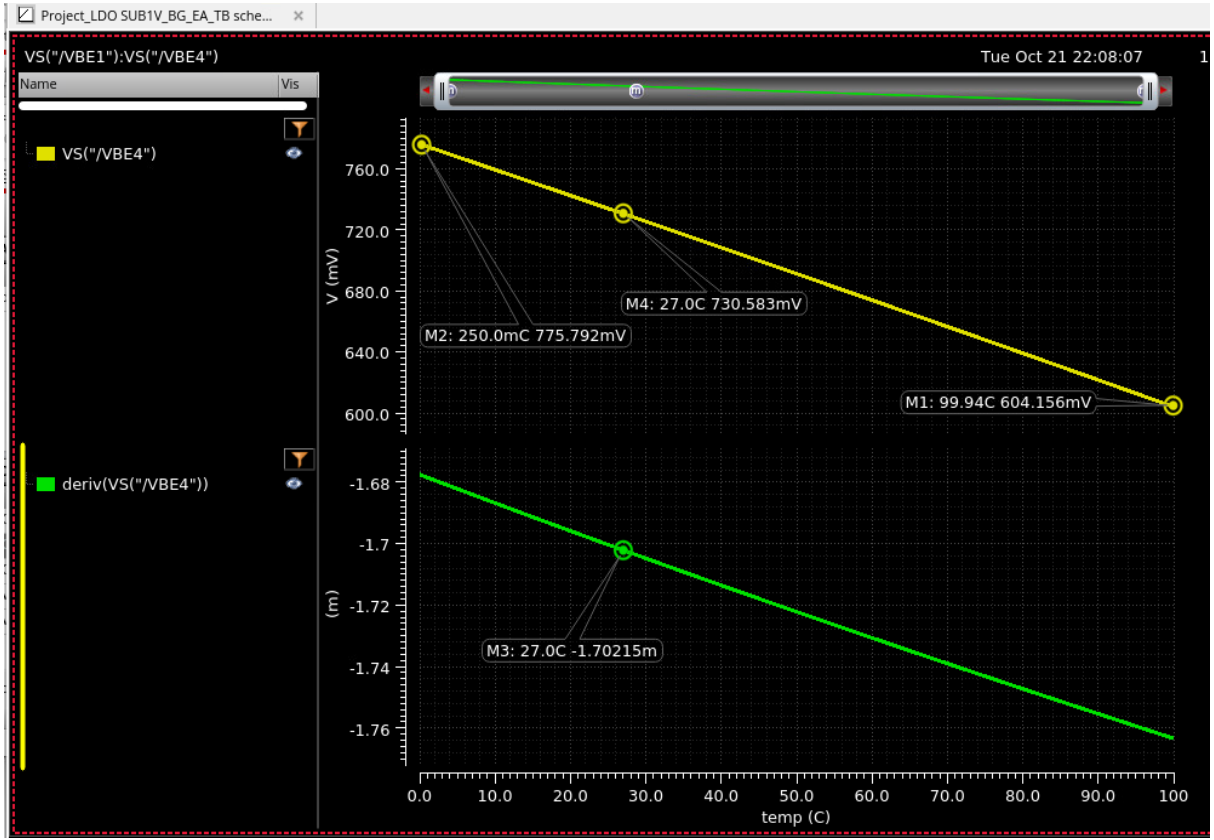
R1=1.5 KΩ
R2 = 14.15 KΩ

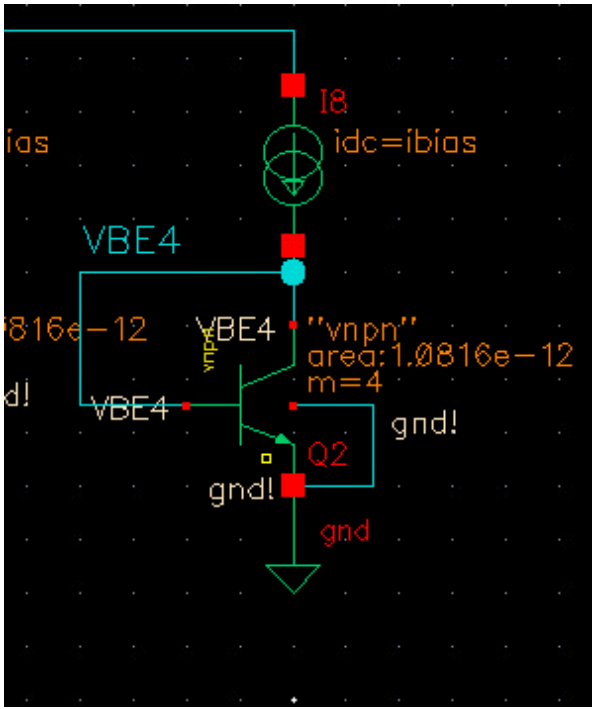
Now for Vbg = 0.3 Volts
RL = 3.416 KΩ

First Cut R numbers are :

R1 : 1.5 KΩ
R2 : 14.15 KΩ
R3 : 3.416 KΩ

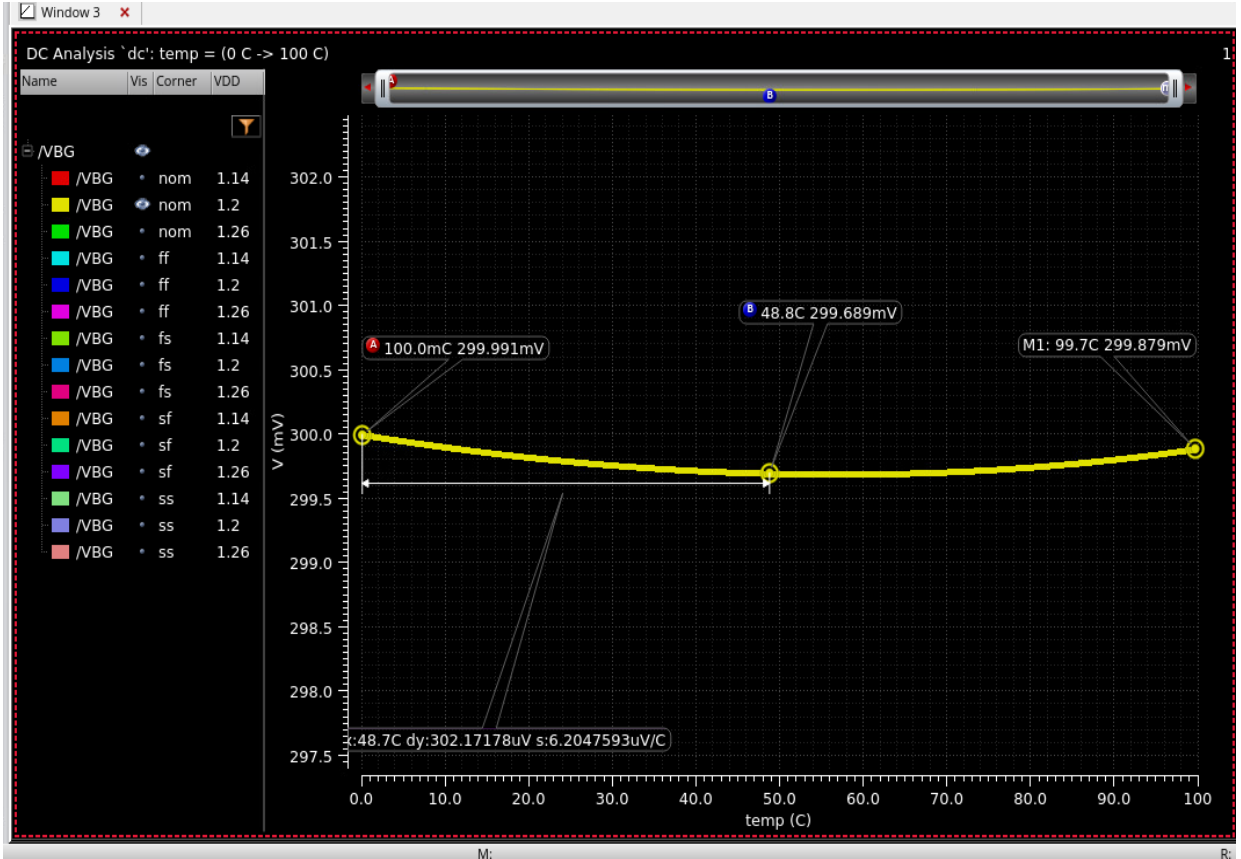
Ibias : 35uA (Vtln(8)/1.5K) assumed R1 : 1.5K



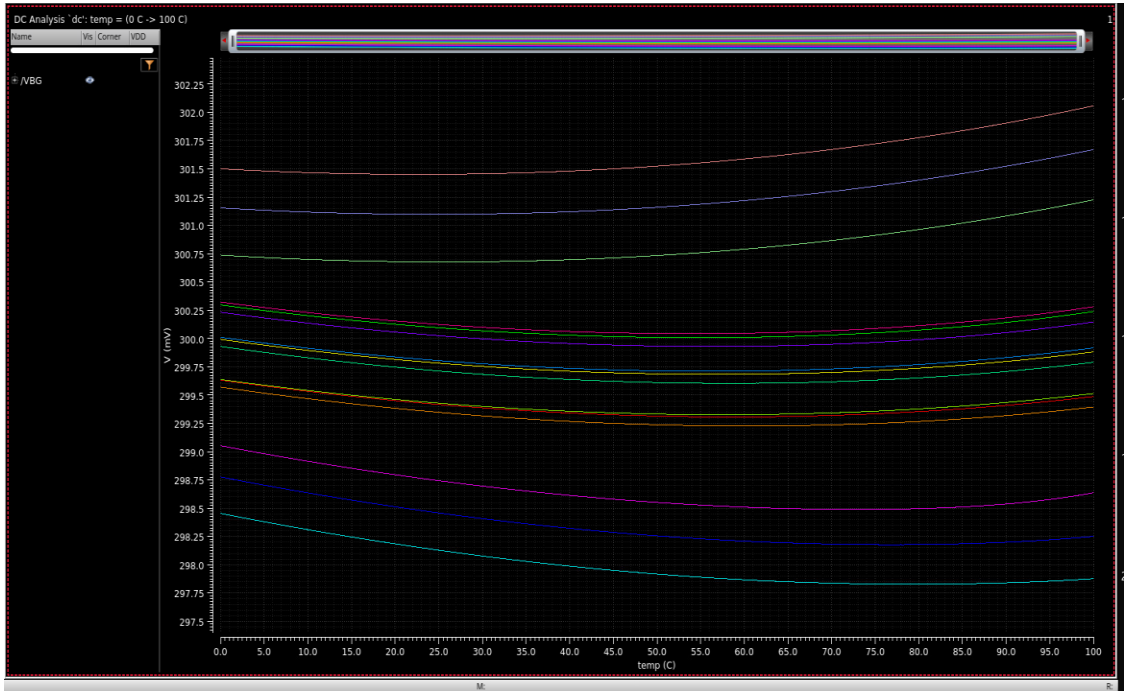


DC Sim (Nominal)

Note : The Handcalculation didn’t give the umbrella curve so using simulation the resistor values were tweaked in order to achieve that



DC Sims Across PVT (5 Process corners, 3 Supply Corners, 3 Temperature points 0,27,100)



We can see that across the process Vbe values changes which changes the effective Vbg value as well, this requires resistor trimming techniques which ensures the slope cancellation and Vbg value maintained at 300mV.

Power Consumption

9/12 rows

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	ff	fs	sf	ss
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
Parameters: VDD=1.14												
1	DCSIM	I_27C	462.7u	< 800u		pass	436.7u	487.3u	487.3u	463.2u	461.9u	436.7u
1	DCSIM	I_100C	460.6u	< 800u		pass	436.7u	483.8u	483.8u	460.9u	459.9u	436.7u
1	DCSIM	I_0C	463.8u	< 800u		pass	437u	489u	489u	464.4u	462.9u	437u
Parameters: VDD=1.2												
2	DCSIM	I_27C	464.5u	< 800u		pass	438.6u	489u	489u	464.9u	463.8u	438.6u
2	DCSIM	I_100C	462.2u	< 800u		pass	438.4u	485.4u	485.4u	462.5u	461.5u	438.4u
2	DCSIM	I_0C	465.7u	< 800u		pass	438.9u	490.8u	490.8u	466.1u	464.9u	438.9u
Parameters: VDD=1.26												
3	DCSIM	I_27C	466u	< 800u		pass	440.2u	490.5u	490.5u	466.4u	465.4u	440.2u
3	DCSIM	I_100C	463.6u	< 800u		pass	439.9u	486.8u	486.8u	463.8u	463u	439.9u
3	DCSIM	I_0C	467.3u	< 800u		pass	440.6u	492.4u	492.4u	467.7u	466.6u	440.6u

Max Power @ 1.2 Volts = 1.2*490uA = 0.58mW
Current Distribution : Around 200uA in Error Amps, 3*(0.3/3.86K) in the three branches : 233uA
And some biasing branches

Why Choose M=8 ?

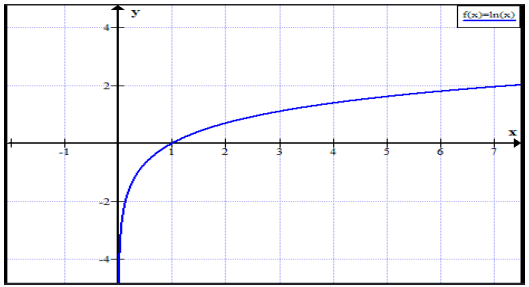
If we have a Vos (input referred offset of the opamp) then Vbg expression comes out to be :

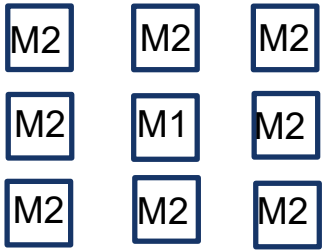
$Vbg = R_L/R_2(Vbe_1 + R_2/R_1 * Vt*\ln(M) – (1+R_2/R_1)*Vos)$

Now to reduce the effect of the offset R_2/R_1 needs to be minimized, to still get the flat Vbg we need to increase value of M so that temperature slopes are cancelled.

But we can't increase the value of M forever as it consumes significant area.

M=2 , ln(2) = 0.693
M=4 , ln(4) = 1.386
M=8, ln(8) = 2.079
M=16 , ln(16) = 2.77

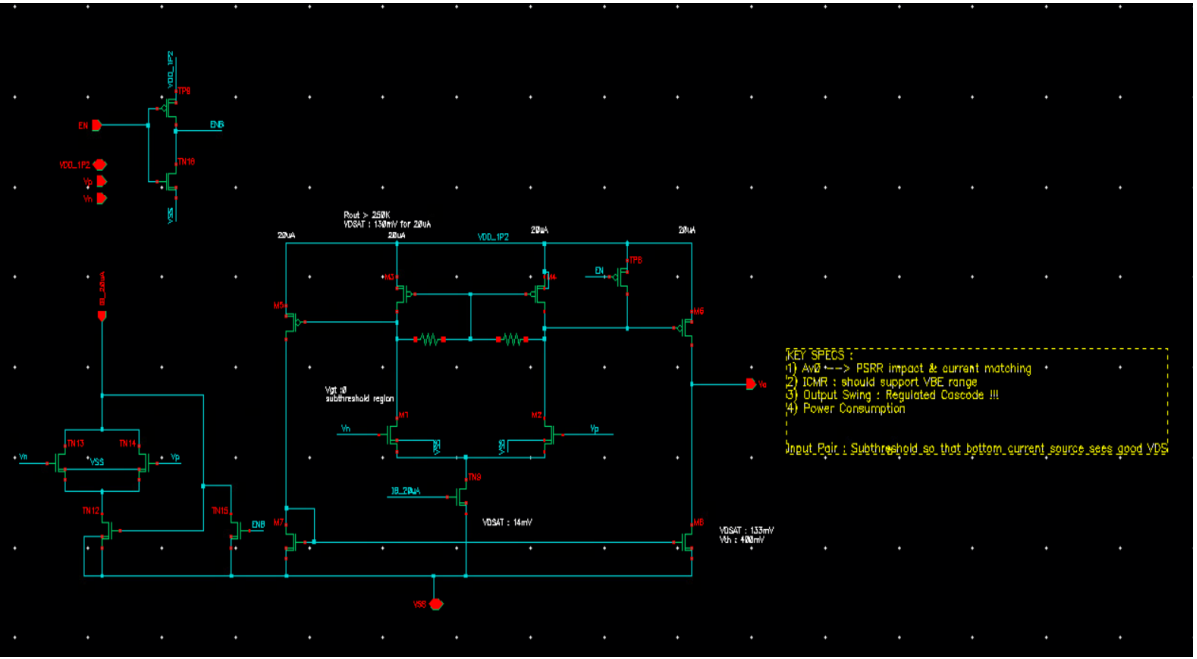




The percentage increase in the values as M increases seems to decrease, so choosing 8 seems to be good Tradeoff.

Error Amp Design

Since the input of the error amp is at voltage level of Vbe1 (Vx) that why the ICMR should be decided by that which is 601mV to 775mV (slide 6) → NMOS input pair-based ERROR AMP was chosen.
Current mirror type opamp but with some additional resistors in the first stage which gives boost to DC gain.



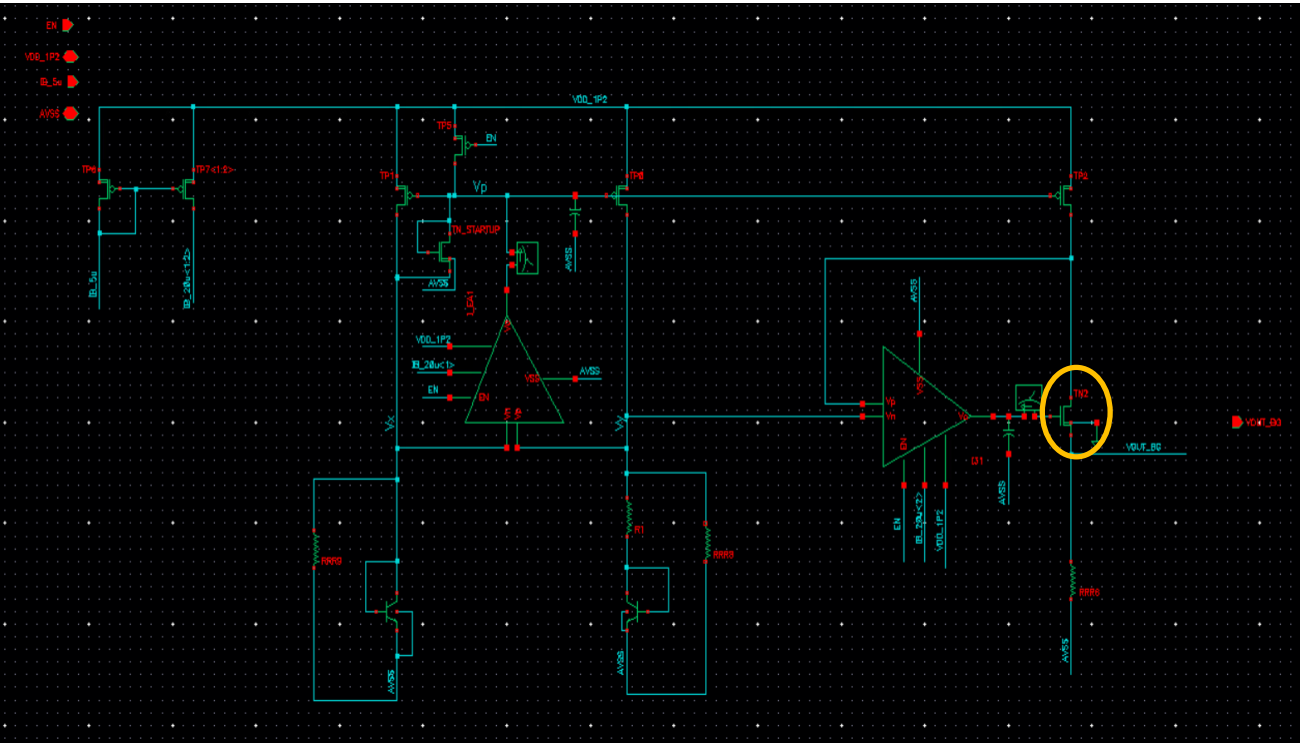
→Gain : Impacts overall accuracy, PSRR

→Should support a ICMR of VBE range across temperature (0.6 to 0.75mV)

→ Its output swing should also include Vbg+Vgs (output stage of the bandgap circuit has a regulated cascode structure)

→ There are two high impedance nodes in this opamp so there was **external cap** used to stabilize the neg-fb loops in which this opamp was used.

Error Amp Design



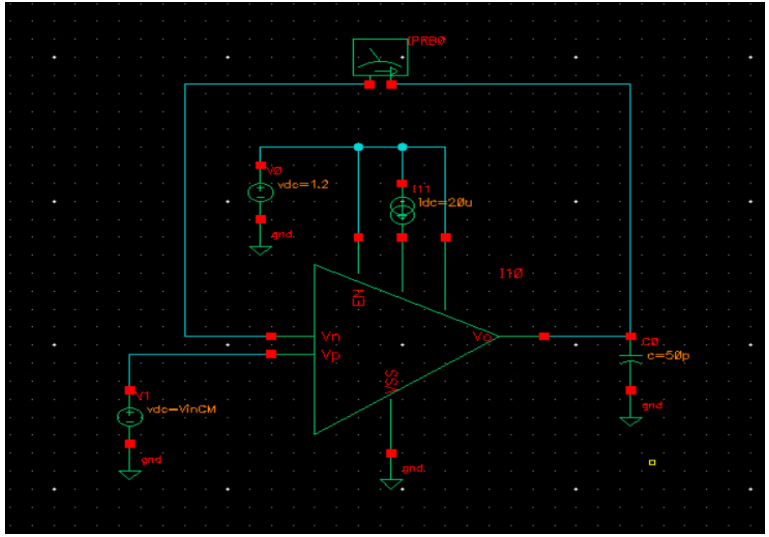
→ Its output swing should also include Vbg+Vgs (output stage of the bandgap circuit has a regulated cascode structure

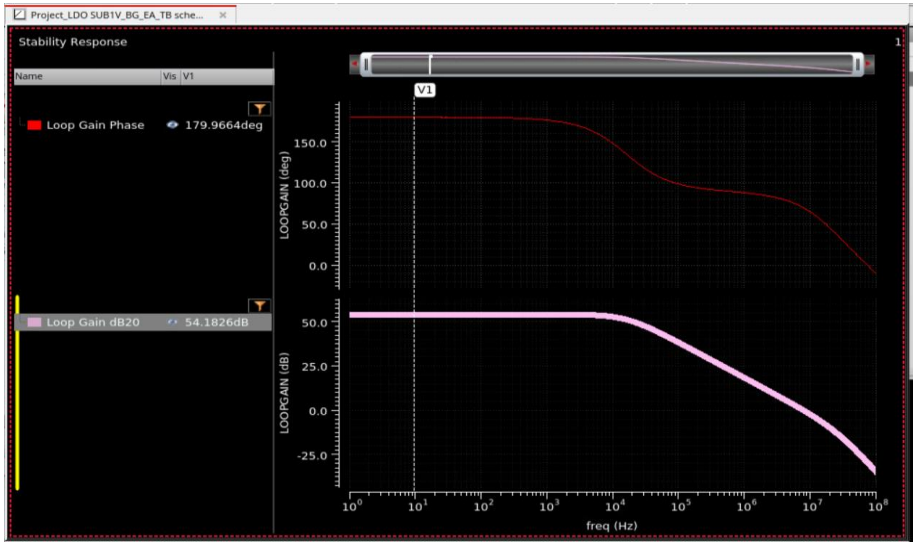
→ At the gate of the encircled transistor voltage will be **Vbg+ Vgs** (and Vgs will be slightly higher than usual due to body effect experienced by TN2)

→ So EA was designed such that output swing includes this point across temperature

Stand-Alone EA Sim Results

EA Current Consumption : 100uA



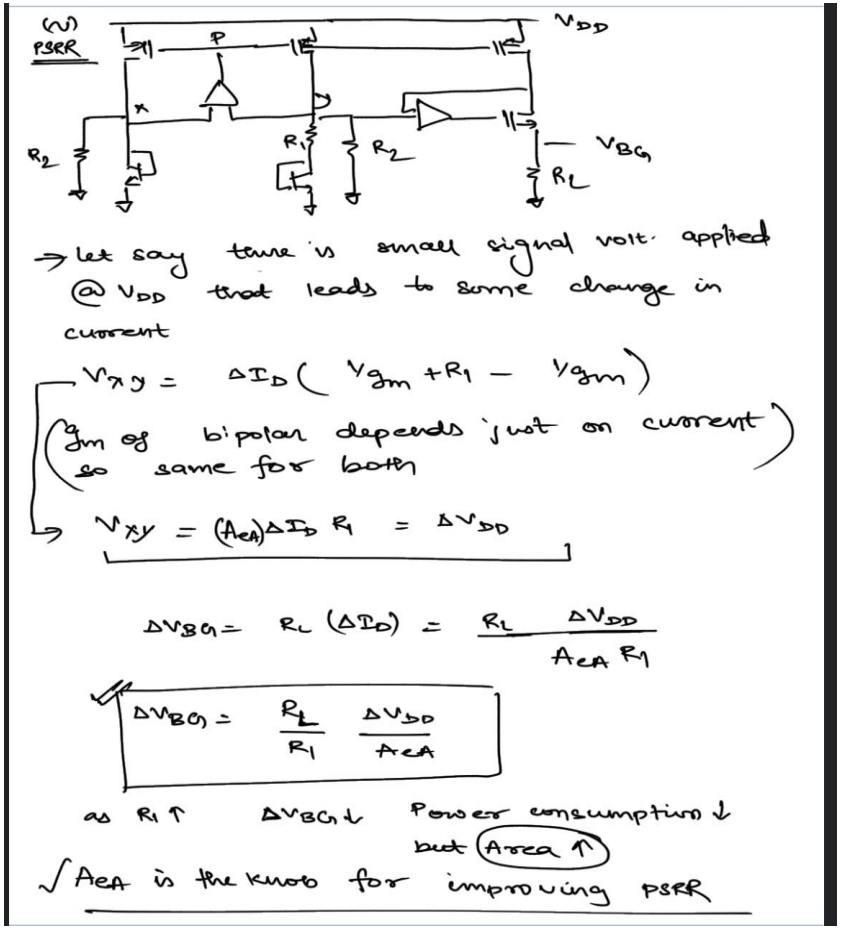


54dB DC gain
50pF output was just kept to ensure output node dominant pole

The –ve fb loop involving error amps uses lesser cap (more details in upcoming slides)

Output node impedance : 192Kohms
First Node Impedance : 30Kohms

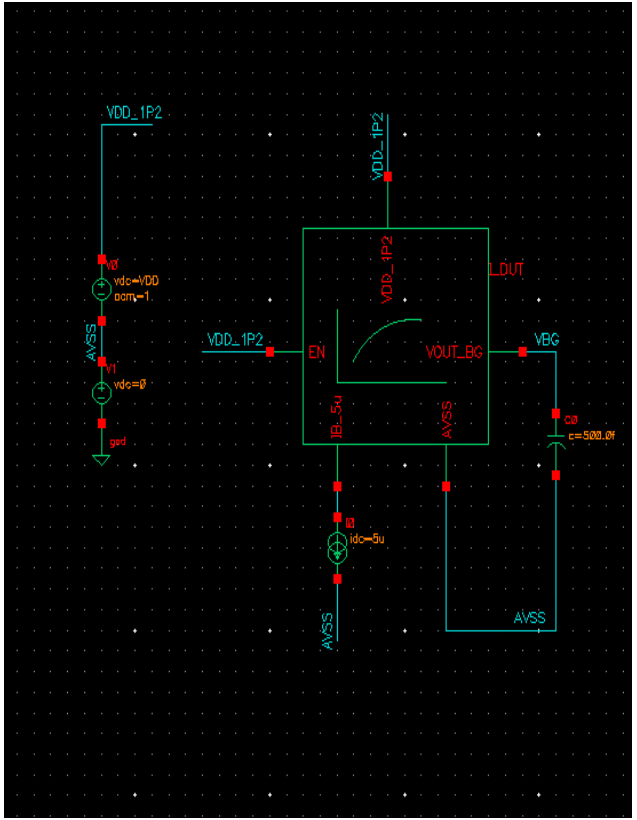
PSRR Calculations



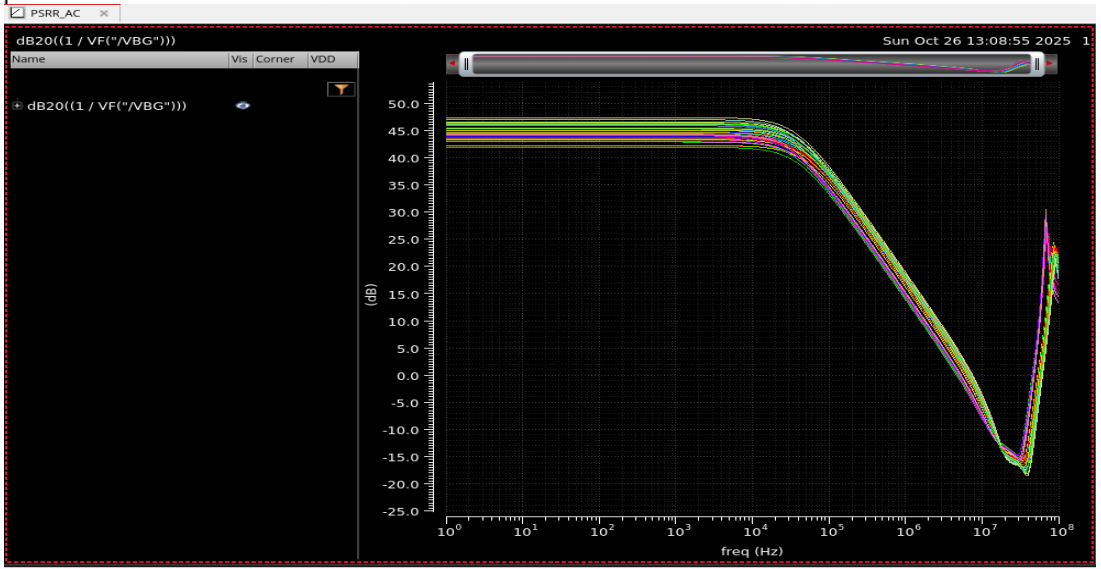
Here it's assumed that OPAMP is able to reject all the supply noise, which is indeed the case. PSR of the opamp is high due to the 2-stage structure.

PSR of Bandgap depends on error-Amp gain,RL, R1.

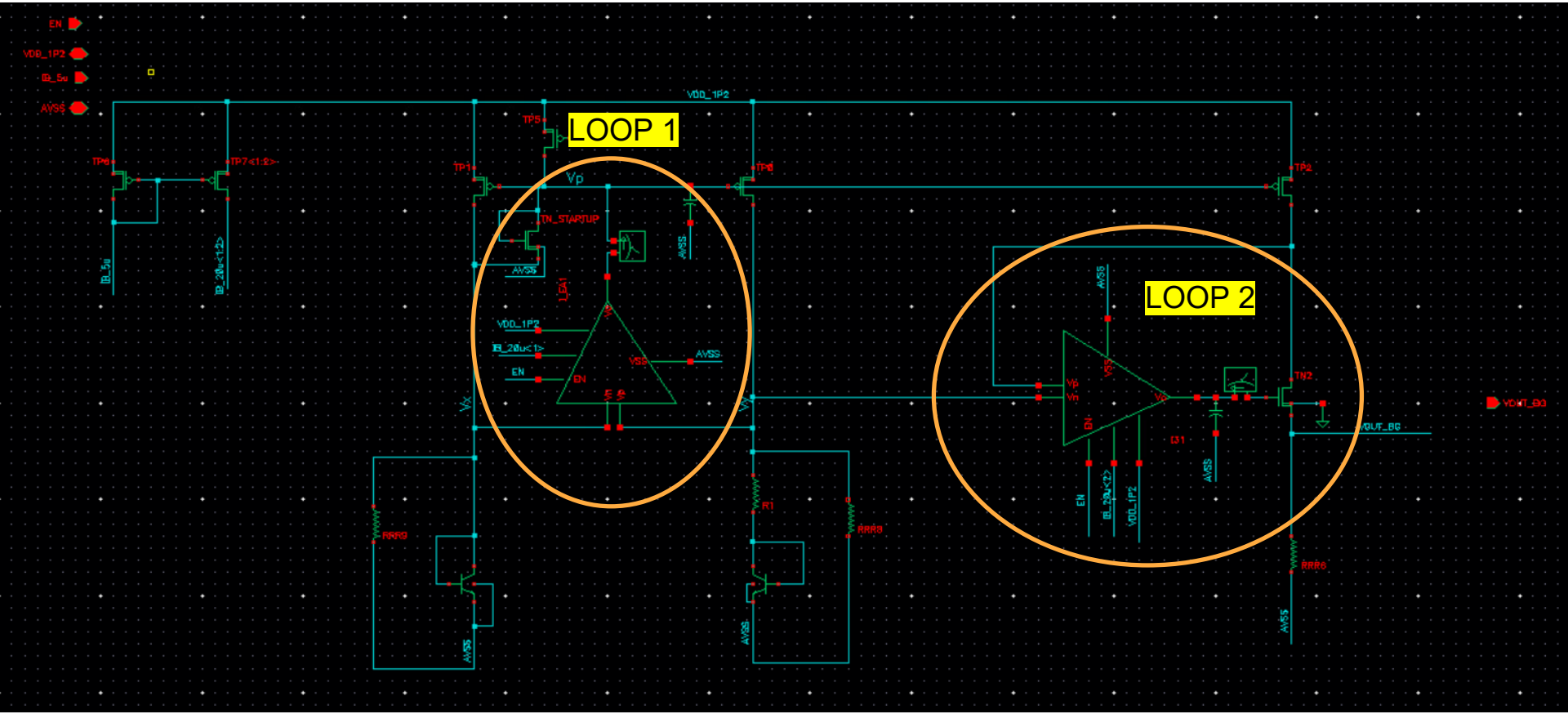
PSRR Sim Results & TB



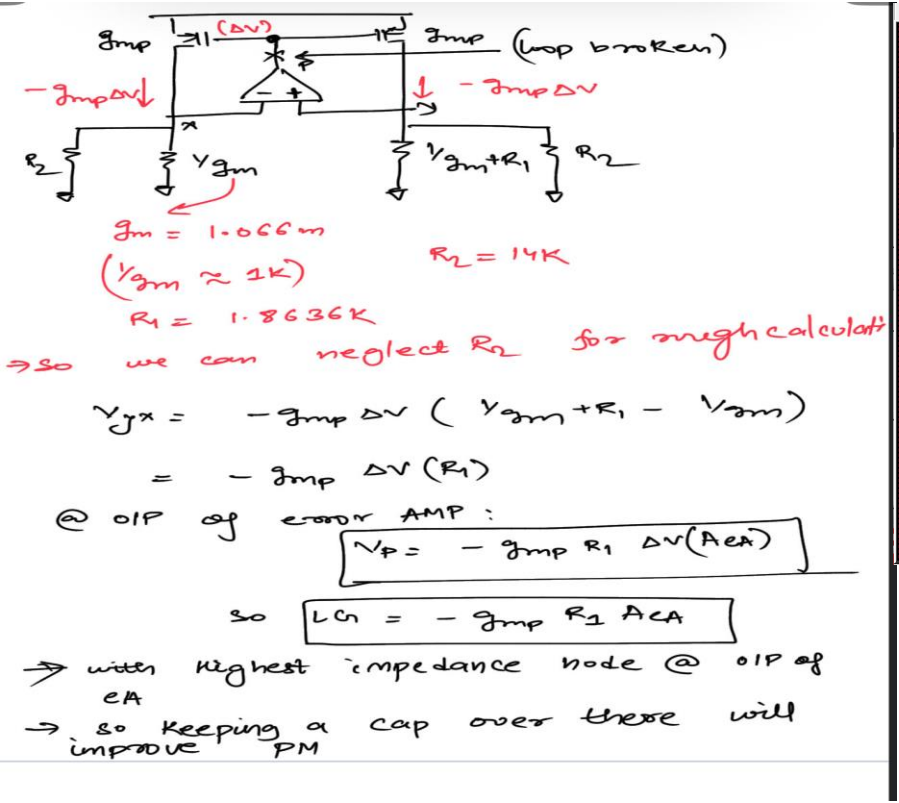
Point	Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
Parameters: VDD=1.2								
1	PSRR_AC	PSR_DC	45.02	> 40		pass	43.26	46.13
Parameters: VDD=1.14								
2	PSRR_AC	PSR_DC	43.53	> 40		pass	41.89	44.62
Parameters: VDD=1.26								
3	PSRR_AC	PSR_DC	46.23	> 40		pass	42.88	47.34

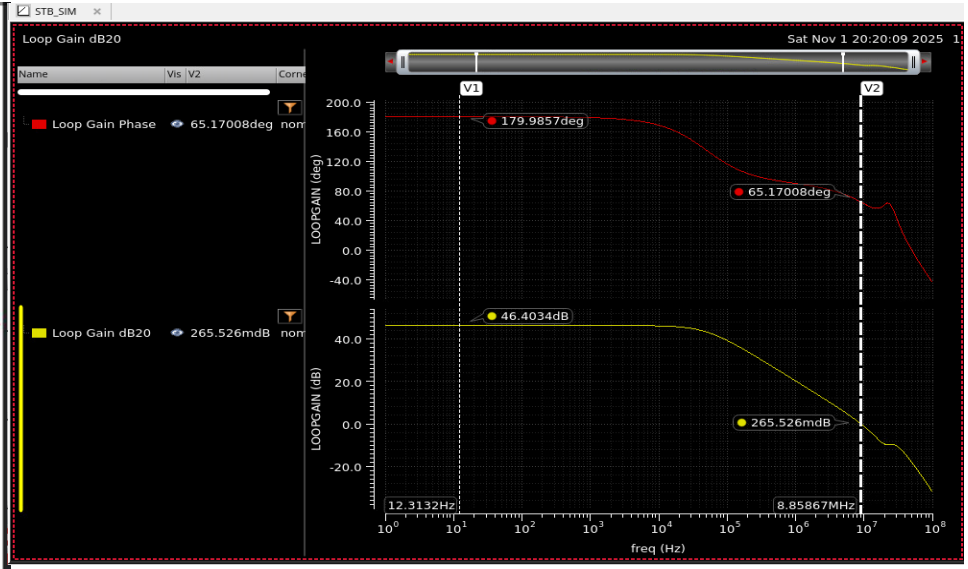


-ve FB loops Stability



Loop1



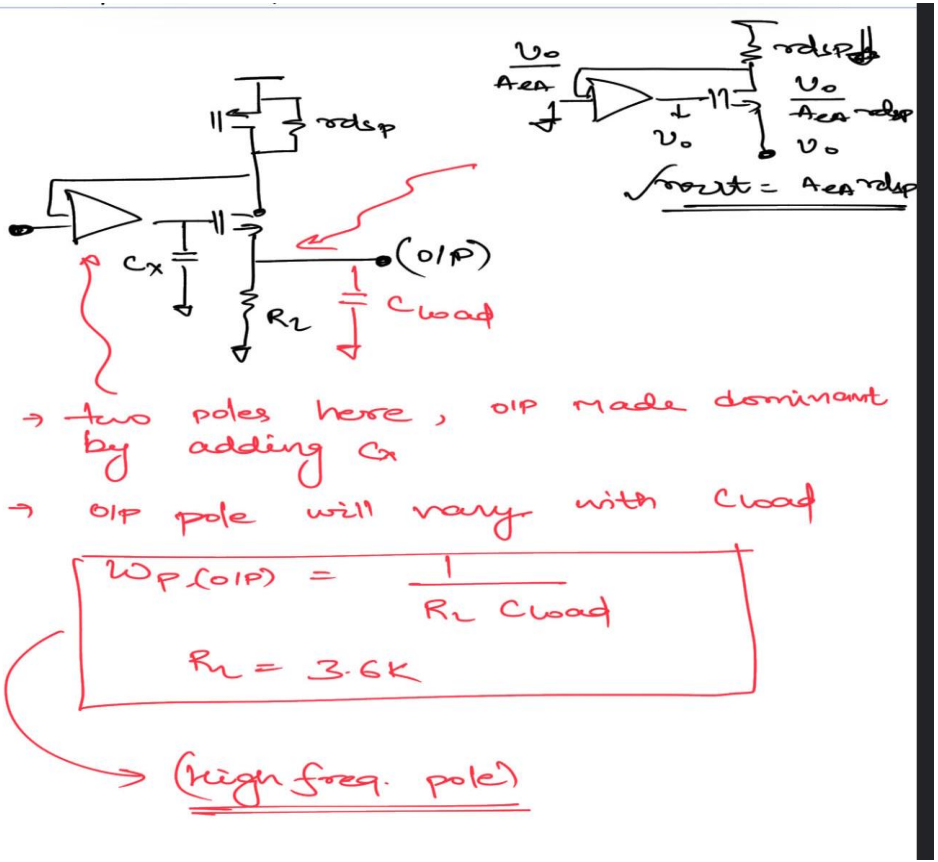


Test	Output	Nominal
Filter	Filter	Filter
STB_SIM	Loop Gain Phase	
STB_SIM	Loop Gain dB20	
STB_SIM	Phase Margin	64.65
STB_SIM	Av0	46.4

Loop1 Stb across Process & Temperature

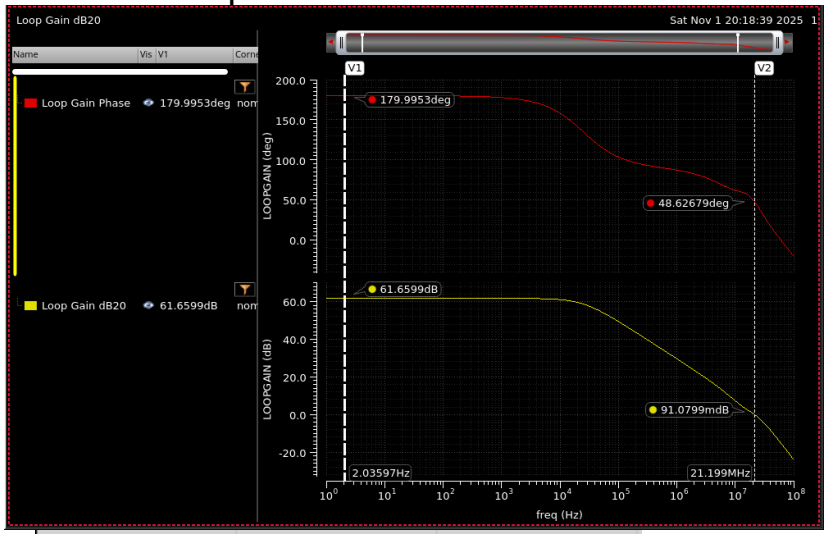
Test	Output	Spec	Weight	Pass/Fail	Min	Max	ff_0	ff_1	ff_2	fs_0	fs_1	fs_2	sf_0
STB_SIM	Loop Gain Phase												
STB_SIM	Loop Gain dB20												
STB_SIM	Phase Margin				61.28	71.18	61.28	63.84	70.16	63.01	65.34	71.18	61.67
STB_SIM	Av0				43.67	47.68	47.62	46.84	44.74	46.43	45.68	43.67	47.68

Loop 2



Loop Gain is higher in this case due to the presence of common-source stage. Due to which Error Amp used here was of less gain in order to place less cap (Cx) to make it stable.

Cx used : 40pF



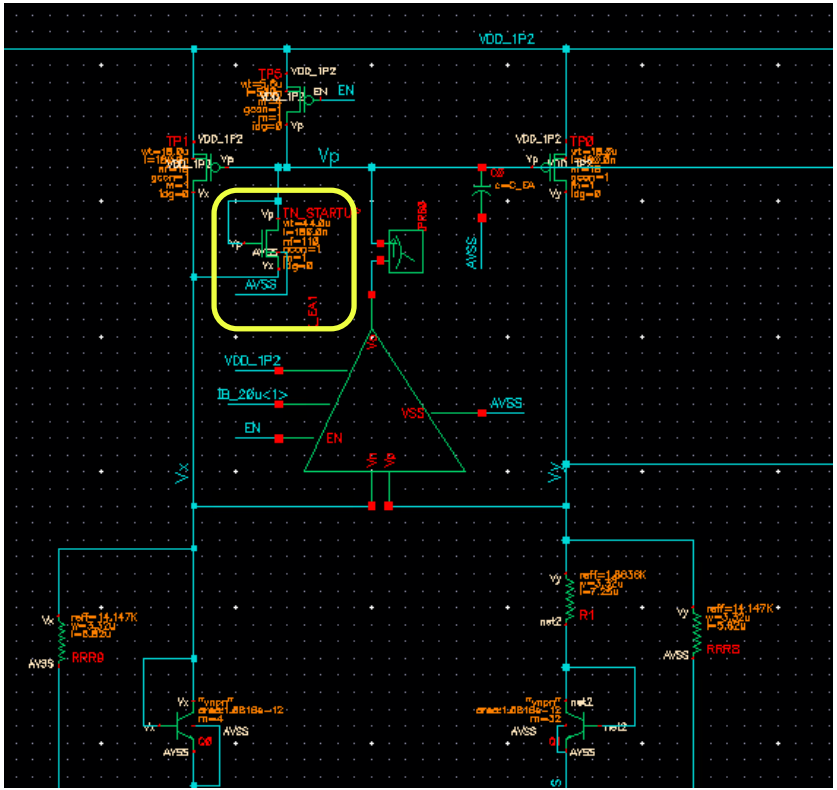
STB_SIM	Loop Gain Phase	
STB_SIM	Loop Gain dB20	
STB_SIM	Phase Margin	48.25
STB_SIM	Av0	61.66

Loop2 stability across Process and Temperature

4 rows

Test	Output	Spec	Weight	Pass/Fail	Min	Max	ff_0	ff_1	ff_2	fs_0	fs_1	fs_2	sf_0	s_
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
STB_SIM	Loop Gain Phase													
STB_SIM	Loop Gain dB20													
STB_SIM	Phase Margin				47.55	51.22	49.65	47.94	48.34	50.37	48.18	47.55	50.45	4
STB_SIM	Av0				60.33	62.25	62.09	62.25	61.71	61.85	62.1	61.74	60.67	6

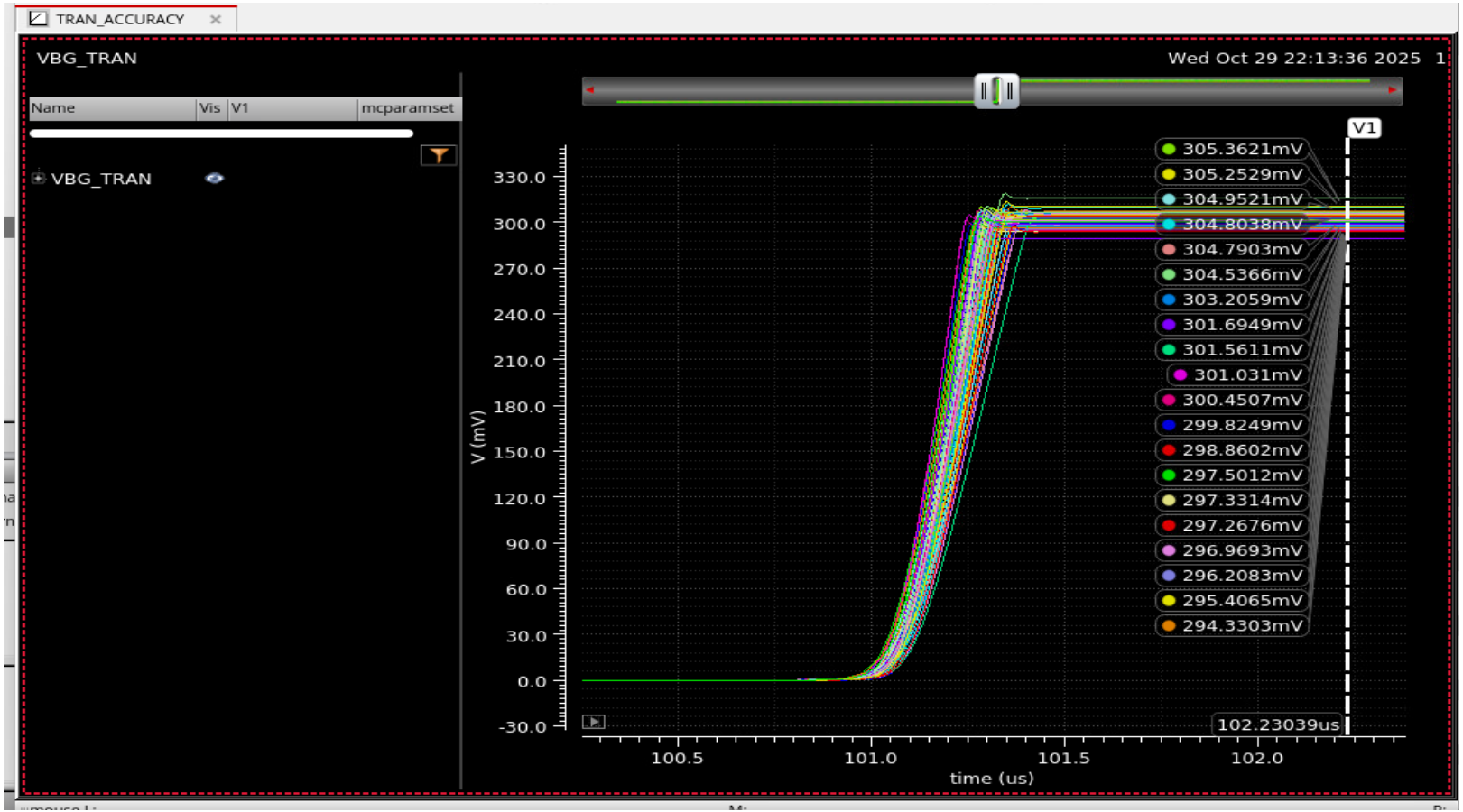
Startup Circuitry



Operation :
So if the startup device was not there than Vx& Vy can just stay at zero with Vp : VDD

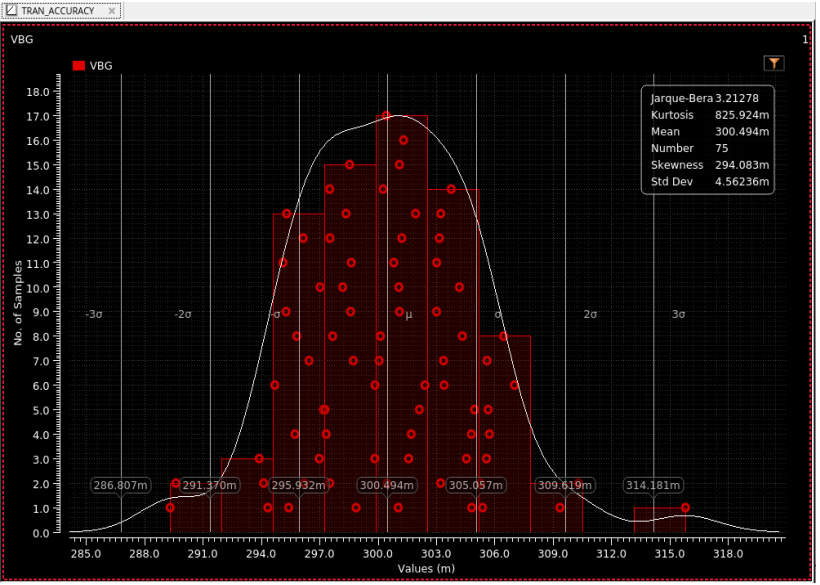
Now due to inclusion of this device, it will perturb the node Vx,Vy during the startup and during the steady state it won't be drawing any current so won't be disturbing the normal operation.

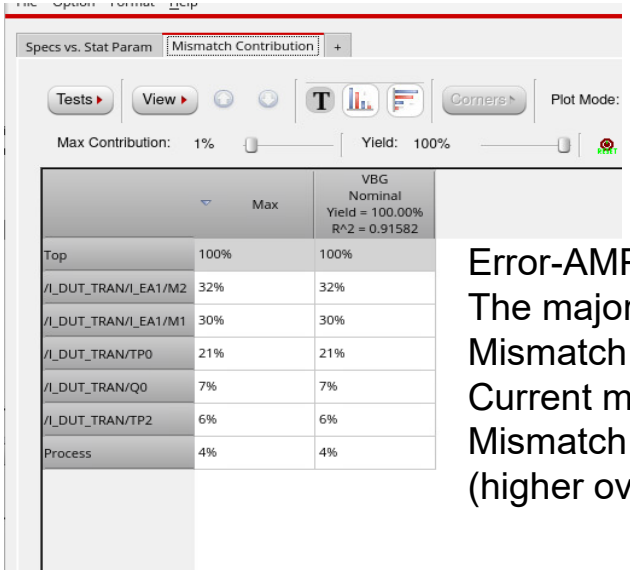
StartUP Sims (1M Ramp Rate at the Supply)



Monte Carlo Sim

TRAN_ACCURACY							
VBG(sum...	100% (75/75)	289.3m	info	315.8m	300.5m	4.562m	0
VBG	100% (75/75)	289.3m	info	315.8m	300.5m	4.562m	0





	Max	VBG Nominal Yield = 100.00% R^2 = 0.91582
Top	100%	100%
/I_DUT_TRAN/I_EA1/M2	32%	32%
/I_DUT_TRAN/I_EA1/M1	30%	30%
/I_DUT_TRAN/TP0	21%	21%
/I_DUT_TRAN/Q0	7%	7%
/I_DUT_TRAN/TP2	6%	6%
Process	4%	4%

Error-AMP offset is
The major contributor in the Mismatch.
Current mirror were optimized for Mismatch by having large lengths (higher overdrives)

SCM

	SPEC	Simulation
DC Accuracy	< 1% across temperature	@nominal 302uV Slide 7
PSRR DC	>40dB	Min PSRR achieved : 41.89 dB (across PVT) Slide 15
Power Consumption	<1mW	0.58mW Slide 9
Sigma (@27)	5mV	4.5mV Slide 21