ECEN 620: Network Theory

Final Project Report

Design of a 3.2GHz Frequency Synthesizer for Wireless Communications with spurs under -70 dBc

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Motivation & Project Overview

The oscillators used in RF transceivers are architected as frequency synthesizers to provide accurate control over the output frequency. The rapid increase in wireless applications has led to an increased development of many RF frequency synthesis techniques. A communication protocol such as Bluetooth has channels in the range of 2.4 - 2.48GHz (80 1MHz channels). This creates a need for an accurate frequency synthesizer.

A common shortcoming of such a frequency synthesizer using integer divider ratios is that the frequency step size is always equal to/or multiple of reference frequency. For applications which require a step size which is lesser than the reference frequency. Fractional–N synthesizers help solve this problem, allowing a *fractional* relationship between the channel spacing and reference frequency. A fractional N-synthesizer makes use of a time varying divider ratio rather than a constant divider ratio to get intermediate non-integer ratios.

In this project we will use this principle to design a 3.2 GHz frequency synthesizer which will have channels at the spacing of 8 MHz and the spur level below –70 dBc and Phase noise lesser than –110 dBc at 1MHz offset. We are targeting a tuning range of about 6.28% which means frequency synthesizer can provide clock whose frequency can range from 3 to 3.2 GHz.

Literature Survey

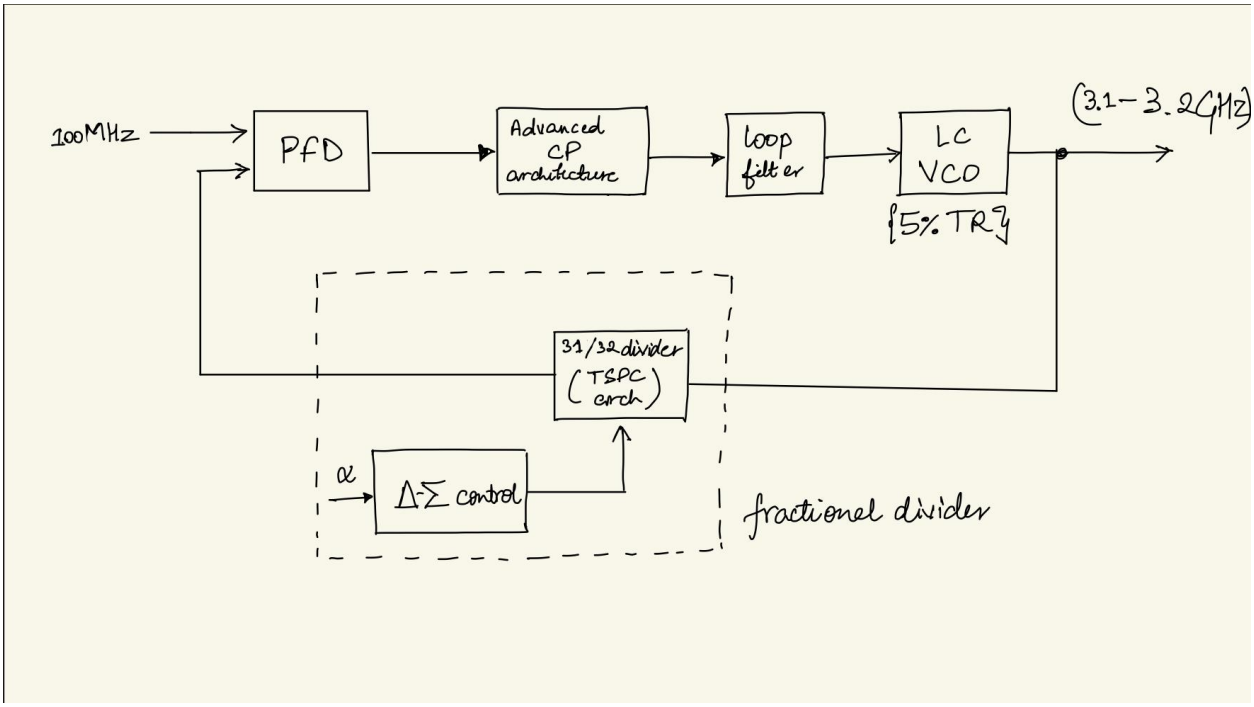
While choosing an architecture we looked at a variety of research papers and thesis dissertations to understand the pros and cons of each topology to meet the target specifications. The following research resources were useful sources of information and reference planning our work. We looked at some digital PLLs as well.

1) RF microelectronics by Behzad Razavi: Useful in figuring out the pros and cons of Integer-N and fractional-N PLL
2) Design of Analog CMOS Integrated Circuits by Behzad Razavi: Useful in figuring out the topology to use for oscillators & Charge pumps.
3) Woogeun Rhee; Zhiping Yu, "Fractional-N PLL," in *Phase-Locked Loops: System Perspectives and Circuit Design Aspects*, IEEE, 2024, pp.237-285, doi: 10.1002/9781119909071.ch9.
4) M. H. Perrott, M. D. Trott and C. G. Sodini, "A modeling approach for /spl Sigma/-/spl Delta/ fractional-N frequency synthesizers allowing straightforward noise analysis," in *IEEE Journal of Solid-State Circuits*, vol. 37, no. 8, pp. 1028-1038, Aug. 2002, doi: 10.1109/JSSC.2002.800925
5) D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori and A. L. Lacaita, "A 2.9–4.0-GHz Fractional-N Digital PLL With Bang-Bang Phase Detector and 560-fs_{rms} Integrated Jitter at 4.5-mW Power," in *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2745-2758, Dec. 2011, doi: 10.1109/JSSC.2011.2162917.
6) B. Miller and R. J. Conley, "A multiple modulator fractional divider," in *IEEE Transactions on Instrumentation and Measurement*, vol. 40, no. 3, pp. 578-583, June 1991, doi: 10.1109/19.87022.
7) T. A. D. Riley, M. A. Copeland and T. A. Kwasniewski, "Delta-sigma modulation in fractional-N frequency synthesis," in *IEEE Journal of Solid-State Circuits*, vol. 28, no. 5, pp. 553-559, May 1993, doi: 10.1109/4.229400.
8) C. Weltin-Wu, G. Zhao and I. Galton, "A 3.5 GHz Digital Fractional- PLL Frequency Synthesizer Based on Ring Oscillator Frequency-to-Digital Conversion," in *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 2988-3002, Dec. 2015, doi: 10.1109/JSSC.2015.2468712
9) A. Elkholy, T. Anand, W. -S. Choi, A. Elshazly and P. K. Hanumolu, "A 3.7 mW Low-Noise Wide-Bandwidth 4.5 GHz Digital Fractional-N PLL Using Time Amplifier-Based TDC," in *IEEE Journal of Solid-State Circuits*, vol. 50, no. 4, pp. 867-881, April 2015, doi: 10.1109/JSSC.2014.2385753.
10) M. M. Bajestan, H. Attah and K. Entesari, "A 2.8–4.3GHz wideband fractional-N sub-sampling synthesizer with −112.5dBc/Hz in-band phase noise," *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, San Francisco, CA, USA, 2016, pp. 126-129, doi: 10.1109/RFIC.2016.7508267.

	[7]	[8]	[9] *	[10] *	[11]
Frequency	405MHz	0.15-1GHz	3.5GHz	4.5 GHz	3.2 GHz
Reference frequency	10MHz	200KHz	26MHz	50 MHz	40 MHz
Channel spacing	5kHz	2kHz	-	-	-
Divider	40/41	3-modulator divider + 32/33 prescaler	-	-	-
Phase Noise	-70dBc	-80dBc	-92dBc @100kHz	-104 dBc @100 kHz	-143 dBc @20MHz

*Digital PLLs

Architecture



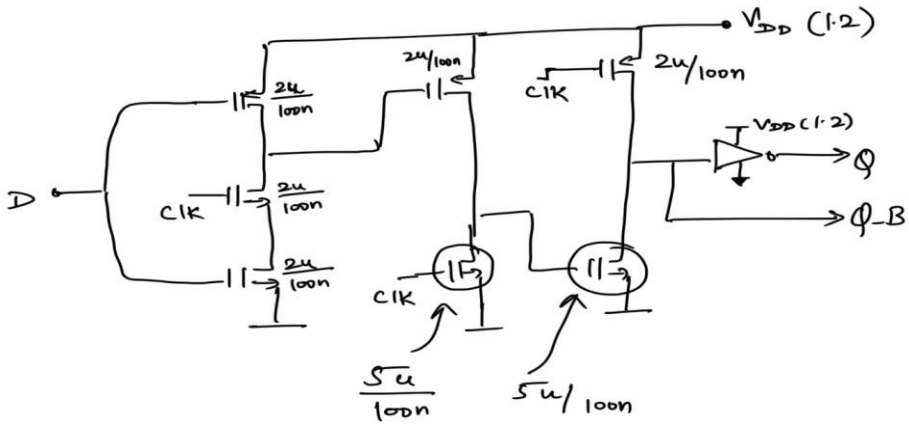
3rd Order Type-2 Fractional-N Charge Pump based PLL with Digital Control

In the proposed architecture we will be going for **LC VCO** since it will be easier to meet the phase noise spec using the LC oscillator as compared to the ring oscillator. We will be going with capacitive tuning whose control voltage is provided by the loop filter. MOSFET is used as the capacitor in the LC oscillator. It was seen that with the control voltage changing from **0.2 Volts to 1 Volt** the Frequency of the oscillator changed from **3 GHz to 3.2 GHz** which indicates we do have some margin on the control voltage to meet the frequency range.

Divider Architecture is based on **TSPC D Flip Flop**. Since the LC-VCO produces sinusoidal waveform and divider works with CMOS levels as compared to the CML logic level we are working on adding a comparator/ **CML-CMOS** converter between the VCO and Divider to ensure proper operation.

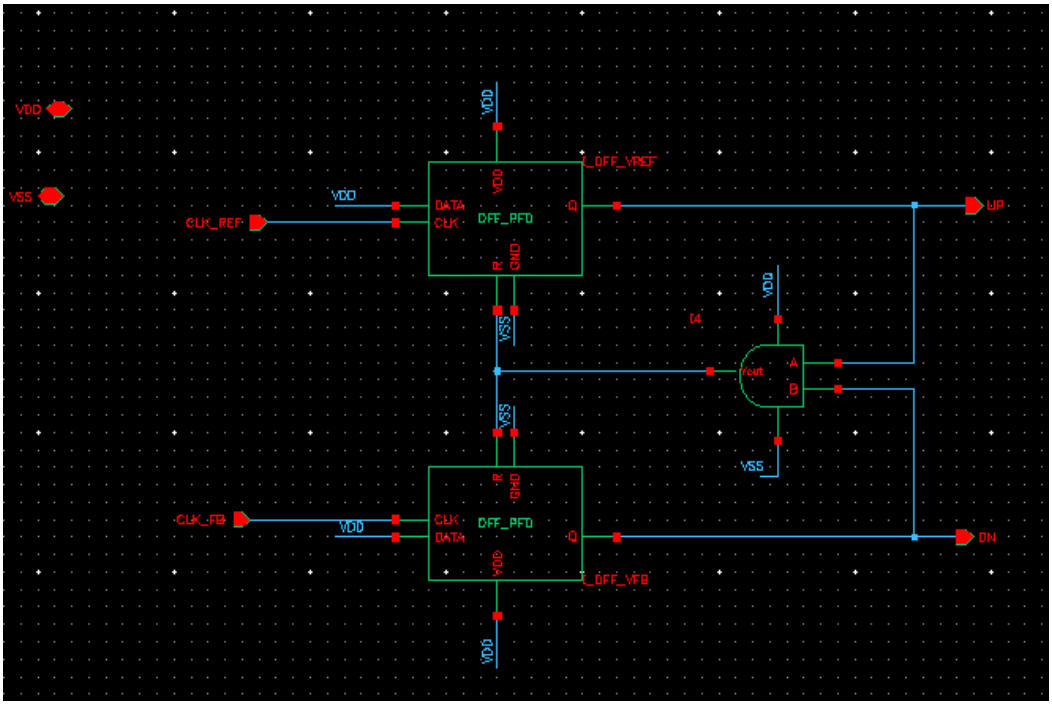
Below is the Dual Modulus 31/32 Divider circuitry which is used in the PLL loop.

Below is the D Flip Flop that we will be using to achieve our desired divider operation. (work well till 3.5 GHz, results attached in the next section).



Implementation Details

A) **PFD**: Standard phase-frequency detector was being used for phase and frequency locking purposes. Its working was checked till 200MHz as our reference frequency was around 100MHz. Below is the schematic attached for PFD.
There was no external delay circuitry added to avoid the dead zone as the gates (AND & NOR) used were providing the needed delay.

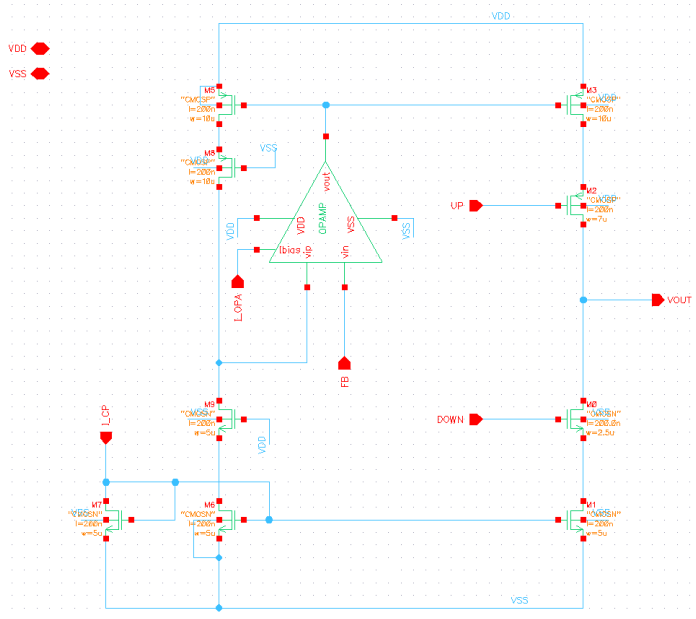


B) Charge Pump & Filter Parameter Calculations:

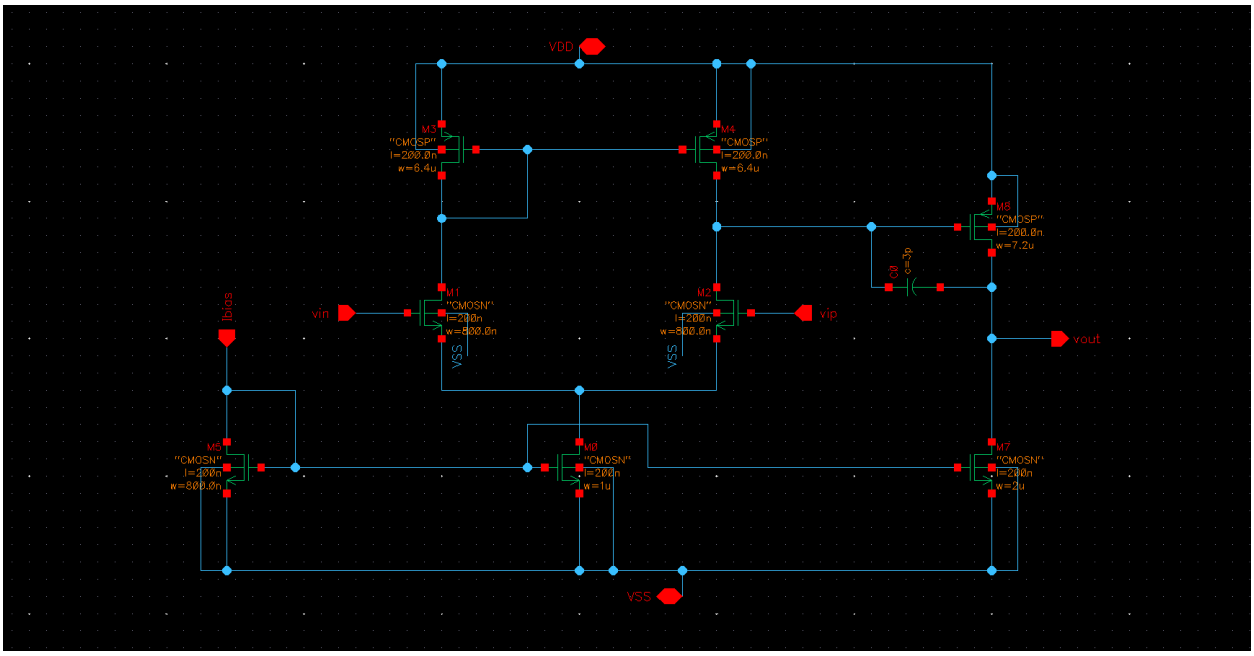
These values were calculated based on Fout = 3.2GHz
Fref = 100MHz and using N=32 (31/32 dual modulus divider)
Bandwidth = Fref/10 = 10MHz
Kvco = 2π*(0.35) GHz/V
Following the procedure mentioned in the course material we get the following values :
R: 10 KΩ
C1: 5.74 pF
C2 = C1/12 = 0.478 pF
Icp = 105uA

Tradeoff was chosen between the bandwidth and the ripples on Vcontrol as having a higher bandwidth was given more ideal spectrum on VCO output means the loop try to replicate the crystal oscillator spectrum (Fref) on the output which in turn gives better phase noise number but since the bandwidth is higher loop filter passes on the ripples till higher frequency.

Charge Pump Schematics:



Charge Pump OPAMP Details:

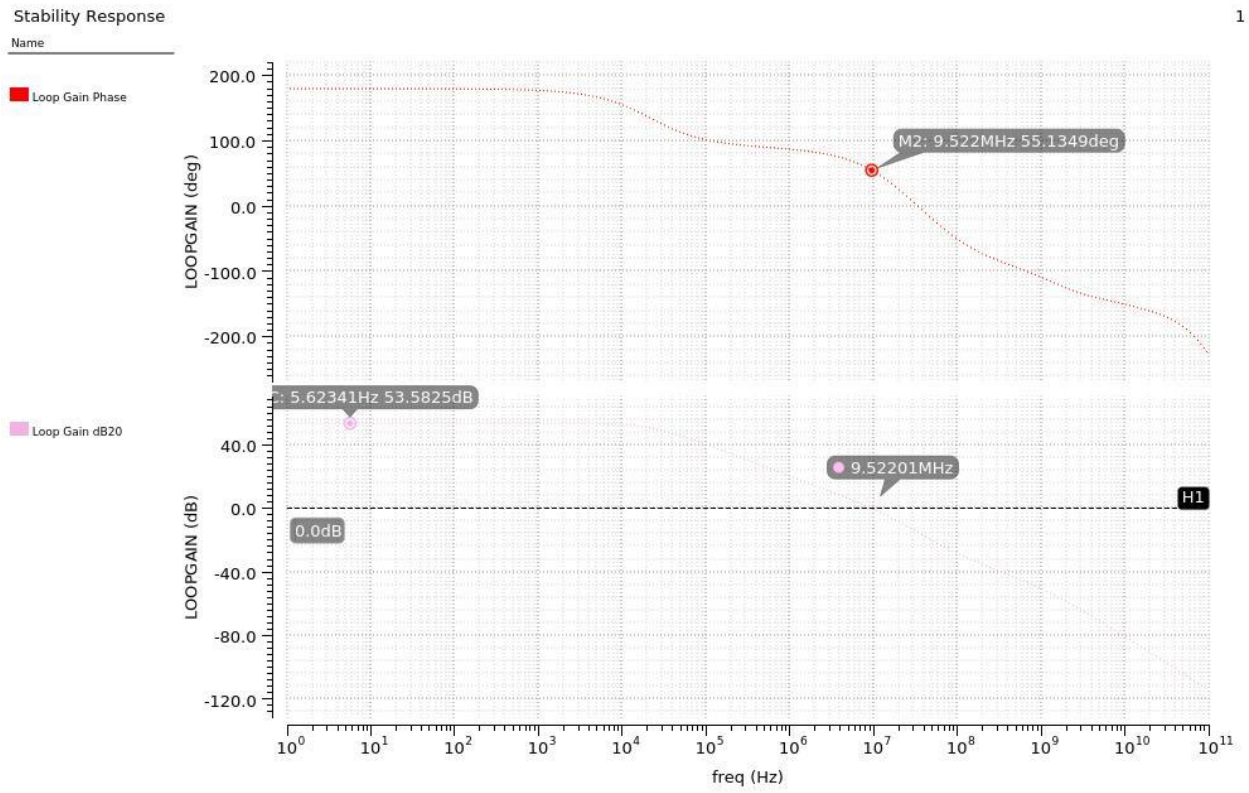


2 stage Miller compensated OPAMP

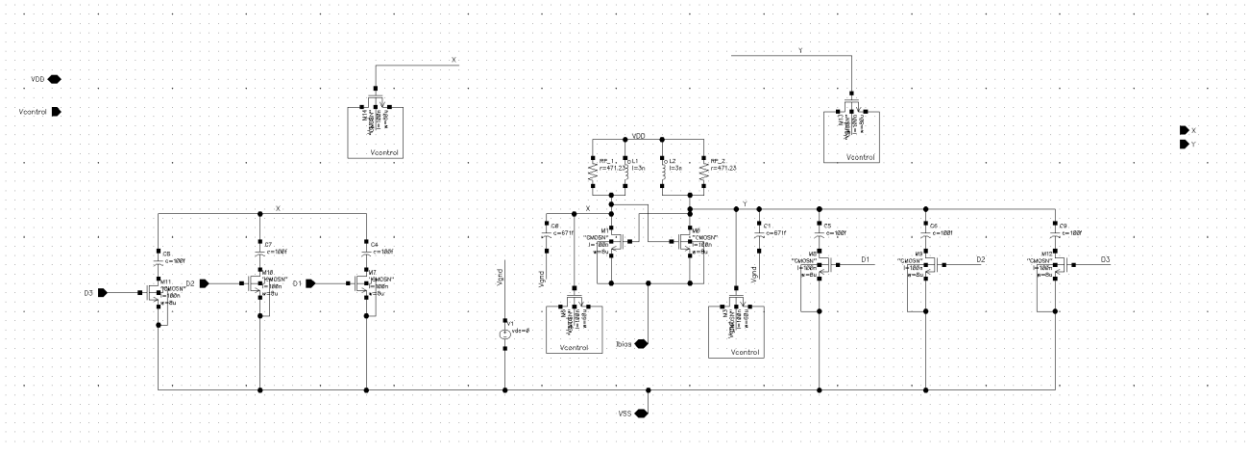
Phase margin: 55 degrees (unity feedback configuration)

A0: 53.5835 dB

UGB: 9.5 MHz (It was not designed for a specific UGB as this opamp was meant to just keep the input terminals average voltage at the same voltage which will ensure lesser ripples on the Vcontrol).

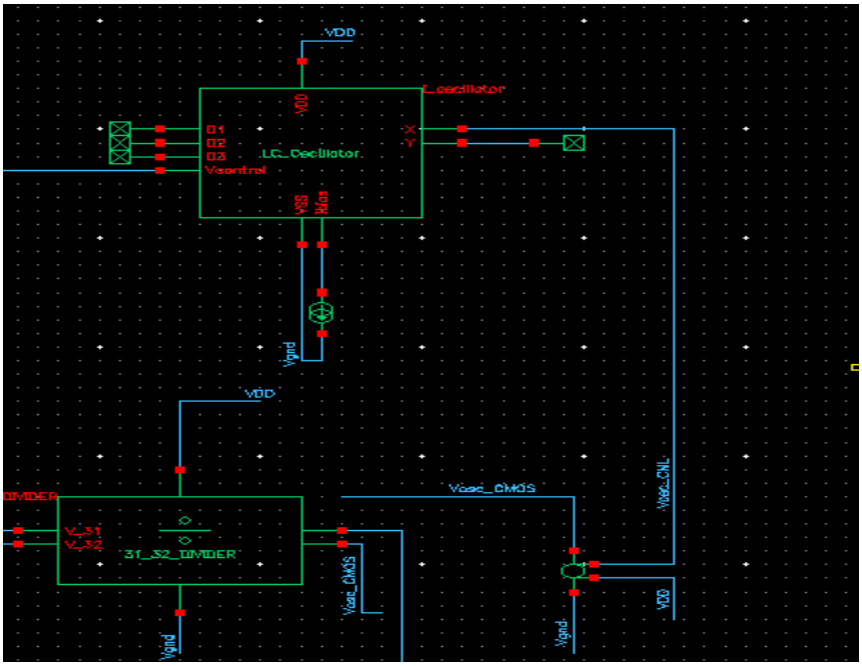


C) LC-VCO: It was designed such that as the control voltage increases the frequency of the LC-VCO also increases.
Cap built using MOSFET was used for changing the frequency with the change in Vcontrol.
Target Frequency: 3 GHz to 3.2 GHz for Vc from 200mV to 1V
200mV margin was kept on the Vcontrol.
Schematics Used:



D) CML to CMOS Converter:

To convert the CML waveforms into CMOS levels compatible with the divider, a comparator was being used which acted like CML to CMOS converter. VCO output was having a common mode level of VDD, comparator was comparing the VCO output with VDD and resulting output was given to Divider input.



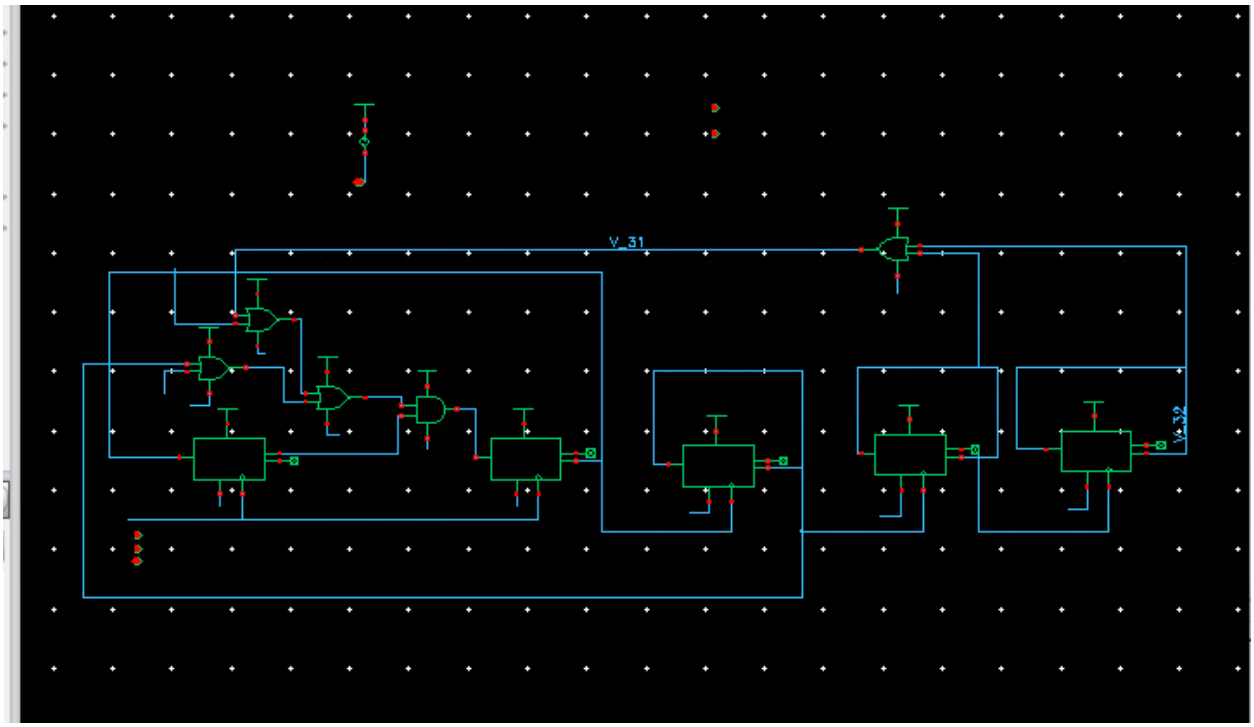
E) Sigma-delta Control: To achieve the fractional divider ratios modulus control of the divider was fed using the sigma-delta control. This block was implemented in Verilog-A.

Verilog-A code for Sigma-Delta Control:

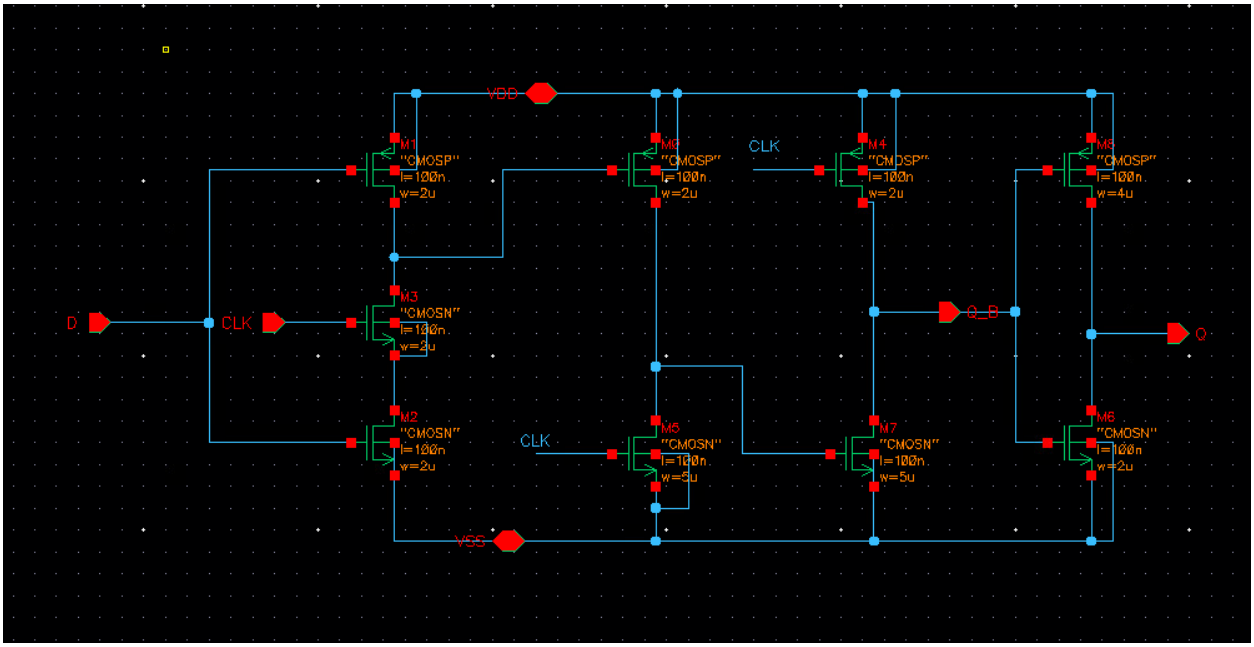
```
//
module sigmadelta_1storder(vin, vclk, vout);
input vin, vclk;
output vout;
electrical vin, vout, vclk ;
parameter real vth=0.0 ;
parameter real vout_high=1.2 ;
parameter real vtrans_clk=0.6 ;
parameter real trise=1p from (0:inf);
parameter real tfall=1p from (0:inf);
parameter real tdel=0.0 from [0:inf);

   real vsum;
   real vd;
   real vint ;
   real vout_val;

   real hi, lo;

   analog begin

      @ ( initial_step ) begin
         vout_val = 1.0;
         hi=1.0;
         lo=-1.0;
      end

      @ (cross(V(vclk)-vtrans_clk, 1.0))begin

         // summing junction
         vsum = V(vin) - vd ;

         // integrator
         vint = vsum + vint;

         // quantizer
         if (vint > vth)
            vout_val = hi ;
     else
            vout_val = lo ;

         // D2A
         vd = vout_high * vout_val ;

      end
      V(vout) <+ transition(vout_val, tdel, trise, tfall);
   end
endmodule
```

F) Divider 31/32 Dual Modulus Divider:

Schematics Used:



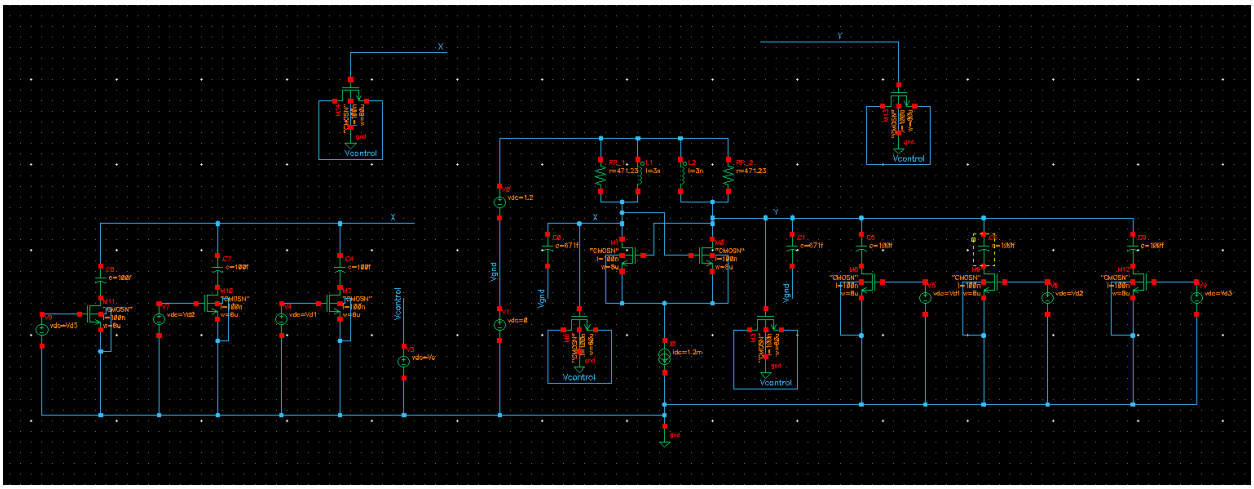
High Speed D-FlipFlop used: This was tested till 3.5 GHz



Simulation Results

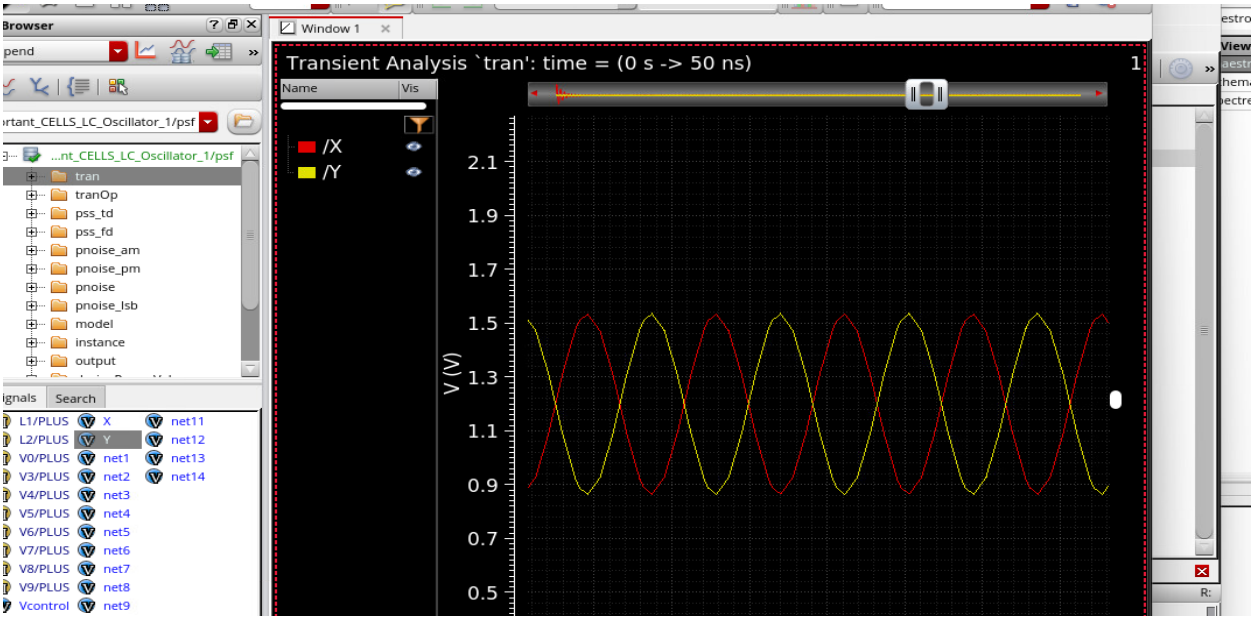
A) Oscillator Simulation Results

Schematic and Testbench



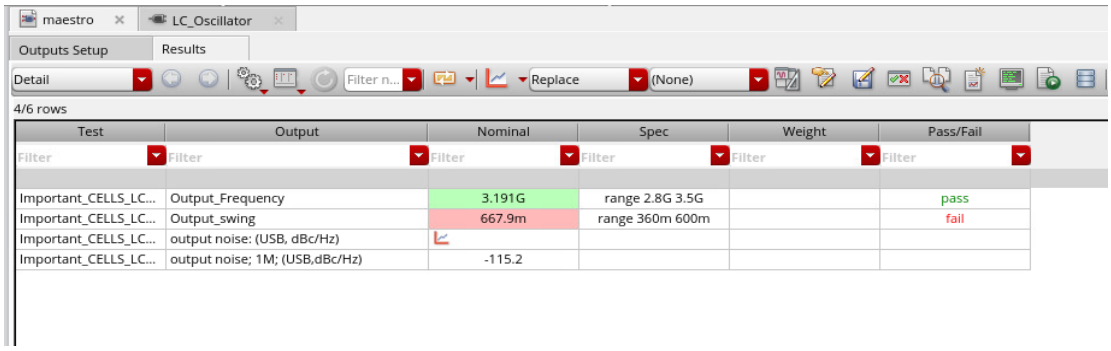
Results:

1) Control Voltage of 0.2 Volts



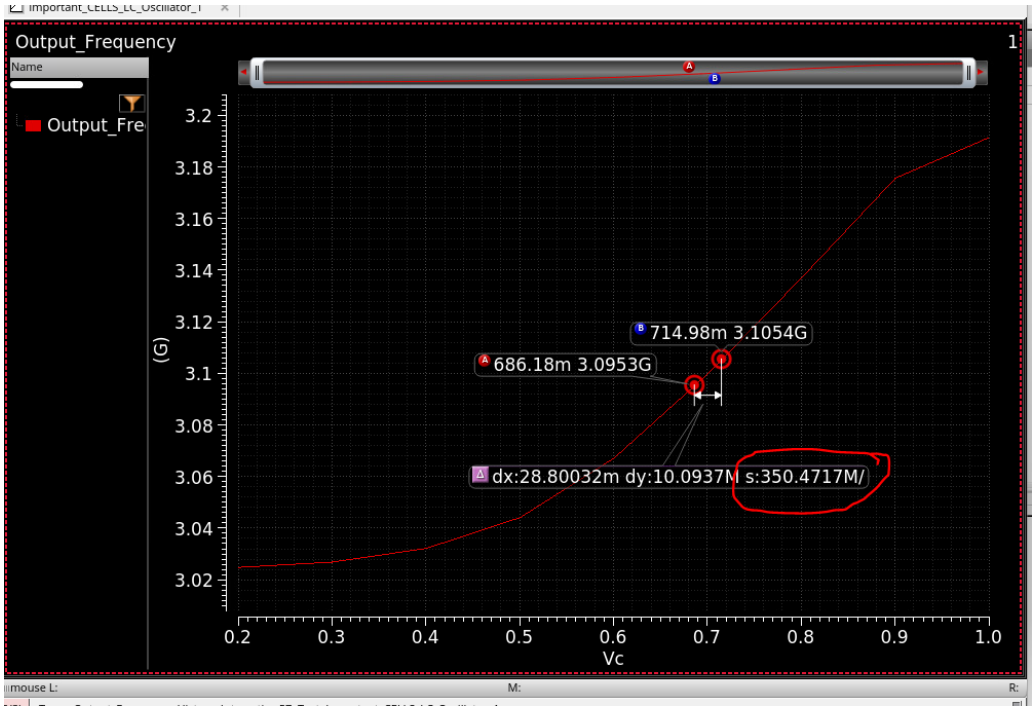
Test	Output	Nominal	Spec
Important_CELLS_LC...	Output_Frequency	3.021G	range 2.8G 3.5G
Important_CELLS_LC...	Output_swing	669.2m	range 360m 600m
Important_CELLS_LC...	output noise: (USB, dBc/Hz)		
Important_CELLS_LC...	output noise; 1M; (USB,dBc/Hz)	-116.3	

2) Control Voltage of 1 Volts



Test	Output	Nominal	Spec	Weight	Pass/Fail
Important_CELLS_LC...	Output_Frequency	3.191G	range 2.8G 3.5G		pass
Important_CELLS_LC...	Output_swing	667.9m	range 360m 600m		fail
Important_CELLS_LC...	output noise: (USB, dBc/Hz)				
Important_CELLS_LC...	output noise; 1M; (USB,dBc/Hz)	-115.2			

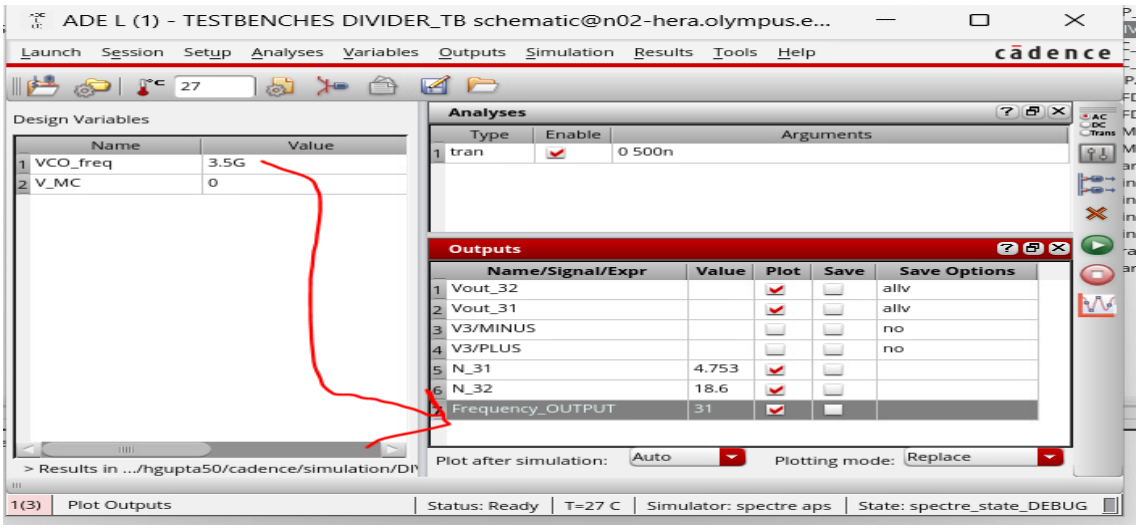
3) Kvco Characterization:
In this test Vco frequency was monitored vs control Voltage in order to get the Kvco value which was used in the loop filter and charge pump calculations.



B) Divider Simulation Results (Works till 3.5 GHz)

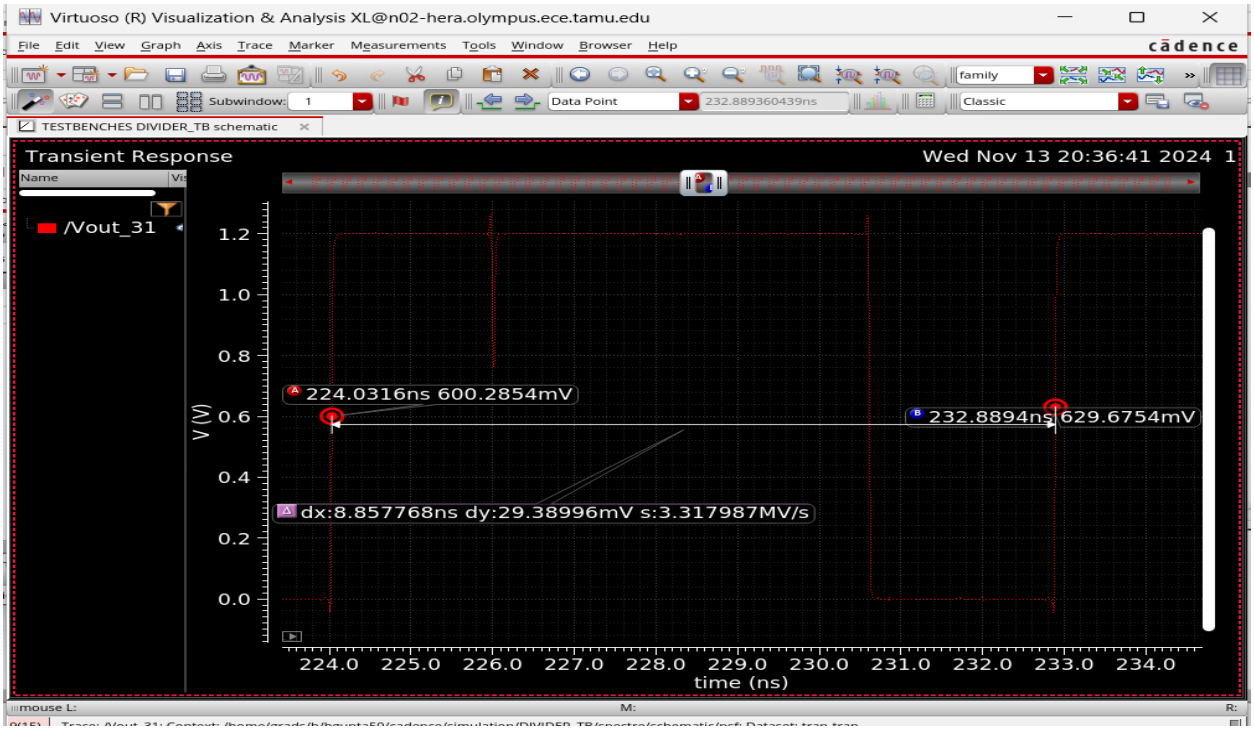
TSPC based D FlipFlop is tested on 31/32 dual modulus architecture.

Simulation Results of Modulus Control of zero, which will divider ratio of 31.



Where frequency output was ratio of 3.5 GHz and divider output frequency computed using below calculator expression.

(3.5e+09 / value(freq(v("/Vout_32" ?result "tran") "rising" ?xName "time"? mode "auto" ?threshold 0.0) 4e-07))

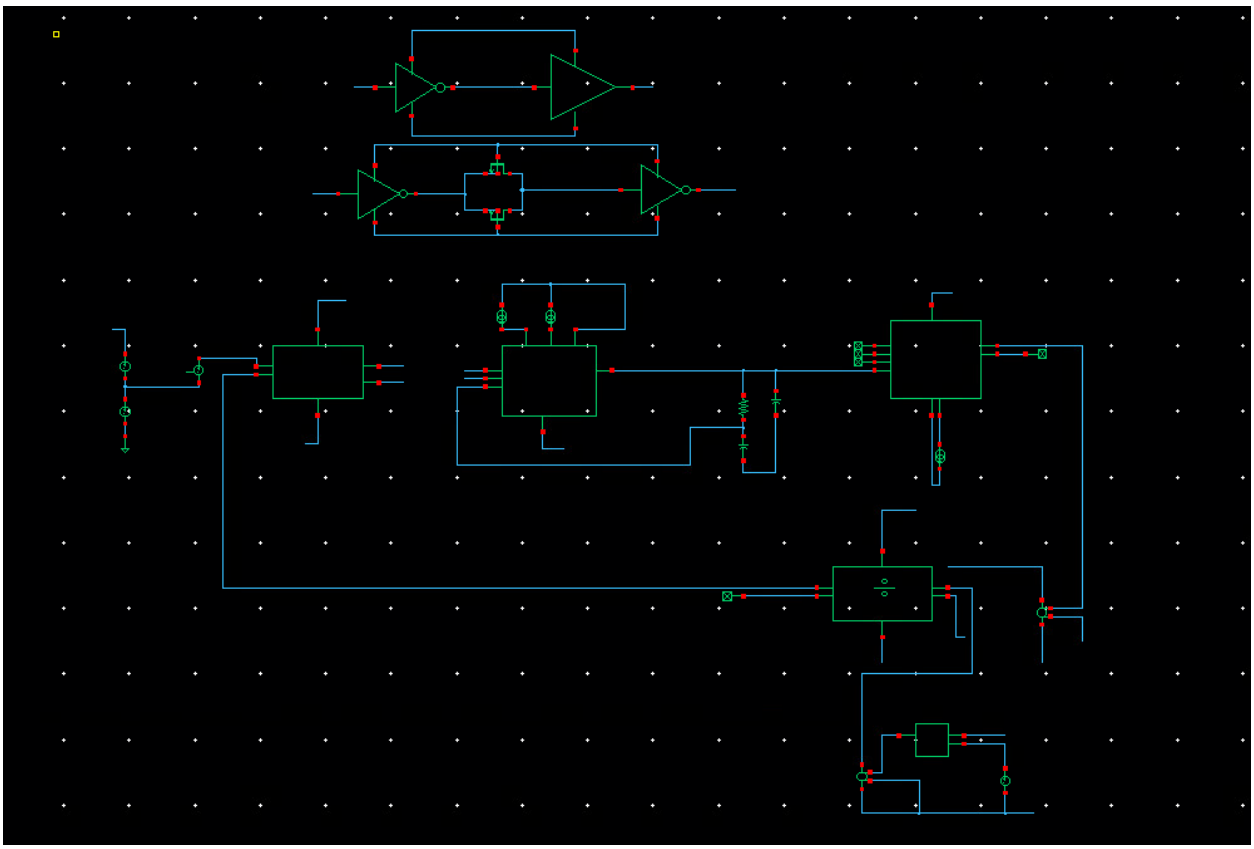


Pulse Width = 31* (Time-period of 3.5 GHz clock)

C) TOP Level Testbench and Simulations results:

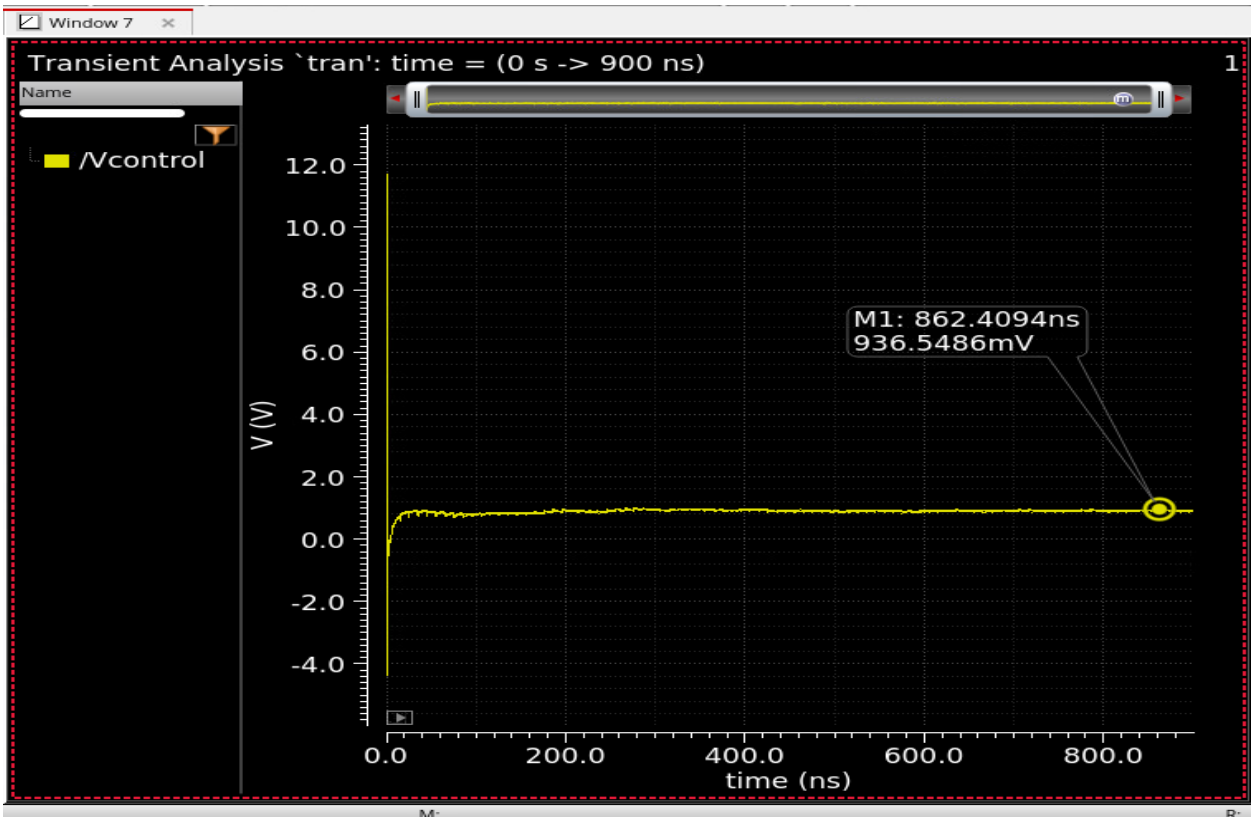
This testbench was used to see the locking behavior of PLL with MOD=1 which means divider ratio of 32 and VOUT Frequency of 3.2 GHz as Fref was 100kHz.

Testbench:

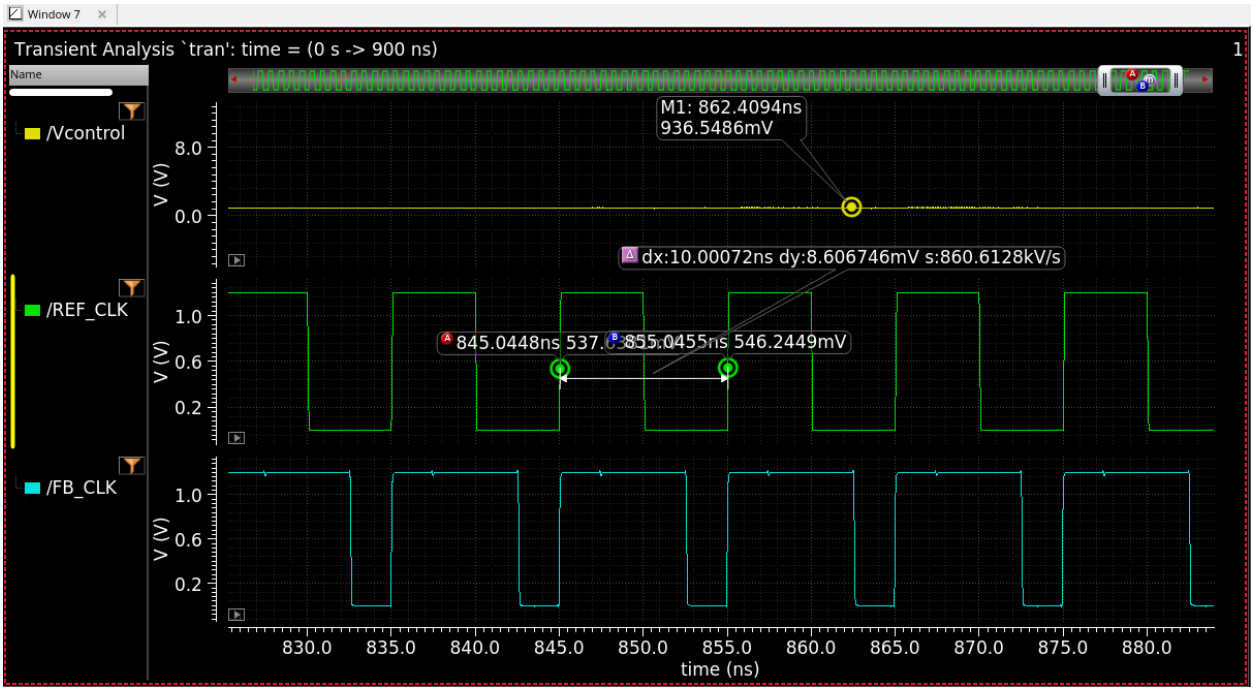


Simulation Results:

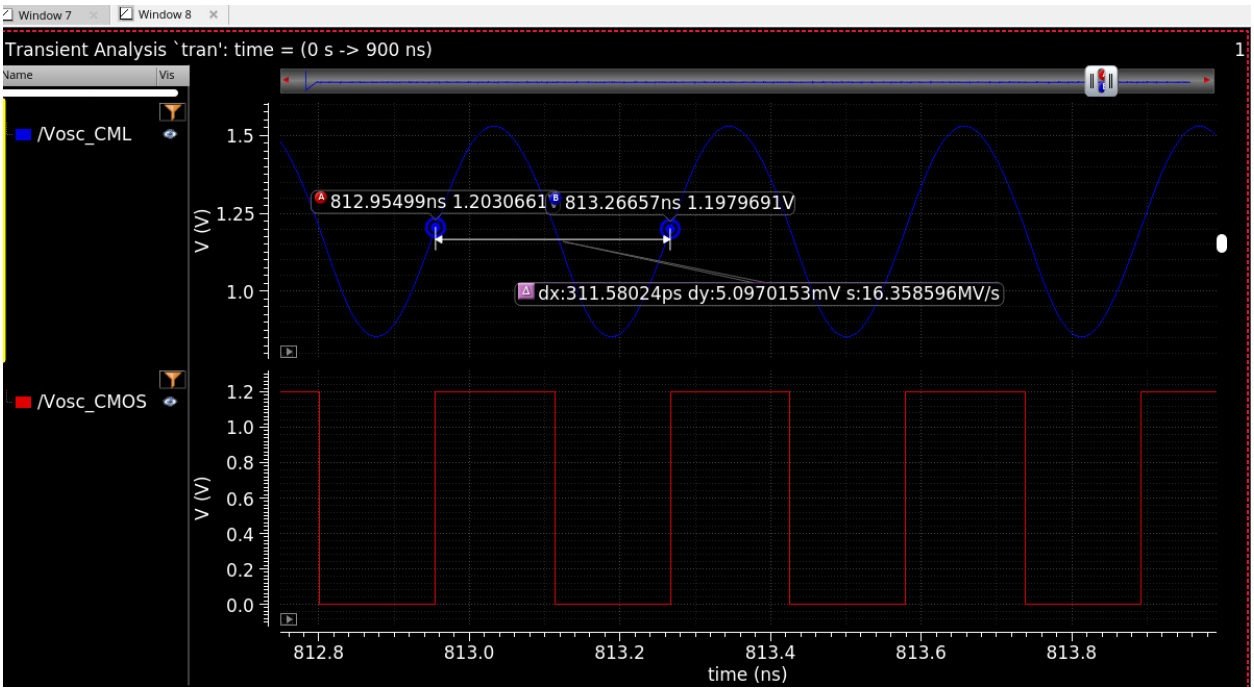
Control Voltage:



Phase & Frequency Locking of the Ref clock and FB clock:



Output of the Oscillator & Input of the Divider (Vosc_CML & Vosc_CMOS):

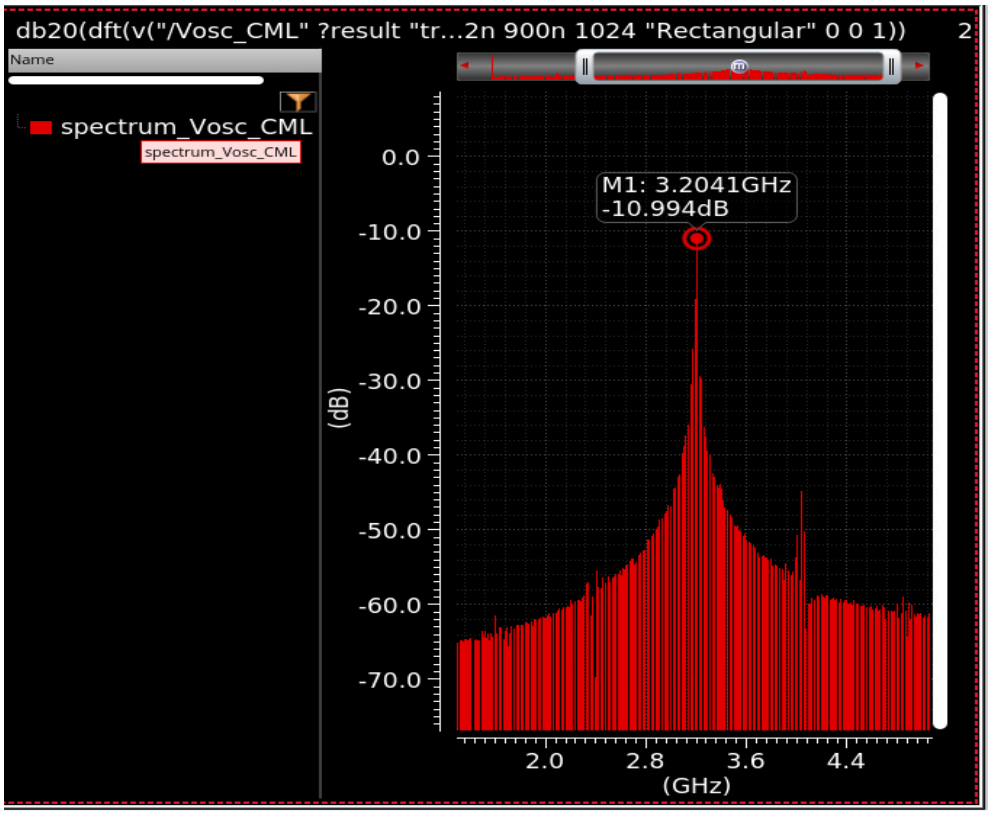


11 rows

Test	Output	Nominal
Filter	Filter	Filter
ECEN620_PROJECT_TB_TOP_TB_1	N_31	32
ECEN620_PROJECT_TB_TOP_TB_1	/Vosc_CML	
ECEN620_PROJECT_TB_TOP_TB_1	/FB_CLK	
ECEN620_PROJECT_TB_TOP_TB_1	/Vosc_CMOS	
ECEN620_PROJECT_TB_TOP_TB_1	N_32	32
ECEN620_PROJECT_TB_TOP_TB_1	frequency(v("/net8" ?...	eval err
ECEN620_PROJECT_TB_TOP_TB_1	/V_32	
ECEN620_PROJECT_TB_TOP_TB_1	CMOS_freq	3.202G
ECEN620_PROJECT_TB_TOP_TB_1	F_32	100M
ECEN620_PROJECT_TB_TOP_TB_1	FB_clk_freq	100M
ECEN620_PROJECT_TB_TOP_TB_1	CML_freq	3.202G

In the above snippet CMOS Frequency corresponds to the Oscillator frequency which locking around 3.202 GHz as expected.

PLL output Frequency Spectrum:



Parameters: alpha=100m			
1	proj620_VCO_T...	frequency(v("/V...	3.106G
Parameters: alpha=200m			
2	proj620_VCO_T...	frequency(v("/V...	3.113G
Parameters: alpha=300m			
3	proj620_VCO_T...	frequency(v("/V...	3.12G
Parameters: alpha=400m			
4	proj620_VCO_T...	frequency(v("/V...	3.127G
Parameters: alpha=500m			
5	proj620_VCO_T...	frequency(v("/V...	3.134G
Parameters: alpha=600m			
6	proj620_VCO_T...	frequency(v("/V...	3.142G
Parameters: alpha=700m			
7	proj620_VCO_T...	frequency(v("/V...	3.149G
Parameters: alpha=800m			
8	proj620_VCO_T...	frequency(v("/V...	3.156G
Parameters: alpha=900m			
9	proj620_VCO_T...	frequency(v("/V...	3.164G
Parameters: alpha=1			
10	proj620_VCO_T...	frequency(v("/V...	3.17G
Parameters: alpha=1.1			
11	proj620_VCO_T...	frequency(v("/V...	3.178G
Parameters: alpha=1.2			
12	proj620_VCO_T...	frequency(v("/V...	3.185G
Parameters: alpha=1.3			
13	proj620_VCO_T...	frequency(v("/V...	3.193G
Parameters: alpha=1.4			
14	proj620_VCO_T...	frequency(v("/V...	3.2G

For achieving the channel spacing spec, alpha parameter was used for the sigma-delta modulator along with the divider in order to achieve the fractional frequency ratios.

Performance Table:

Parameter	Results
Fout	3.2 GHz
Tuning Range	6 %
Fref	100 MHz
Phase Noise @ 1MHz	-116 dBc/Hz
Power (CP + LC Oscillator)	1.614 mW
Average Channel Spacing	7.143 MHz
Reference Spurs	-40 dBc
Single Ended Peak-Peak Swing	> 450mV (0.375*VDD)