Department of Computer Science & Engineering, IGIT, GGSIPU Delhi

Lab manual For COMPUTER ORGANISATION

(Version 1.0)

Odd Semester – MCA FIRST YEAR

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Course Objectives:

The objective of this course is to make familiar with the basic modules of a computer system and the understanding of their circuit details.

The lab work mainly covers the details of these circuits and there functioning.

LIST OF EXPERIEMENTS

1. **Verify the truth tables of AND, OR, NOT, NAND, NOR, XOR, and XNOR GATES.**
2. **Verify that NAND and NOR gates are universal gates.**
3. **Design a Half adder circuit and verify its truth table.**
4. **Design a Half subtractor circuit and verify its truth table.**
5. **Design a full adder circuit using half adders and verify its truth table.**
6. **Design a full subtractor circuit using half subtractor and verify its truth table.**
7. **Design a 2-bit binary incrementor using half adder circuit.**
8. **Design and implement a 3: 8 Decoder.**
9. **Design and implement a 4 X 1 Multiplexer.**
10. **Design and implement SR flip flop.**
11. **Design and implement D flip flop.**
12. **Design and implement JK flip flop.**
13. **Design and implement T flip flop.**
14. **Design and implement Master Slave flip flop.**

Experiment No. 1

<u>Aim</u>: To verify the truth tables of AND, OR, NOT, NAND, NOR, XOR, and XNOR GATES.

<u>Apparatus required</u>: Trainers kit with required integrated circuits and connecting wires.

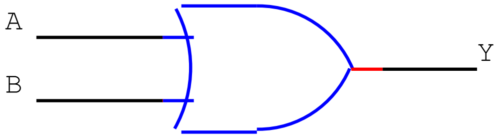
Theory:

A logic gate is a digital circuit that follows certain logical relationship between one or more than one input and the output. The input and the output are voltages which can be only on one of the possible two states. Thus the input or output may be low (called logic 0) or high (called logic 1). Some of the commonly used gates are:

OR GATE (2 INPUTS)

It is a logic gate based on logical OR operation. It is a logic gate in which either of the two inputs (A or B) is high (logic one) to get high (logic one) output.

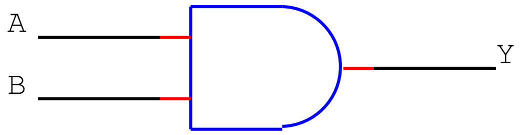
Y = A + B



AND GATE (2 INPUTS)

It is a logic gate based on logical and operation. It is a logic gate which gives high (logic 1) output when both inputs (A and B) are high.

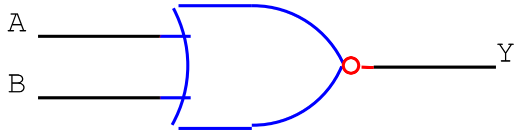
Y = A. B



NOR GATE (2 INPUTS)

It is a logic based on neither logical nor operation. It is a logic gate which gives high output only when both inputs are low.

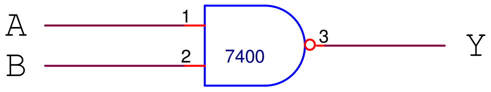
Y = (A + B)’



NAND GATE (2 INPUT)

It is a logic based on logical Nand operation. It is a logic gate which gives low output only when both inputs are high.

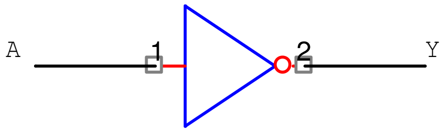
Y = (A. B)’



NOT GATE

It is a logic based on logical not operation. It is a logic gate which gives output (Y) the complement of the input (A). It is also known as inverter.

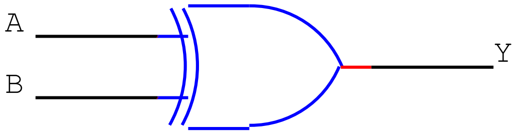
Y = A’



XOR GATE (2 INPUT)

It is a logic gate based on exclusive or operation. It is a logic gate which yields a high output when inputs are different and low output when both the inputs are same.

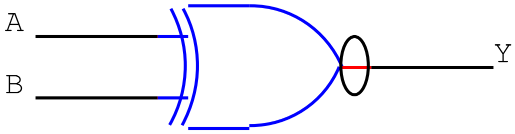
Y = A’B + AB’



X-NOR GATE

It is a logic gate based on exclusive nor gate. It is a logic gate which yields a high output when both inputs are same and low output when both inputs are different.

Y = (A’B + AB’)’



Procedure:

1. Make connections on trainer kit for a required gate say AND gate.

2. Connect the terminals 2 and 3 of the AND gate IC on trainer kit to input terminals (1 and 2 Pin) and output to pin no. 3. (i.e. the required LEDs to required pin nos.)

3. Connect the pin no.7 to ground and pin no.14 to the supply (Vcc). Switch on the trainer kit.

4. Observe the output of the gate for various sets of inputs. Note the observations.

5. Repeat all the above steps or all other gates using the appropriate IC and note the observation.

Observations:

(1) AND GATE

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(2) OR GATE

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(3) NAND GATE

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(4) NOR GATE

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

(5) XOR GATE

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

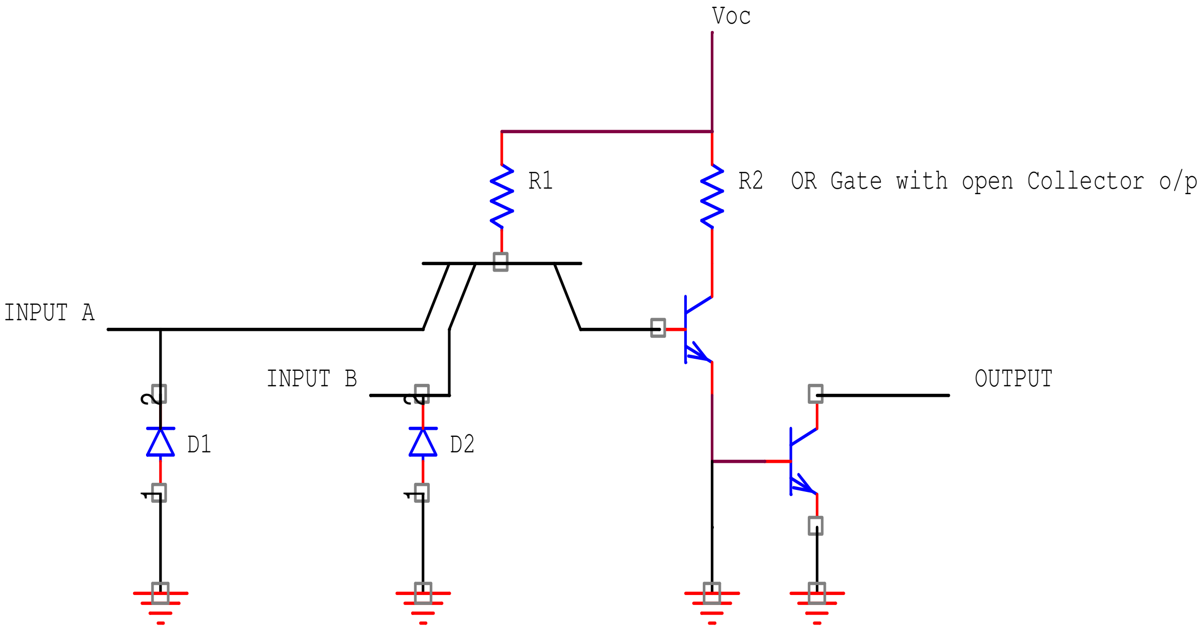
(6) XNOR GATE

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

(7) NOT GATE

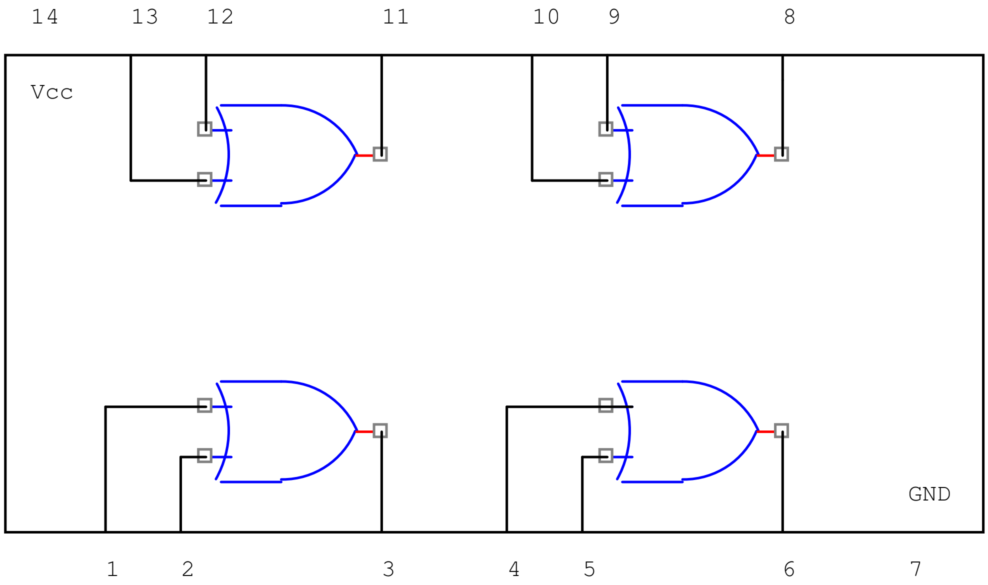
A	Y
0	1
1	0

QUAD 2 I/P OR GATE (7432)



INTERNAL CIRCUIT

14 PIN DIAGRAM (7432)



<u>Result:</u> Truth tables were verified for AND, OR, NAND, NOR, XOR, XNOR, NOT and BUFFER logic gates.

PRECAUTIONS:

1. All the IC's should be handled carefully.
2. All the connection should be tight.
3. Supply should be given after all connections are made.
4. Use IC plucker when remove the IC from Bread Board.

Experiment No. 2

Aim: Verify that NAND and NOR gates are universal gates.

Apparatus required: IC (No. 7400 and 7402), connecting wires,
and bread board.

Theory:

It is possible to design all the logic gates using NAND and NOR gates. So these two gates are called universal gates.

USING NAND GATE

1. **OR GATE**

   OR gate can be designed using 3 NAND gates. For OR gate with A and B as input and Y be the output then

   Y = A + B
   Y = ((A+B)')' = (A'.B')'   (using Demorgans Law)
   = (A NAND A) NAND (B NAND B)

2. **AND GATE**

   AND gate can be designed using 2 NAND gates.
   Here Y = A.B
   Y = ((A.B)')' = (A NAND B) NAND (A NAND B)

3. **NOT GATE**

   NOT gate can be designed using only 1 NAND gate. For NOT gate:
   Y = A'
   Y = ((A)')' = (A.A)'
   Y = A NAND A

4. **NOR GATE**

   NOR gate can be designed using 4 NAND gates. For NOR gate:
   Y = (A+B)'

Y = [(A NAND A) NAND (B NAND B)] NAND [(A NAND A) NAND (B NAND B)]

5. XOR GATE

XOR gate can be designed using 4 NAND gates. For XOR gates:
Y = A’B + AB’
Y = [(A NAND (A NAND B)) NAND (B NAND (A NAND B))]

6 XNOR GATE

XNOR gate can be designed using 5 NAND gates. Here
Y = [(A NAND (A NAND B)) NAND (B NAND (A NAND B))] NAND [(A NAND (A NAND B)) NAND (B NAND (A NAND B))]

USING NOR GATE

1. OR GATE

OR gate can be designed using 2 NOR gates. Here
Y = (A NOR B) NOR (A NOR B)

2. AND GATE

AND gate can be designed using 3 NOR gates. Here
Y = (A NOR A) NOR (B NOR B)

3. NOT GATE

NOT gate can be designed using only 1 NOR gate. For NOT gate:
Y = A NOR A

4. NAND GATE

NAND gate can be designed using 4 NOR gates.
Y = [(A NOR A) NOR (B NOR B)] NOR [(A NOR A) NOR (B NOR B)]

5. XOR GATE

XOR gate can be designed using 5 NOR gates. For XOR gates:
Y = [(A NOR (A NOR B)) NOR (B NOR (A NOR B))] NOR
[(A NOR (A NOR B)) NOR (B NOR (A NOR B))]

6. XNOR GATE

XNOR gate can be designed using 4 NOR gates. Here
Y = = [(A NOR (A NOR B)) NOR (B NOR (A NOR B))]

Procedure:

1. For designing the required gate from NAND or NOR gate, connect the required IC.

2. Connect the gate in the required manner with the help of connecting wires and make proper connections for ground (pin 7) and supply (pin 14).

3. Connect the inputs and outputs to the required LEDs. Switch on the supply.

4. Note the output for various combinations of input, note the observations and compare them with the observations of original gate.

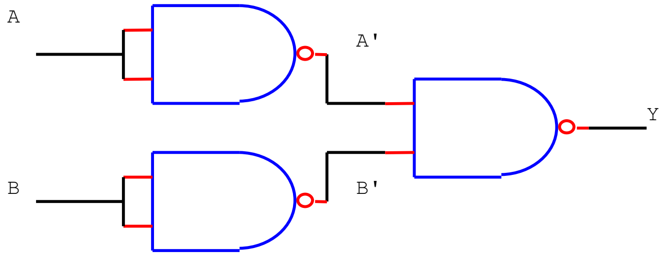
5. Repeat the above steps for all other gates and note the observations.

Observations:

DESIGN OF GATES USING NAND GATE

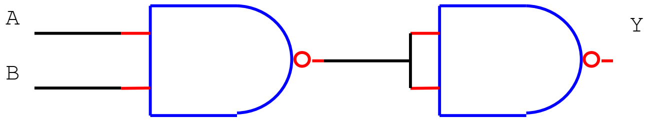
(1) **OR GATE**

Y = A + B



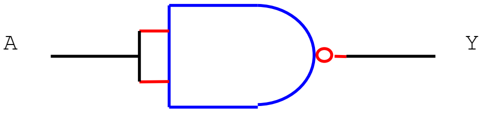
(2) **AND GATE**

Y = A. B



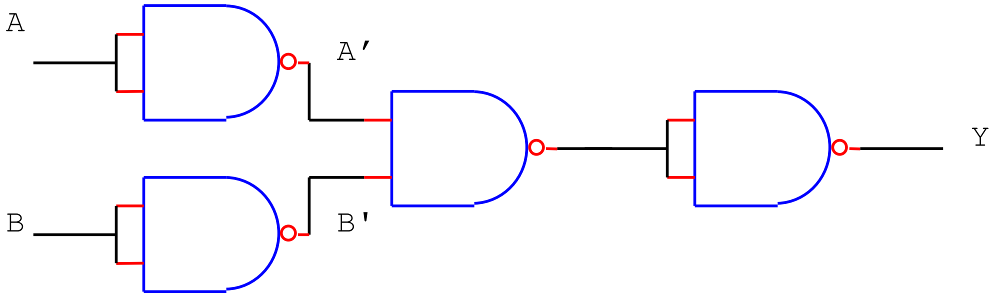
(3) **NOT GATE**

Y = A’



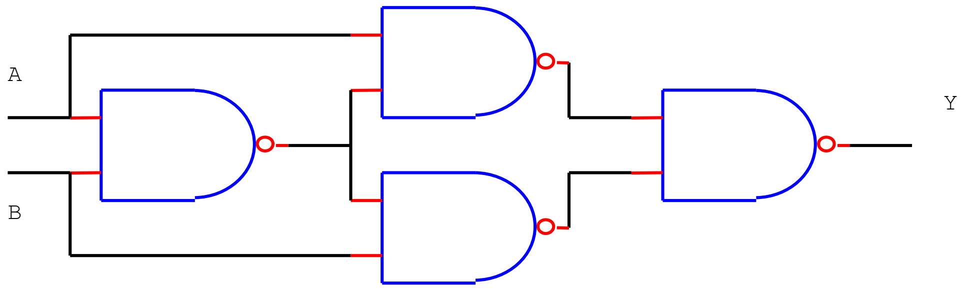
(4) **NOR GATE**

Y = (A + B)’



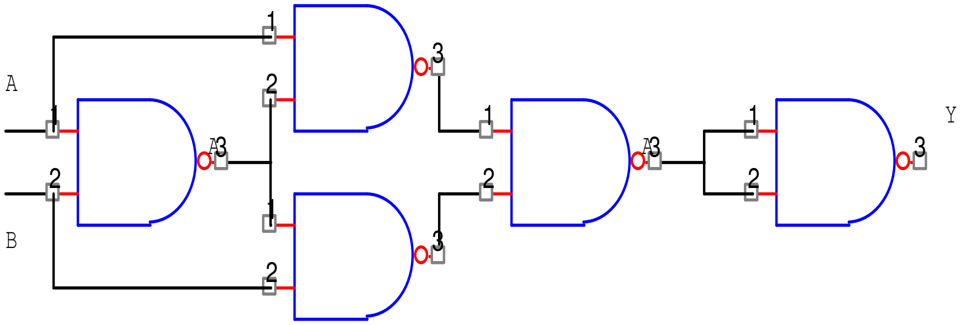
(5) **XOR GATE**

Y = A’B + AB’



(6) **XNOR GATE**

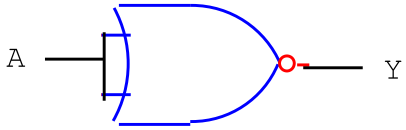
Y = (A’B + AB’)’



DESIGN OF BASIC GATES USING NOR GATE

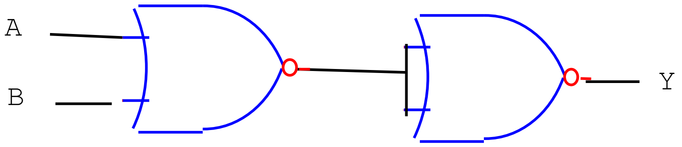
(1) **NOT GATE**

Y = A’



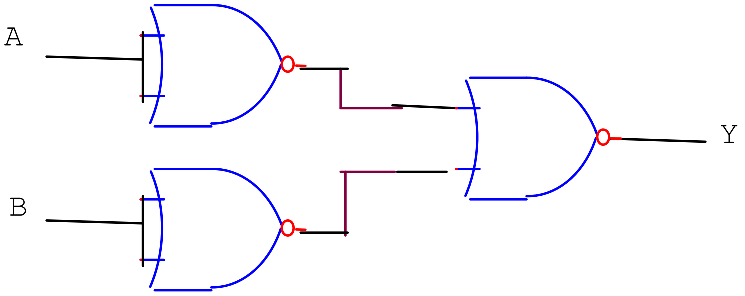
(2) **OR GATE**

Y = A + B



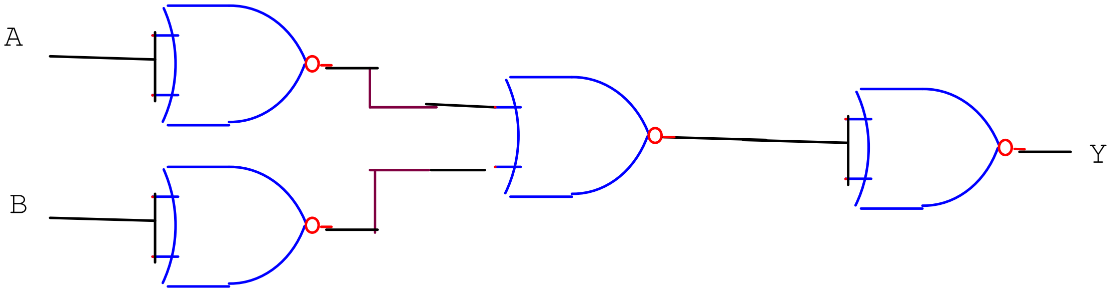
(3) **AND GATE**

Y = A.B



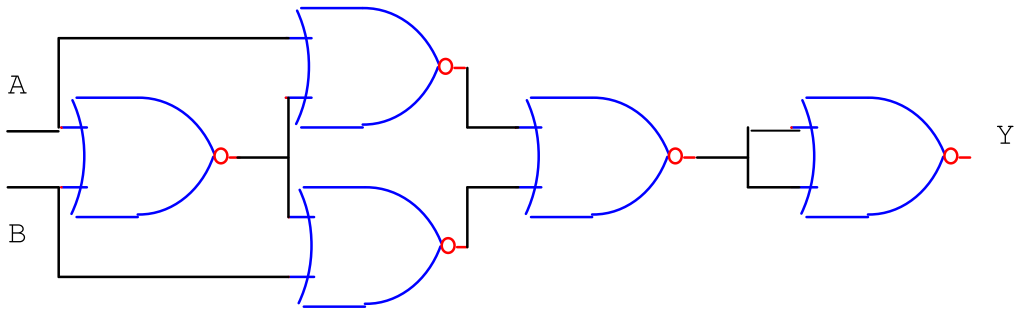
(4) **NAND GATE**

Y = (A.B)’



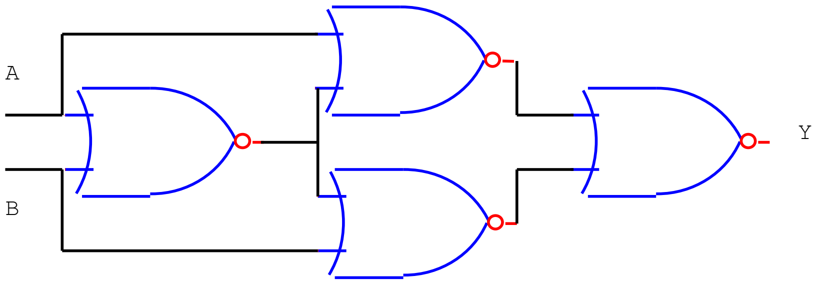
(5) **XOR GATE**

Y = A’B + AB’



(6) **XNOR GATE**

Y = (A’B + AB’)’



Result: All the gates (AND, OR, NOT, XOR, XNOR, NAND (NOR)) were designed using NAND and NOR gates and their truth tables verified.

PRECAUTIONS:

1. All the IC’s should be handled carefully.
2. All the connection should be tight.
3. Supply should be given after all connections are made.
4. Use IC plucker when remove the IC from Bread Board.

Experiment No. 3

Aim: To design a Half adder circuit and verify its truth table.

Apparatus required: IC (No. 7408 and 7486), connecting wires,
and trainers kit.

Theory:

HALF ADDER

A half adder is a combinational circuit that programs the addition of two bits. The circuit has two binary inputs and two binary outputs. The input variables (A and B) designate the augend and addend bits and the output variables (S and C) are sum and carry respectively. The C output is 1 only when both inputs are 1 and S represents the last significant bit of the sum.

The simplified Boolean functions for two outputs as obtained from the truth table are:

$S = A'B + AB'$
$C = AB$

Procedure:

1. For designing half adder, connect the required IC.

2. Connect the gates in the required manner with the help of connecting wires and make proper connections for ground (pin 7) and supply (pin 14).

3. Connect the input and output to required LEDs. Switch on the supply.

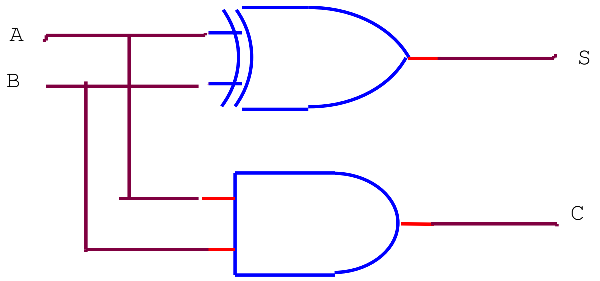
4. Note the output for various combinations of input variables.

Observations:

Truth table of Half Adder

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

HALF ADDER



Result: A half adder was designed and its truth table was verified.

PRECAUTIONS:

1. All the IC's should be handled carefully.

2. All the connection should be tight.

3. Supply should be given after all connections are made.

4. Use IC plucker when remove the IC from Bread Board.

Experiment No. 4

Aim: To design a Half subtractor circuit and verify its truth table.

Apparatus required: IC (No. 7432, 7404, 7408 and 7486), connecting wires, and trainers kit.

Theory:

HALF SUBTRACTOR

A half subtractor is a combinational circuit that programs the subtraction of two bits. The circuit has two binary inputs (A and B) and two binary outputs (D as difference and B_o as borrow).

The simplified Boolean functions for two outputs as obtained from the truth table are:

D = A’B + AB’
B_o= A’B

Procedure:

1. Connect the required ICs and make connections of gates in required manner and make proper connections for ground (pin 7) and supply (pin 14).

2. Connect the input and output to required LEDs. Switch on the supply.

3. Note the output for various combinations of input variables.

4. Repeat the steps for full adder and note down the observations.

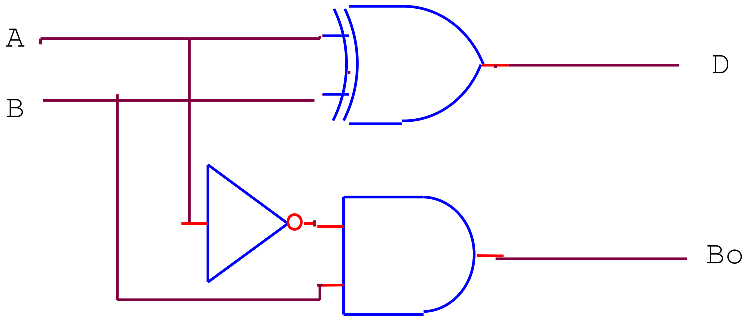
Observations:

Truth table of Half Subtractor

A	B	D	B_o
0	0	0	0
0	1	1	0

1	0	1	0
1	1	0	0

HALF SUBTRACTOR



Result: A half Subtractor was designed and its truth table was verified.

PRECAUTIONS:

1. All the IC’s should be handled carefully.

2. All the connection should be tight.

3. Supply should be given after all connections are made.

4. Use IC plucker when remove the IC from Bread Board.

Experiment No. 5

Aim: Design a full adder circuit using half adders and verify its truth table.

Apparatus required: IC (No. 7432, 7408, 7404 and 7486), connecting wires, and trainers kit.

Theory:

FULL ADDER

A full adder is a combinational circuit that performs the addition of 3 bits. The circuit has 3 input variables (A, B and C) and two output variables (S as sum and C as carry). The third input C represents the carry from previous lower significant position. The Boolean functions for two outputs obtained from truth table are:

$S = A' (B'C + BC') + A (B'C' + BC)$
$S = A \text{ XOR } B \text{ XOR } C$
and
$C_o = A'BC + AB'C + ABC' + ABC + ABC + ABC$
$\quad = AB (C + C') BC (A + A') +AC (B + B')$
$\quad = AB + BC + AC$

It can be implemented using two half adders and one OR gate. The output of first adder is sent as input to next half adder to obtain final sum.

Procedure:

1. For designing half adder, connect the required IC.

2. Connect the gates in the required manner with the help of connecting wires and make proper connections for ground (pin 7) and supply (pin 14).

3. Connect the input and output to required LEDs. Switch on the supply.

4. Note the output for various combinations of input variables.

5. Repeat the steps for full adder and note down the observations.

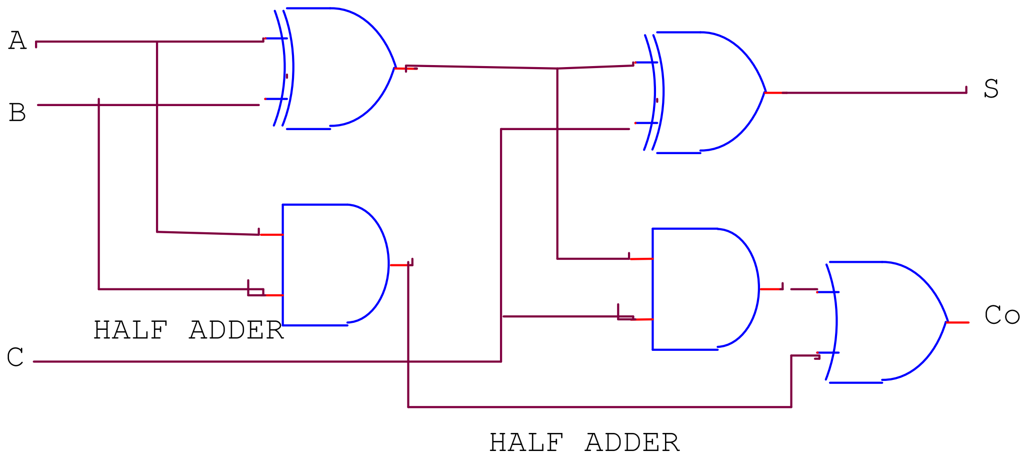
Observations:

Truth table of Full Adder

A	B	C	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FULL ADDER

FULL ADDER USING TWO HALF ADDERS



Result: A half adder was designed and its truth table was verified. A full adder was also designed using half adders and its truth table is verified.

PRECAUTIONS:

1. All the IC's should be handled carefully.
2. All the connection should be tight.
3. Supply should be given after all connections are made.
4. Use IC plucker when remove the IC from Bread Board.

CONCLUSION:

Using a half Adder we can realize the addition of two single bit numbers. Using Full Adder circuit, we can realize the addition of n single bit numbers.

Experiment No. 6

Aim: To. Design a full subtractor circuit using half subtractor and verify its truth table.

Apparatus required: IC (No. 7432, 7404, 7408 and 7486), connecting wires, and trainers kit.

Theory:

FULL SUBTRACTOR

A full subtractor is a combinational circuit that performs the subtraction of 3 bits. The circuit has 3 input variables (A, B and C) and two output variables (D as difference and B_o as borrow). The Boolean functions for two outputs obtained from truth table are:

S = A’ (B’C’ + BC) + A’ (B’C + BC’)
S = A XOR B XOR C
And
B_o = A’B’C + A’BC’ + A’BC
= A’C + A’B + BC

A full subtractor can also be designed using two subtractor and an OR gate

Procedure:

1. Connect the required ICs and make connections of gates in required manner and make proper connections for ground (pin 7) and supply (pin 14).

2. Connect the input and output to required LEDs. Switch on the supply.

3. Note the output for various combinations of input variables.

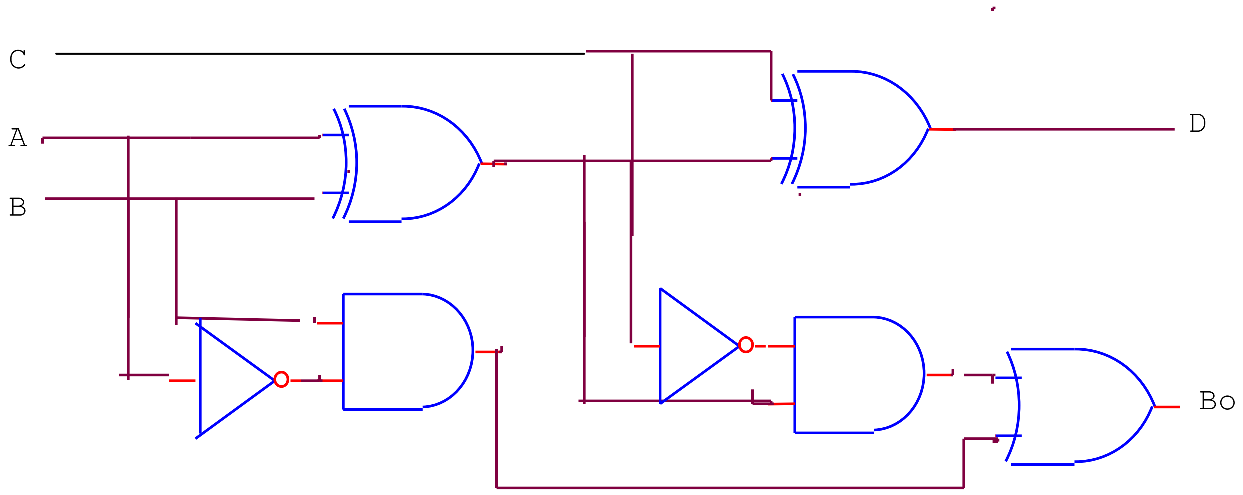
4. Repeat the steps for full adder and note down the observations.

Observations:

Truth table of Full Subtractor

A	B	C	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

FULL SUBTRACTOR USING TWO HALF SUBTRACTORS



Result: A full Subtractor was designed using half Subtractor and its Truth table is verified.

PRECAUTIONS:

1. All the IC’s should be handled carefully.

2. All the connection should be tight.

3. Supply should be given after all connections are made.

4. Use IC plucker when remove the IC from Bread Board.

Experiment No. 7

Aim: To implement Binary Incrementer

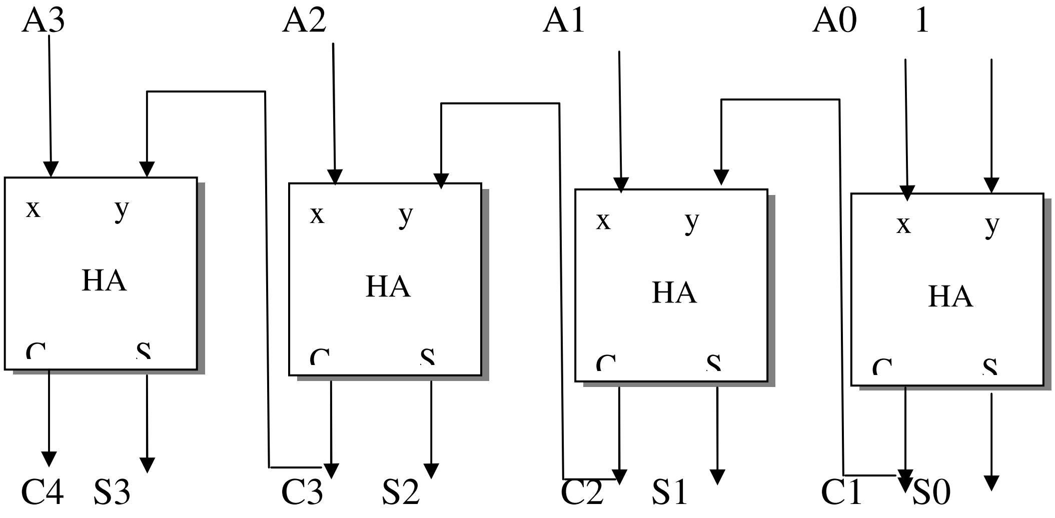
Apparatus Required:IC (No. 7432, 7404, 7408 and 7486), connecting wires, and trainers kit.

Theory:

BINARY INCREMENTER

The incrementer microopereation adds one to a number in a register.The circuit if incrementer is shown below: . One of the input to the least significant HA is connected to logic 1 and the other input is connected to the least significant bit of the number to be incremented. The output carry from one HA is connected to one of the inputs of the next higher order HA.

The circuit can be extended to n bit incrementer by extending the diagram to include n Has.



Procedure:

1. Connect the required ICs and make connections of gates in required manner and make proper connections for ground (pin 7) and supply (pin 14).

2. Connect the input and output to required LEDs. Switch on the supply.

3. Note the output for various combinations of input variables.

4. Repeat the steps for incrementer and note down the observations.

Observations:

Truth table of Incrementer

A3	A2	A1	A0	S3	S2	S1	S0
0	0	0	0	0	0	0	1
0	0	1	1	0	1	0	0
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	1	0	0	1	1	0	1
1	1	1	1	0	0	0	0

Result: A Incrementer was designed and its Truth table is verified.

PRECAUTIONS:

1. All the IC’s should be handled carefully.

2. All the connection should be tight.

3. Supply should be given after all connections are made.

4. Use IC plucker when remove the IC from Bread Board.

Experiment No. 8

Aim: To design and implement a 3: 8 Decoder

Apparatus required: Trainers kit with required integrated circuit and connecting wires.

Theory:

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. If the n bit coded information has unused combination the decoder may have fewer than 2^n output.

An example of decoder is a 3: 8 decoder. The three inputs are decoded into8 outputs each representing one of the minterms of the three input variables. The three inverters provide the complement of the inputs and each one of the eight AND gates generate one of the minterms. A particular application of this decoder is binary to octal conversion. The input variables represent a binary number and outputs represent the eight digits in octal number system. For each possible input combination, there are seven outputs that are equal to 0 and only one that is equal to 1. The output whose value is equal to 1 represents the minterms equivalent of the binary number presently available in input lines.

Procedure:

1. Connect the gates on the trainer kit in the required manner.

2. Make suitable connections for ground and supply. Connect input and output terminals to required LEDs.

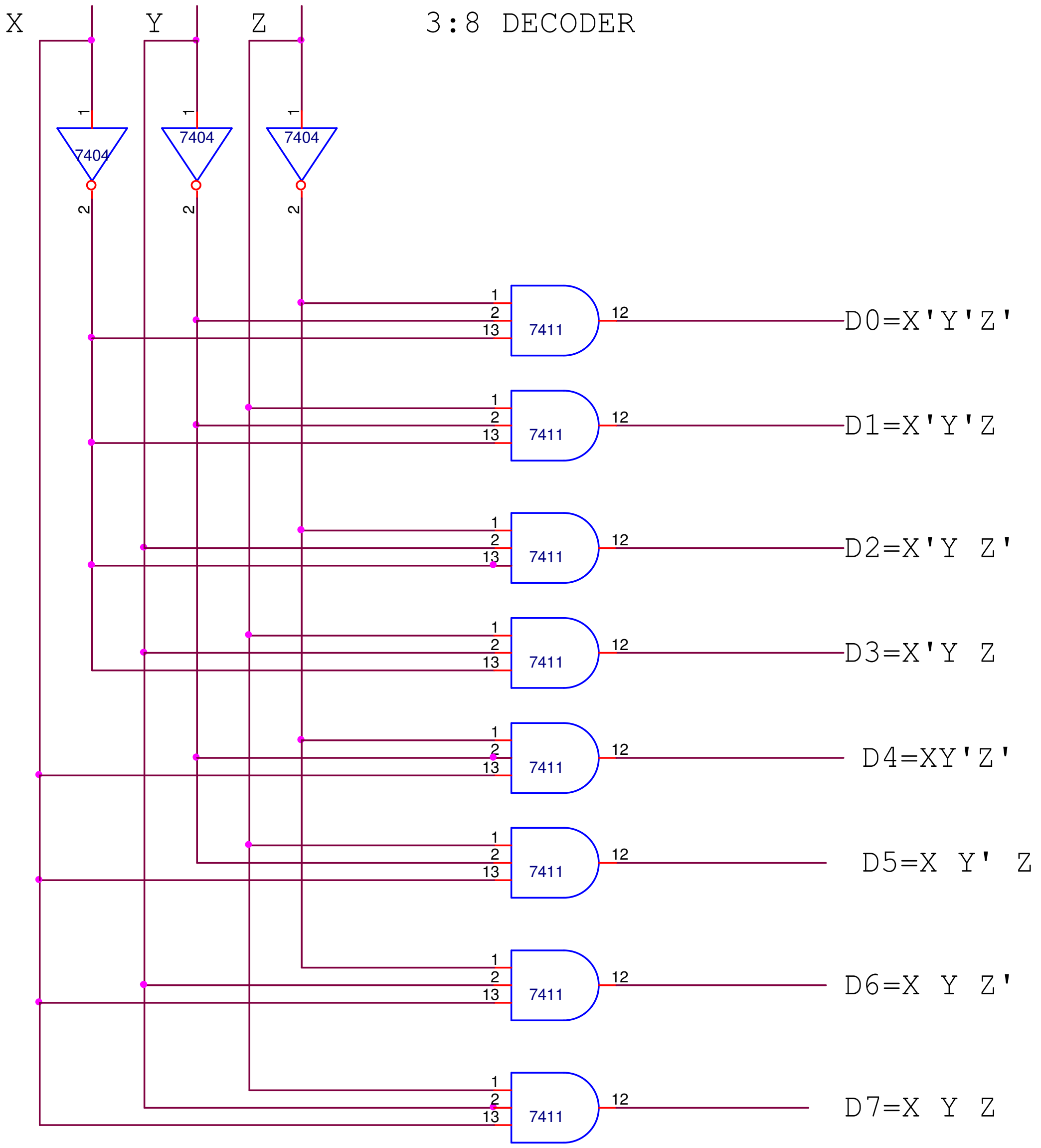
3. Switch ON the supply. For various combinations of input and selection lines, give the input.

4. Note down the values of output line for various combinations.

Observations:

TRUTH TABLE

INPUTS X Y Z	OUTPUTS							
	D0	D1	D2	D3	D4	D5	D6	D7
0 0 0	1	0	0	0	0	0	0	0
0 0 1	0	1	0	0	0	0	0	0
0 1 0	0	0	1	0	0	0	0	0
0 1 1	0	0	0	1	0	0	0	0
1 0 0	0	0	0	0	1	0	0	0
1 0 1	0	0	0	0	0	1	0	0
1 1 0	0	0	0	0	0	0	1	0
1 1 1	0	0	0	0	0	0	0	1



Result: A 3: 8 Decoder was designed and implemented using basics digital logic gates and its truth table was noted and verified.

PRECAUTIONS:

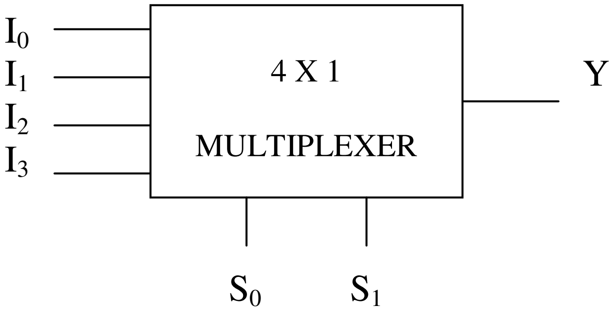
1. All the IC's should be handled carefully.
2. All the connection should be tight.
3. Supply should be given after all connections are made.
4. Use IC plucker when remove the IC from Bread Board.

Experiment No. 9

Aim: To design and implement a 4 X 1 Multiplexer.

Apparatus required: Trainers kit with required integrated circuit and connecting wires.

Theory:



A multiplexer is a special combinational circuit that is one of the most widely used standard circuit in digital design. The multiplexer is a logic circuit that gates one out of several inputs to a single output. The input selected by a set of select inputs. Generally, for 2^n input lines there is one output and n selection lines. Depending upon the digital code applied at the selected input, on out of n data sources is selected and transmitted to a single output channel.

In a 4 X 1 multiplexer, there are 4 input lines (I_0, I_1, I_2 and I_3), 2 selection lines (S_0 and S_1) and one output line (Y). Only one of the inputs is transferred to output depending upon the selection line value. It is implemented using AND gates and OR gate.

Procedure:

1. Connect the gates on the trainer kit in the required manner.

2. Make suitable connections for ground and supply. Connect input and output terminals to required LEDs.

3. Switch ON the supply. For various combinations of input and selection lines, give the input.

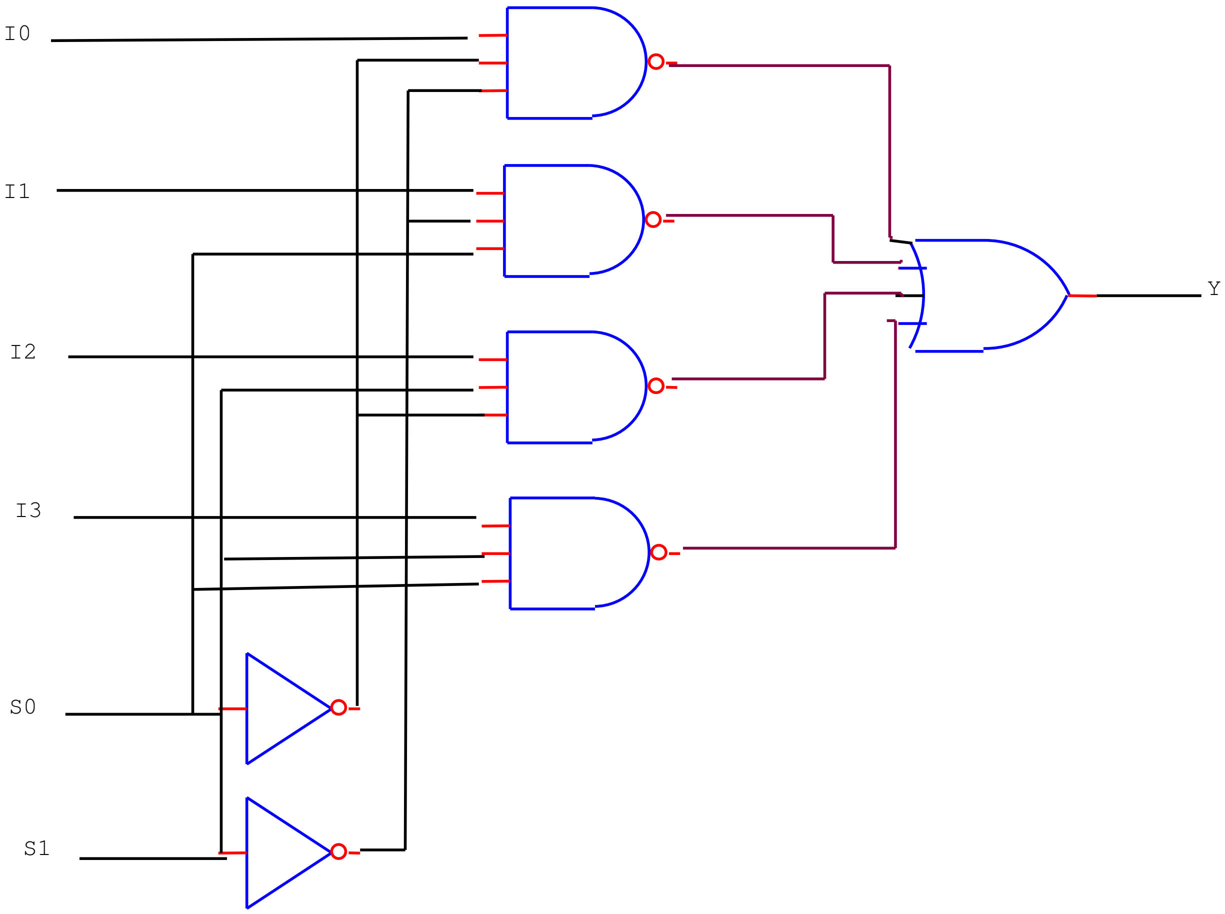
4. Note down the values of output line for various combinations.

Observations:

TRUTH TABLE

S_0	S_1	I_0	I_1	I_2	I_3
0	0	1	0	0	0
1	0	0	1	0	0
0	1	0	0	1	0
1	1	0	0	0	1

4 X 1 MULTIPLEXER



Result: A 4 X 1 multiplexer was designed and implemented using basic digital logic gates and its truth table was noted and verified.

PRECAUTIONS:

1. All the IC's should be handled carefully.
2. All the connection should be tight.
3. Supply should be given after all connections are made.
4. Use IC plucker when remove the IC from Bread Board.

Experiment No. 10

Aim: To design and implement **SR** flip flop.

Apparatus required: Trainers kit with required integrated circuit and connecting wires.

Theory:

A basic digital memory circuit is known as flip flop. It has two stable states as the 1 or set state and 0 or reset state. It can be obtained using NAND or NOR gates. There are various types of flip flops. Some of them are:

1. SR flip flop: This type of flip flop consists of S, R inputs along with clocked pulse input, also the present value of output depends on previous output values. When the clock pulse is 1, then the circuit responds to inputs S and R else the gates G_3 and G_1 inhibited. The combination of S = R = 1 is not allowed as it is indeterminate because here both Q and Q' attain same value.

Procedure:

1. For the required flip flop say SR flip flop connect the gates in the required manner.

2. Make the input and output connections in required manner and make connections for supply and ground.

3. Switch on the supply. For the various combinations of input variables more the value of outputs.

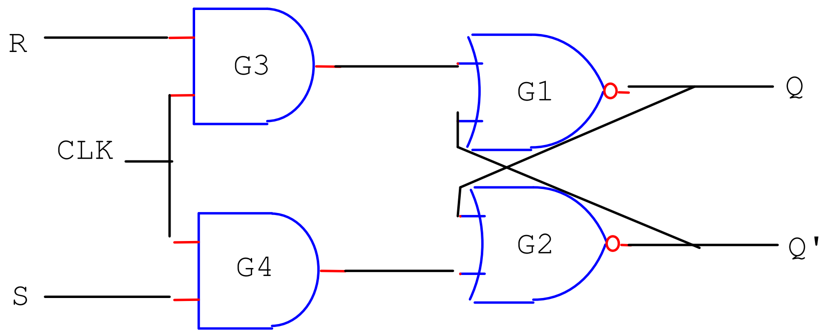
4. Repeat the above steps for various flip flops and note the observations for various combinations of input variables.

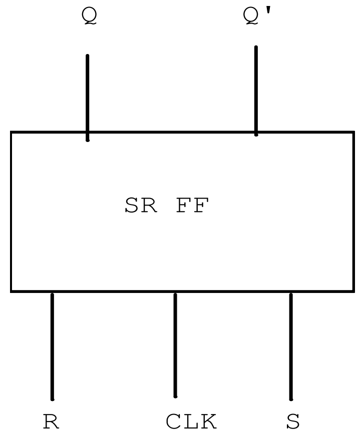
Observations:

TRUTH TABLE FOR **SR FLIP FLOP**

Q_t	S	R	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	*
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	*

SR FLIP FLOP





Result: SR flip flop were designed and implemented and their characteristic tables were noted.

PRECAUTIONS:

1. All the IC's should be handled carefully.

2. All the connection should be tight.

3. Supply should be given after all connections are made.

4. Use IC plucker when remove the IC from Bread Board.

Experiment No. 11

Aim: To design and implement **D** flip flop.

Apparatus required: Trainers kit with required integrated circuit and connecting wires.

Theory:

A basic digital memory circuit is known as flip flop. It has two stable states as the 1 or set state and 0 or reset state. It can be obtained using NAND or NOR gates. There are various types of flip flops. Some of them are:

1. D flip flop: In this type of flip flop, there is only one input referred to as D input or data input. The output Q_{th} is equal to input D_t when clock pulse is there. This is equivalent to saying that the input data appears at the output end of clock pulse. Thus the transfer of data from the input to the output is delayed and hence named as delay (D) flip flop. The D type flip flop is either used as a delay device or a latch to store 1 bit of binary information.

Procedure:

5. For the required flip flop say SR flip flop connect the gates in the required manner.

6. Make the input and output connections in required manner and make connections for supply and ground.

7. Switch on the supply. For the various combinations of input variables more the value of outputs.

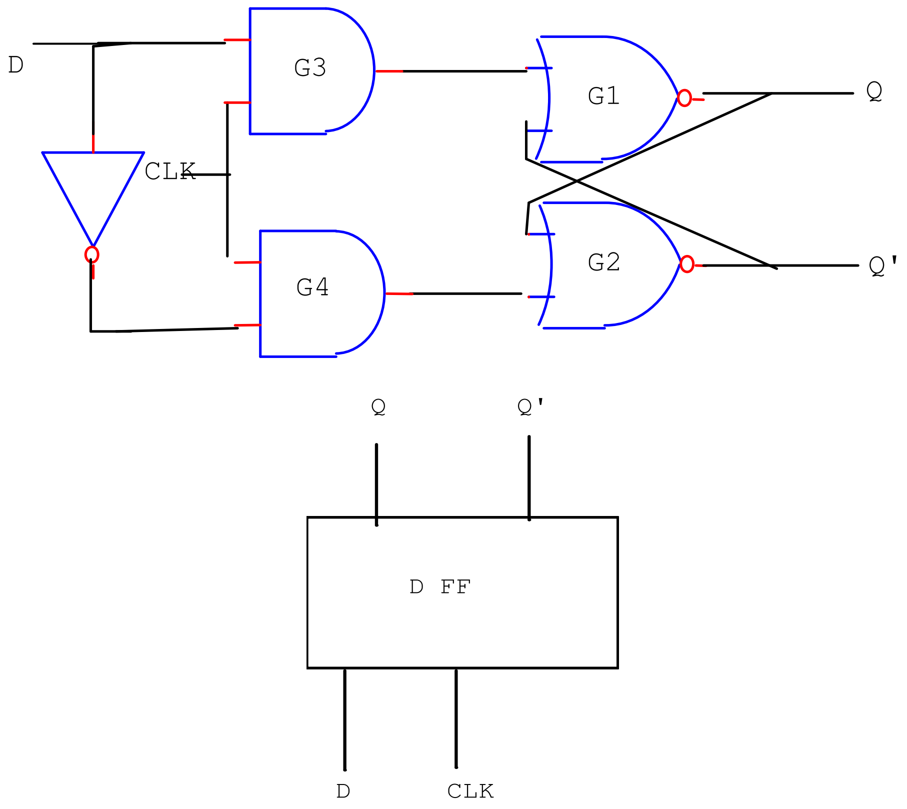
8. Repeat the above steps for various flip flops and note the observations for various combinations of input variables.

Observations:

TRUTH TABLE FOR **D FLIP FLOP**

Q_t	D	Q_{t+1}
0	0	0
0	1	1
1	0	0
1	1	1

D FLIP FLOP



Result: D flip flop was designed and implemented and their characteristic tables were noted.

PRECAUTIONS:

1. All the IC's should be handled carefully.

2. All the connection should be tight.

3. Supply should be given after all connections are made.

4. Use IC plucker when remove the IC from Bread Board.

Experiment No. 12

Aim: To design and implement JK flip flop.

Apparatus required: Trainers kit with required integrated circuit
and connecting wires.

Theory:

A basic digital memory circuit is known as flip flop. It has two stable states as the 1 or set state and 0 or reset state. It can be obtained using NAND or NOR gates. There are various types of flip flops. Some of them are:

1. SR flip flop: This type of flip flop consists of S, R inputs along with clocked pulse input, also the present value of output depends on previous output values. When the clock pulse is 1, then the circuit responds to inputs S and R else the gates G_3 and G_1 inhibited. The combination of S = R = 1 is not allowed as it is indeterminate because here both Q and Q' attain same value.

2. JK flip flop: This is another kind of flip flop. The data inputs are J and K which are AND ed with Q and Q' to obtain S and R inputs (if try to implement it as SR flip flop). In the gates G_3 and G_1, J and K inputs are AND ed with clock pulse and previous outputs. Truth table for JK flip flop is prepared for all possible combinations of JK and for each combination both states of previous outputs have been considered.

Procedure:

1 For the required flip flop say SR flip flop connect the gates in the required manner.

2 Make the input and output connections in required manner and make connections for supply and ground.

3 Switch on the supply. For the various combinations of input variables more the value of outputs.

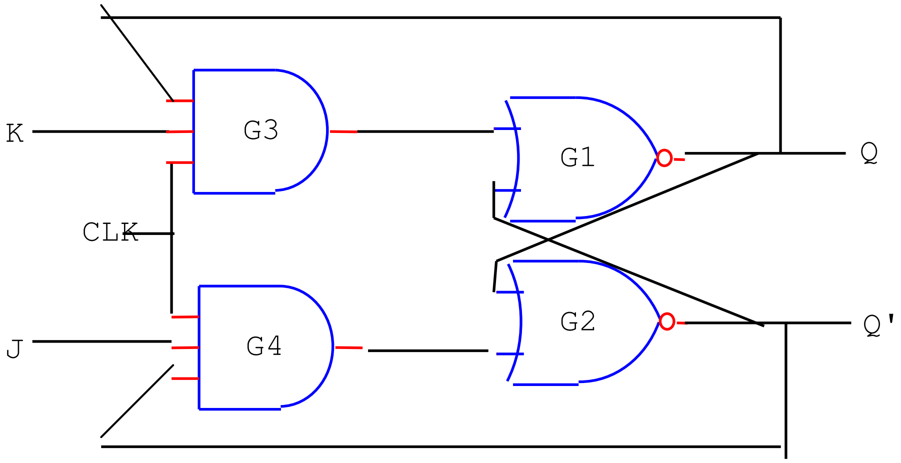
4 Repeat the above steps for various flip flops and note the observations for various combinations of input variables.

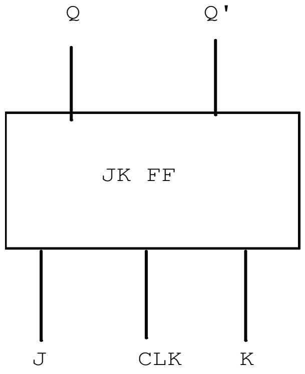
Observations:

TRUTH TABLE FOR **JK FLIP FLOP**

Q_t	J	K	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

JK FLIP FLOP





Result: JK flip flop was designed and implemented and their characteristic tables were noted.

PRECAUTIONS:

1. All the IC's should be handled carefully.

2. All the connection should be tight.

3. Supply should be given after all connections are made.

4. Use IC plucker when remove the IC from Bread Board.

Experiment No. 13

Aim: To design and implement T flip flop.

Apparatus required: Trainers kit with required integrated circuit and connecting wires.

Theory:

A basic digital memory circuit is known as flip flop. It has two stable states as the 1 or set state and 0 or reset state. It can be obtained using NAND or NOR gates. There are various types of flip flops. Some of them are:

1. SR flip flop: This type of flip flop consists of S, R inputs along with clocked pulse input, also the present value of output depends on previous output values. When the clock pulse is 1, then the circuit responds to inputs S and R else the gates G_3 and G_1 inhibited. The combination of S = R = 1 is not allowed as it is indeterminate because here both Q and Q' attain same value.

2. T flip flop: In this type of flip flop, there is only one input referred to as T input. When T = 0, there is no change in the value of output from previous value but when T = 1, the output value toggles from 0 to 1 or 1 to 0. During this period it acts as a toggle switch.

Procedure:

1. For the required flip flop say SR flip flop connect the gates in the required manner.

2. Make the input and output connections in required manner and make connections for supply and ground.

3. Switch on the supply. For the various combinations of input variables more the value of outputs.

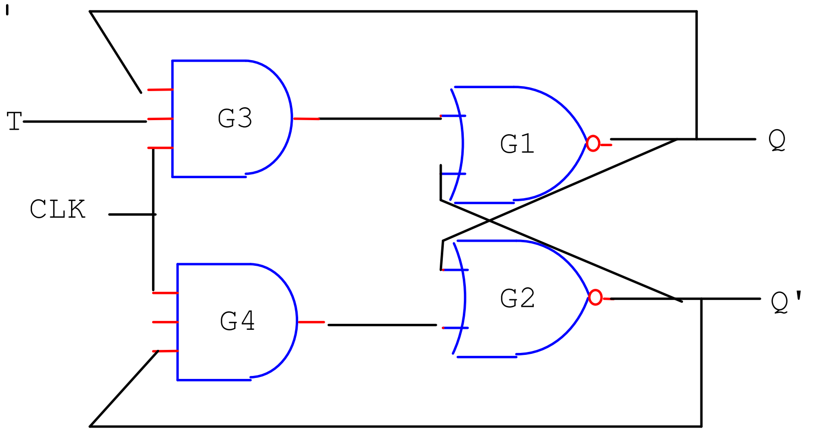
4. Repeat the above steps for various flip flops and note the observations for various combinations of input variables.

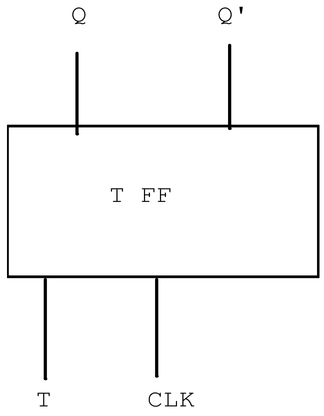
Observations:

TRUTH TABLE FOR **T FLIP FLOP**

Q_t	T	Q_{t+1}
0	0	0
0	1	1
1	0	1
1	1	0

T FLIP FLOP





Result: T flip flop was designed and implemented and their characteristic tables were noted.

PRECAUTIONS:

1. All the IC's should be handled carefully.
2. All the connection should be tight.
3. Supply should be given after all connections are made.
4. Use IC plucker when remove the IC from Bread Board.

Experiment No. 14

Aim: To design and implement JKMS flip flop.

Apparatus required: Trainers kit with required integrated circuit and connecting wires.

Theory:

A basic digital memory circuit is known as flip flop. It has two stable states as the 1 or set state and 0 or reset state. It can be obtained using NAND or NOR gates. There are various types of flip flops. Some of them are:

1. SR flip flop: This type of flip flop consists of S, R inputs along with clocked pulse input, also the present value of output depends on previous output values. When the clock pulse is 1, then the circuit responds to inputs S and R else the gates G_3 and G_1 inhibited. The combination of S = R = 1 is not allowed as it is indeterminate because here both Q and Q' attain same value.

2. JK flip flop: This is another kind of flip flop. The data inputs are J and K which are AND ed with Q and Q' to obtain S and R inputs (if try to implement it as SR flip flop). In the gates G_3 and G_1, J and K inputs are AND ed with clock pulse and previous outputs. Truth table for JK flip flop is prepared for all possible combinations of JK and for each combination both states of previous outputs have been considered.

3. The Master slave JK flip flop: A Master Slave JK flip flop is a cascade of two SR flip flops with feedback from outputs of the second to inputs of first. Positive clock pulses are applied to first flip flop and are inverted to be applied to second flip flop. When CK = 1, the first flip flop is enabled and second is inhibited and second is enabled. Hence the outputs of second flip flop follow the output of first one. Hence second one is referred as slave and first one as master. Hence this configuration is called Master slave flip flop.

Procedure:

1. For the required flip flop say SR flip flop connect the gates in the required manner.

2. Make the input and output connections in required manner and make connections for supply and ground.

3. Switch on the supply. For the various combinations of input variables more the value of outputs.

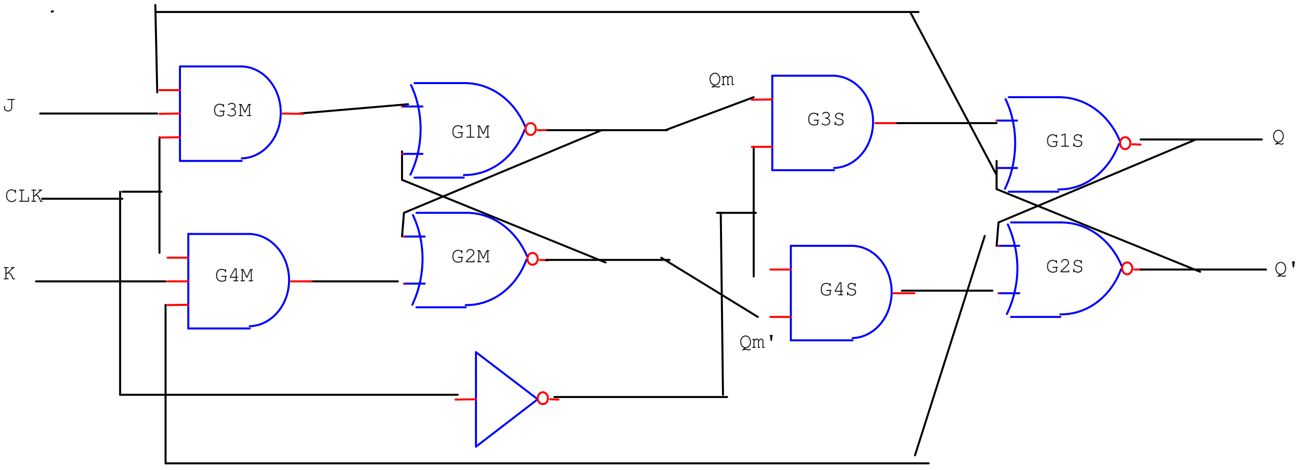
4. Repeat the above steps for various flip flops and note the observations for various combinations of input variables.

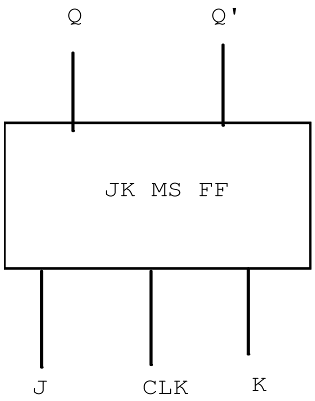
Observations:

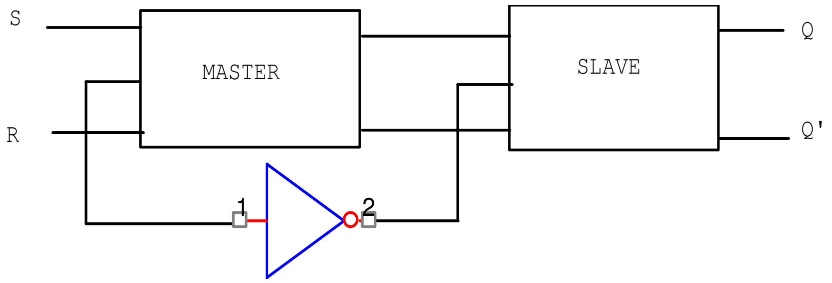
TRUTH TABLE FOR **MS-JK FLIP FLOP**

Q_t	J	K	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

MASTER SLAVE JK FLIP FLOP







Result: JKMS flip flop was designed and implemented and their characteristic tables were noted.

PRECAUTIONS:

1. All the IC's should be handled carefully.

2. All the connection should be tight.

3. Supply should be given after all connections are made.

4. Use IC plucker when remove the IC from Bread Board.