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## Question 11

Match the logic gates in Column A with their equivalents in Column B.

Column-A	Column-B
1. AND GATE	P. XOR GATE
2. OR GATE	Q. XNOR GATE
3. NOT GATE	R. NAND GATE

**TABLE 11: Table-1**

- a) P-2, Q-4, R-1, S-3      b) P-4, Q-2, R-1, S-3  
c) P-2, Q-4, R-3, S-1      d) P-4, Q-2, R-3, S-1

## Question Analysis

The AND gate produces output 1 only when both inputs are 1. The NAND gate is the complement of AND. Hence,  $\text{NAND} = \text{NOT}(\text{AND})$ .

The XOR gate produces output 1 when inputs are different. The XNOR gate is the complement of XOR.

Using logical relationships:

$$Q = (A \cdot B)'$$

After comparing the logical behavior of each gate, the correct matching is:

$$P - 2, Q - 4, R - 3, S - 1$$

## Truth Table

AND Gate:  $Q = A \cdot B$

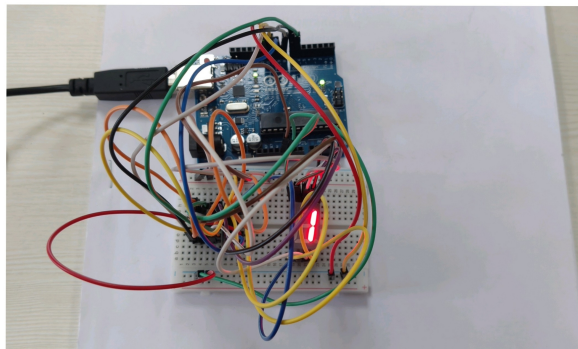
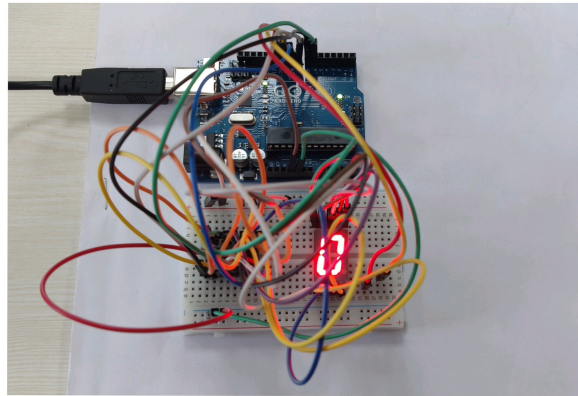
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

NAND Gate:  $Q = (A \cdot B)'$

A	B	NAND
0	0	1
0	1	1
1	0	1
1	1	0

## Hardware Implementation

The circuit is implemented using Arduino UNO and IC 7447. The logical output is displayed on a common anode 7-segment display.



## Required Components

- Arduino UNO
- IC 7447
- Common Anode 7-Segment
- Breadboard
- Jumper wires

## Pin Connections

Pin 16  $\rightarrow$  5V Pin 8  $\rightarrow$  GND Pin 3,4,5  $\rightarrow$  5V

Common Anode  $\rightarrow$  5V

Segments connected from 7447 output pins through resistors.

## Logic Description

The implemented logic verifies the NAND operation.

Expression:  $Q = (A \cdot B)'$

Output is LOW only when both inputs are HIGH.

## Conclusion

The experimental verification confirms the logical equivalence.

Hence the correct answer is verified successfully.