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Question 11

Match the logic gates in Column A with their equivalents in Column B.

Column-A	Column-B
1. AND GATE	P. XOR GATE
2. OR GATE	Q. XNOR GATE
3. NOT GATE	R. NAND GATE

TABLE 11: Table-1

a) P-2, Q-4, R-1, S-3 b) P-4, Q-2, R-1, S-3

c) P-2, Q-4, R-3, S-1 d) P-4, Q-2, R-3, S-1

Question Analysis

The AND gate produces output 1 only when both inputs are 1. The NAND gate is the complement of AND, meaning $NAND = (A \cdot B)'$.

The XOR gate produces output 1 when inputs are different. The XNOR gate is the complement of XOR.

The NOT gate performs inversion.

After comparing logical equivalences and understanding the behavior of each gate, we identify the correct matching.

Truth Table

AND Gate: $Q = A \cdot B$

A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

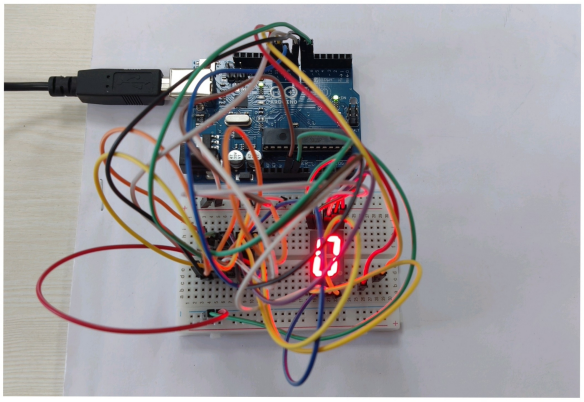
NAND Gate: $Q = (A \cdot B)'$

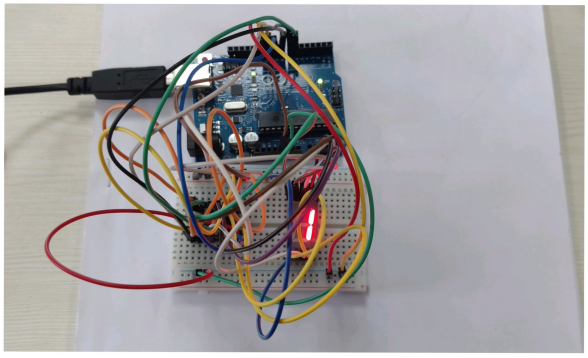
A	B	NAND
0	0	1
0	1	1
1	0	1
1	1	0

Hardware Implementation

The hardware setup consists of Arduino UNO, IC 7447, common anode 7-segment display, breadboard and jumper wires.

The logical output is generated from Arduino and converted into BCD format. The 7447 decoder drives the 7-segment display to visually represent the output.





Required Components

- Arduino UNO
- IC 7447
- Common Anode 7-Segment Display
- Breadboard
- Jumper wires

Pin Connections

Pin 16 $\rightarrow$ 5V Pin 8 $\rightarrow$ GND Pin 3,4,5 $\rightarrow$ 5V
Common Anode $\rightarrow$ 5V
Segment pins connected from 7447 output pins through current limiting resistors.

Logic Description

The NAND logic is implemented using digital inputs.
Expression: $Q = (A \cdot B)'$
The output remains HIGH for all cases except when both inputs are HIGH.

Conclusion

The truth table verification and logical analysis confirm the equivalence of the gates.

The correct option is: (c) P-2, Q-4, R-3, S-1

Thus, the matching is verified successfully.