

Homework Assignment 1

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EE19BTECH11038

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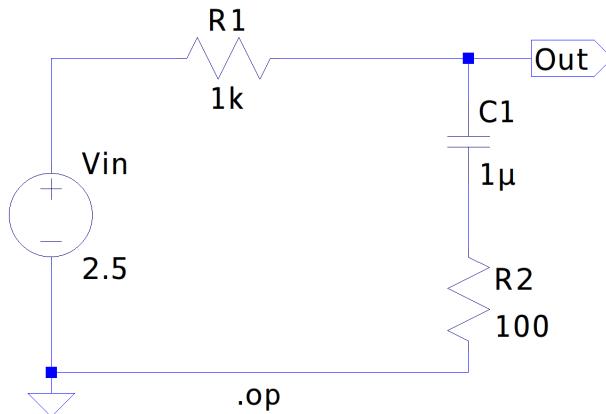
1 SPICE Analyses

(a)

SPICE Netlist

```
Vin N001 0 2.5
R1 Out N001 1k
C1 Out N002 1u
R2 N002 0 100
.op
.backanno
.end
```

TestBench



Operating point simulation results

--- Operating Point ---

V(n001):	2.5	voltage
V(out):	2.5	voltage
V(n002):	2.5e-016	voltage
I(C1):	2.5e-018	device_current
I(R2):	2.5e-018	device_current
I(R1):	-2.66454e-018	device_current
I(Vin):	-2.60209e-018	device_current

Operating point at V_{out} is 2.5V.

(b)

Applying KVL in the given circuit we get,

$$V_{in} = 1k\Omega xi + \frac{\int_0^t i dt}{1\mu} + 100xi$$

In Laplacian domain we get,

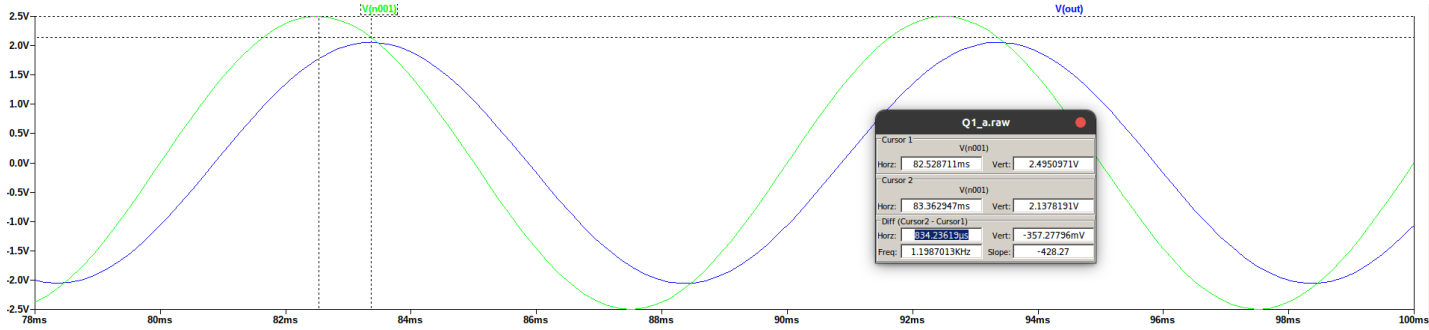
$$V_{in}(s) = \left(1100 + \frac{10^6}{s}\right) I(s)$$

$$\Rightarrow \frac{V_{out}(s)}{V_{in}(s)} = \frac{\left(100 + \frac{10^6}{s}\right) I(s)}{\left(1100 + \frac{10^6}{s}\right) I(s)}$$

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{s + 10000}{11s + 10000}$$

At $f = 100\text{Hz}$,

$$\frac{V_{out}(s)}{V_{in}(s)} = 0.82426 \angle -31.055^\circ$$

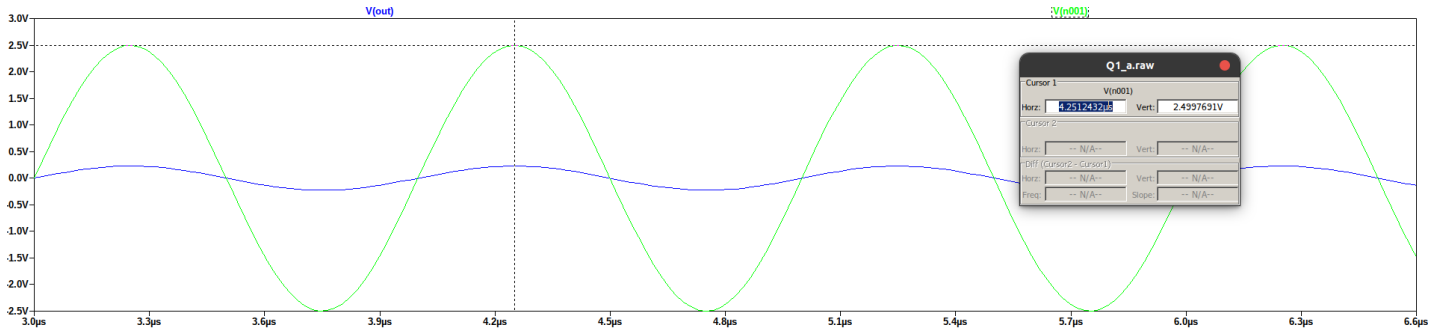


Observe that difference between peaks is $834\mu\text{s}$, and time period is 10ms (or $10000\mu\text{s}$), where V_{out} is lagging.

$$\Delta\phi = -360 \frac{834\mu\text{s}}{10000\mu\text{s}} \Rightarrow \Delta\phi = -30.024^\circ$$

At $f = 1\text{MHz}$,

$$\frac{V_{out}(s)}{V_{in}(s)} = 0.0909 \angle -0.0829^\circ$$



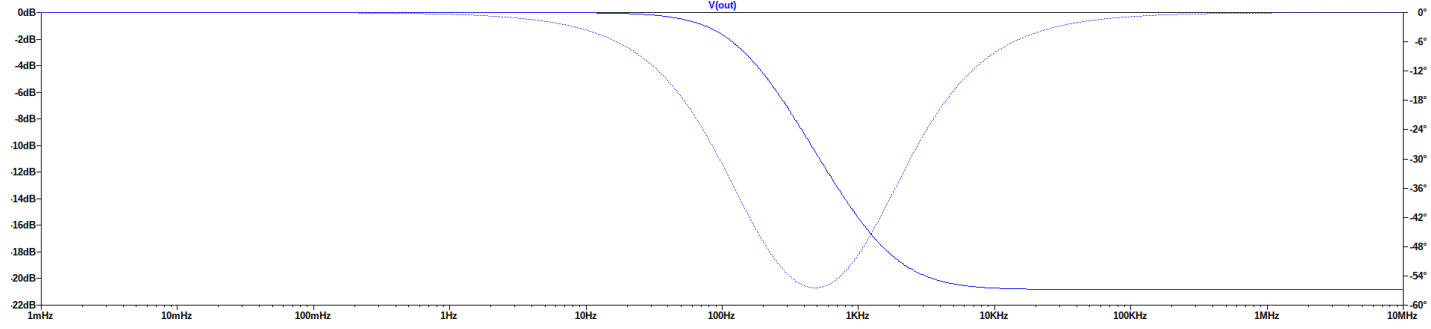
Observe that difference between peaks is approximatly 0.

Finally,

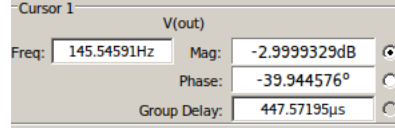
f	$\Delta\phi_{analytical}$	$\Delta\phi_{simulated}$
100Hz	-31.055°	-30.24°
1MHz	-0.0829°	0°

(c)

Bode Plot



3-db Point



From above obtained transfer function we get,

$$\begin{aligned}
 -3 &= 20 \log_{10} \left(\left| \frac{s + 10000}{11s + 10000} \right| \right) \\
 \Rightarrow \left| \frac{j\omega + 10000}{11j\omega + 10000} \right|^2 &= \frac{1}{2} \\
 \left(\frac{\omega^2 + 10^8}{121\omega^2 + 10^8} \right) &= \frac{1}{2} \Rightarrow \omega = 916.7 \text{ rad/s}^{-1} \\
 \Rightarrow f_{3-dB} &= 145.89 \text{ Hz}
 \end{aligned}$$

Corresponding phase lag would be,

$$\begin{aligned}
 \Delta\phi_{3-dB} &= \tan^{-1} \left(\frac{10000}{2\pi f} \right) - \tan^{-1} \left(\frac{10000}{22\pi f} \right) \\
 \Rightarrow \Delta\phi_{3-dB} &= -39.99^\circ
 \end{aligned}$$

2 Analytic calculations vs SPICE simulations

(a)

Applying KVL,

$$\begin{aligned}
 2.5 &= 2k\Omega * I_D + V_D + 2k\Omega * I_D + V_D \\
 \Rightarrow I_D &= \frac{2.5 - 2V_D}{4000} \\
 I_D &= 275 \mu A
 \end{aligned}$$

(b)

Current through diode is characterized by,

$$i_D = I_s \left(e^{\frac{V_D}{V_T}} - 1 \right)$$

Where I_s is Saturation current which is 10^{-14} A and V_T is thermal voltage which is 25.9mV at 300K. Using the above model to solve KVL we obtain,

$$2.5 = 2k\Omega * I_D + V_D + 2k\Omega * I_D + V_D$$

$$2.5 = 4000 * I_s \left(e^{\frac{V_D}{V_T}} - 1 \right) + 2V_D$$

As the above equation is strictly non linear and high exponential, Arriving at analytic solution would be tough so to compute the solution of the above equation "**Newton-Raphson Method**" is used to iteratively compute the solution.

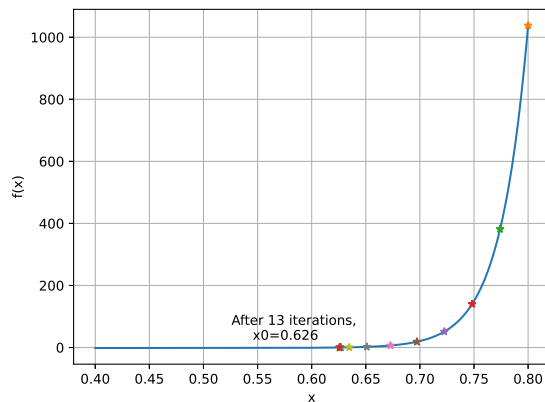
Python script for Newton-Raphson Method

```
import numpy as np
import matplotlib.pyplot as plt

def f(x):
    return 4e-11 * (np.exp(1000*x/25.9) - 1) + 2*x - 2.5
def df(x):
    return (4e-8/25.9)*np.exp(1000*x/25.9) + 2

plt.figure()
plt.plot(np.linspace(0.4, 0.8, 1000), f(np.linspace(0.4, 0.8, 1000)))
plt.grid()
plt.xlabel('x')
plt.ylabel('f(x)')
x0 = 0.8
itr = 12
for i in range(itr):
    print("x{} is {} and f(x{}) is {}".format(i, x0, i, f(x0)))
    plt.plot(x0, f(x0), "*")
    x0 -= f(x0)/df(x0)
plt.text(x0-0.1, f(x0)+25, "After 12 iterations,\n      x0={}".format(np.round(x0, 3)))
plt.savefig('../tex/figs/Q2_solv.eps')
plt.show()
```

Output



Verifying the solution $V_D = 0.626V$,

$$4000 * I_s \left(e^{\frac{V_D}{V_T}} - 1 \right) + 2V_D - 2.5 = -8.88E - 16 \approx 0$$

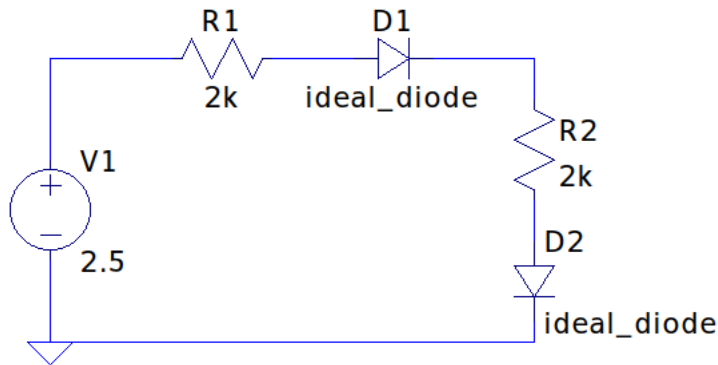
$$\Rightarrow I_D = 312\mu A$$

(c)

Netlist

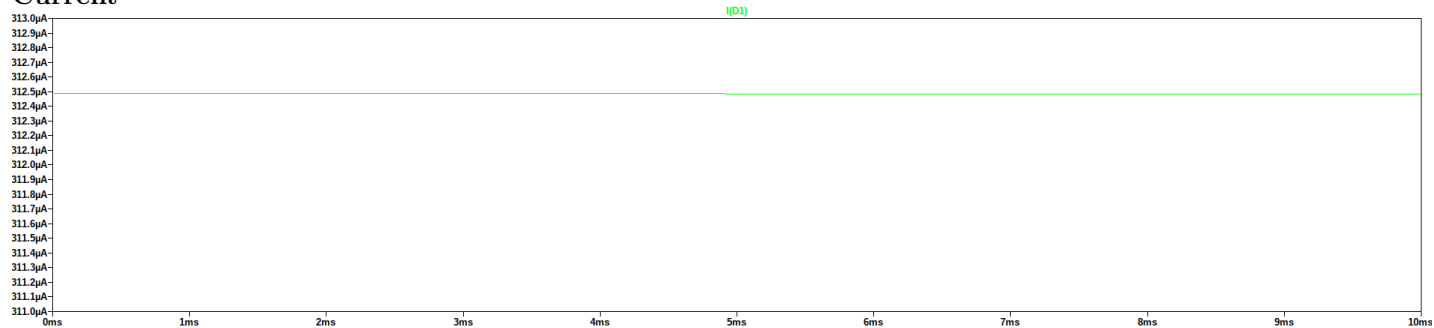
```
V1 N001 0 2.5
R1 N002 N001 2k
D1 N002 N003 ideal_diode
R2 N003 N004 2k
D2 N004 0 ideal_diode
.model D D
.lib C:\users\solomon\My Documents\LTspiceXVII\lib\cmp\standard.dio
.model ideal_diode D (IS=0.01p)
.tran 10m
.backanno
.end
```

Testbench

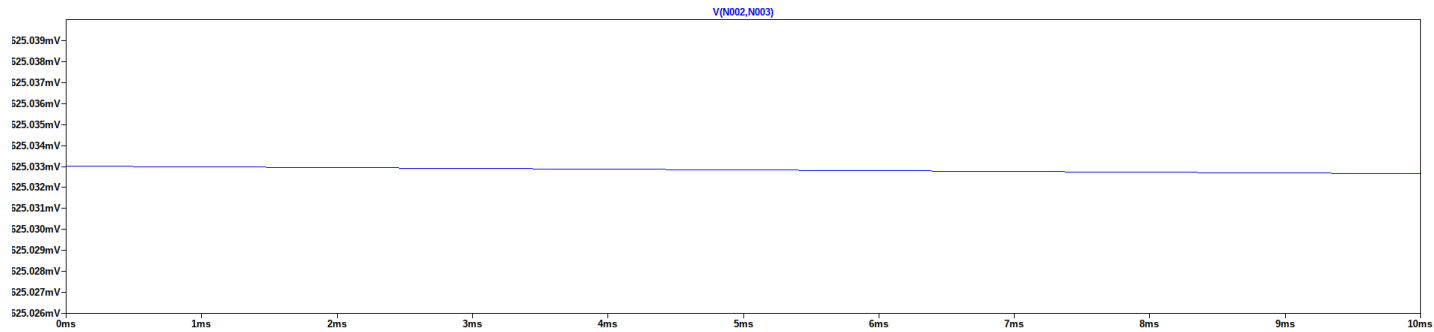


```
.model ideal_diode D (IS=0.01p)
.tran 10m
```

Current



Voltage



Comparisons

Question	I_D	V_D
(a)	$275\mu A$	0.7V
(b)	$312\mu A$	0.626V
(c)	$312.5\mu A$	0.625V

3 Controlled sources

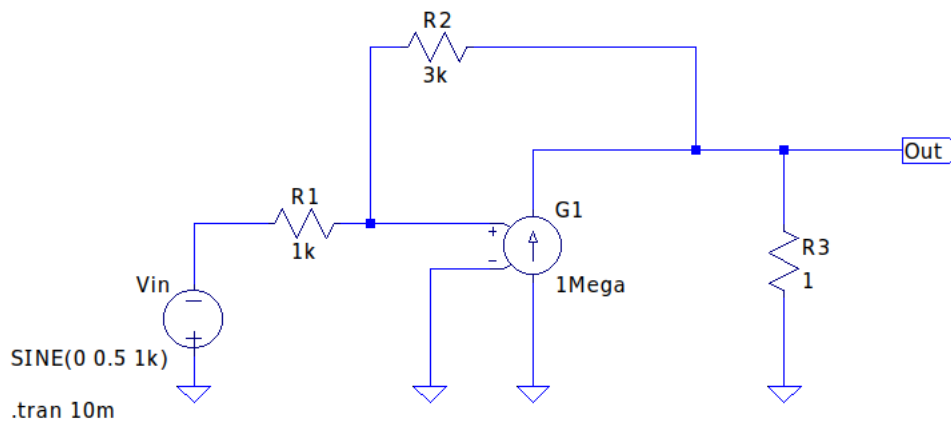
SPICE Netlist

```

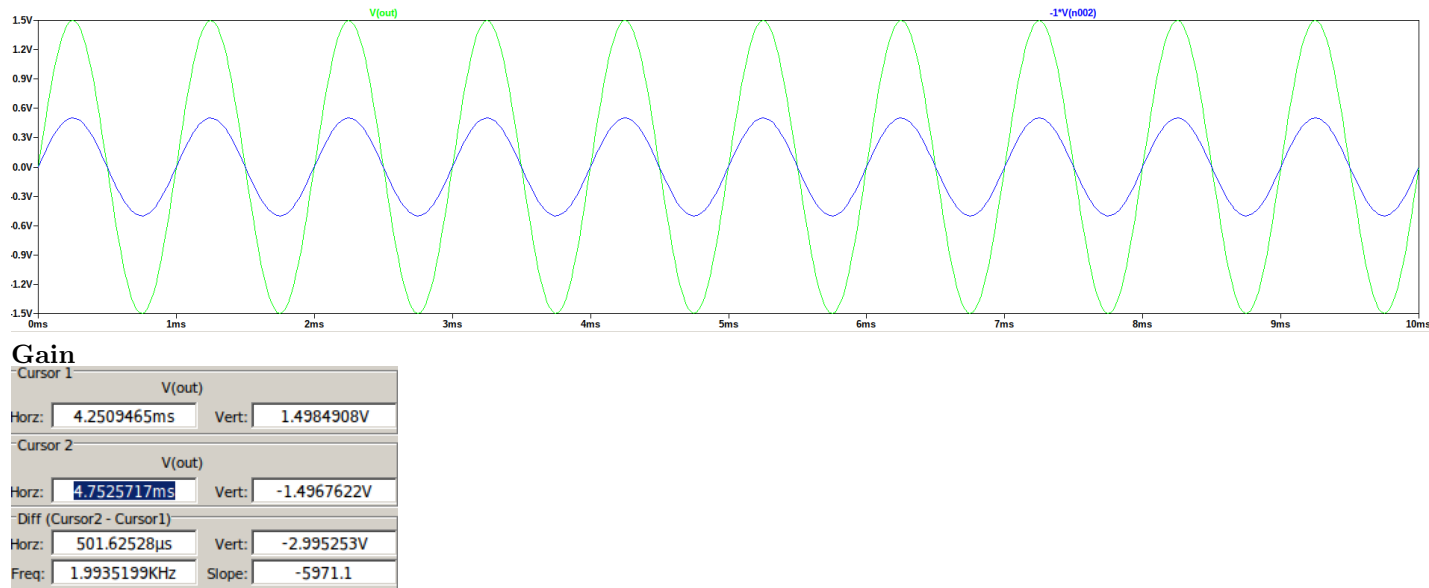
Vin 0 N002 SINE(0 0.5 1k)
R1 N001 N002 1k
G1 0 Out N001 0 1Mega
R2 Out N001 3k
R3 Out 0 1
.tran 10m
.backanno
.end

```

TestBench



Output Response



$$\frac{v_{out}}{v_{in}} = 3$$

Analytical solution,

VCCS has very high gain which means that both the terminal of voltage taps will be approximately same in order to make current flow zero else there would be very high current flow.

$$\begin{aligned}
 -v_{in} - 1000i &= 0 \implies i = \frac{-v_{in}}{1000} \\
 v_{out} &= 0 - 3000 * i \\
 \implies \frac{v_{out}}{v_{in}} &= 3
 \end{aligned}$$

4 MOSFET Characteristics

4.1 NMOS

Short Channel

SPICE Netlist

```

* Z:\home\solomon\VLSI\Assignments\Assignment 1\Simulation\Q4_nmos_sc.asc
Vgs N002 0 {Vgs}
M1 N001 N002 0 0 nch_tt l=180n w=270n
Vds N001 0 1.8
.model NMOS NMOS
.model PMOS PMOS
.lib C:\users\solomon\My Documents\LTspiceXVII\lib\cmp\standard.mos
.include TSMC180.lib
.step param Vgs list 0.4 0.5 0.6 0.7 0.8 0.9
.dc Vds 0 1.8 1m
;.dc Vgs 0 1.8
* Short Channel
* W = 270nm, L = 180nm
.backanno
.end

```

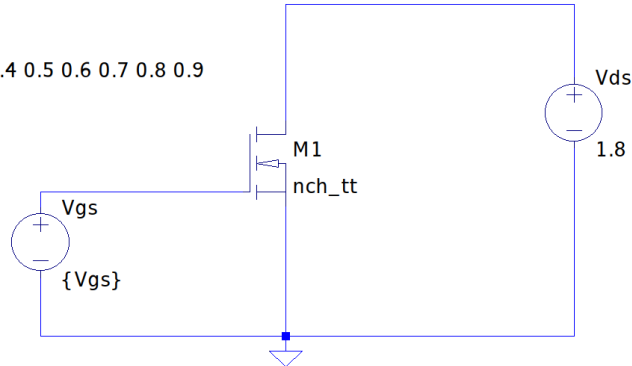
TestBench

Short Channel

W = 270nm, L = 180nm

```
.include TSMC180.lib
.step param Vgs list 0.4 0.5 0.6 0.7 0.8 0.9
.dc Vds 0 1.8 1m

;dc Vgs 0 1.8
```



Long Channel

SPICE Netlist

```
* Z:\home\solomon\VLSI\Assignments\Assignment 1\Simulation\Q4_nmos_lc.asc
Vgs N002 0 {Vgs}
M1 N001 N002 0 0 nch_tt l=10u w=15u
Vds N001 0 1.8
.model NMOS NMOS
.model PMOS PMOS
.lib C:\users\solomon\My Documents\LTspiceXVII\lib\cmp\standard.mos
.include TSMC180.lib
.step param Vgs list 0.4 0.5 0.6 0.7 0.8 0.9
.dc Vds 0 1.8 1m
;dc Vgs 0 0.4
* Long Channel
* W = 15um, L = 10um
.backanno
.end
```

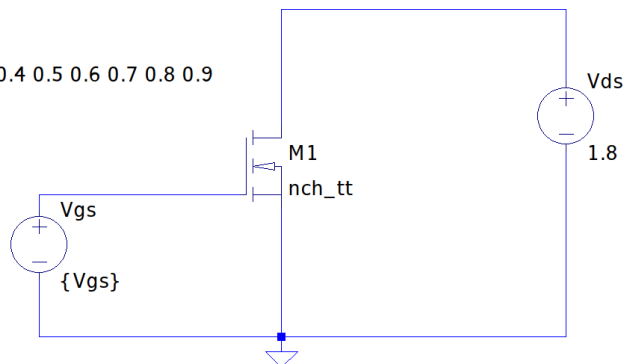
TestBench

Long Channel

W = 15um, L = 10um

```
.include TSMC180.lib
.step param Vgs list 0.4 0.5 0.6 0.7 0.8 0.9
.dc Vds 0 1.8 1m

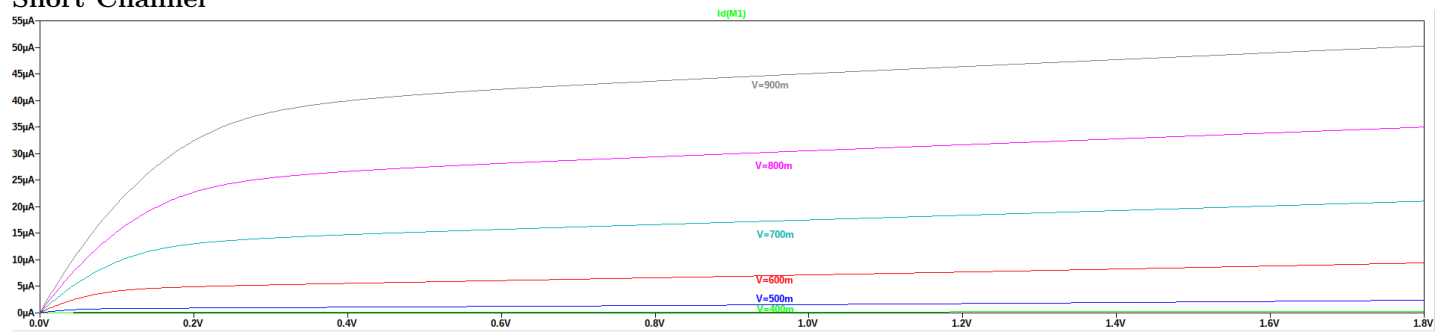
;dc Vgs 0 0.4
```



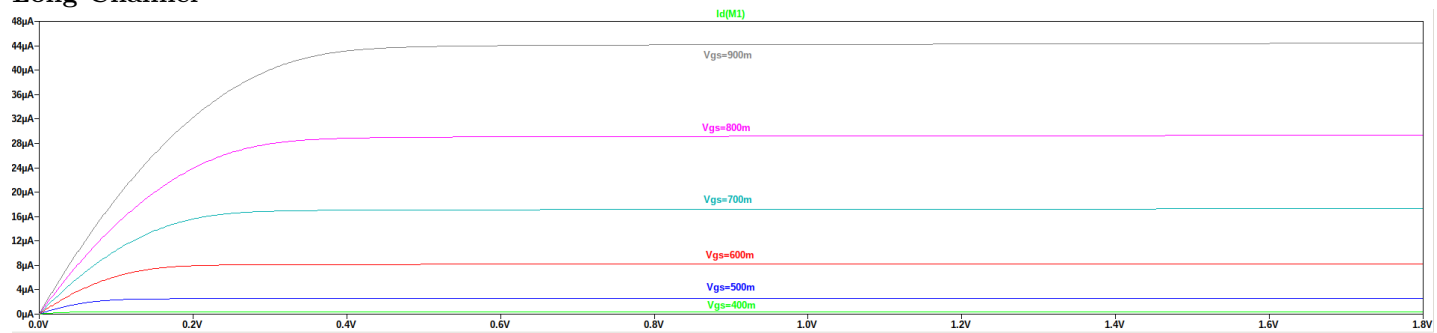
(a)

I_{ds} vs V_{ds}

Short Channel

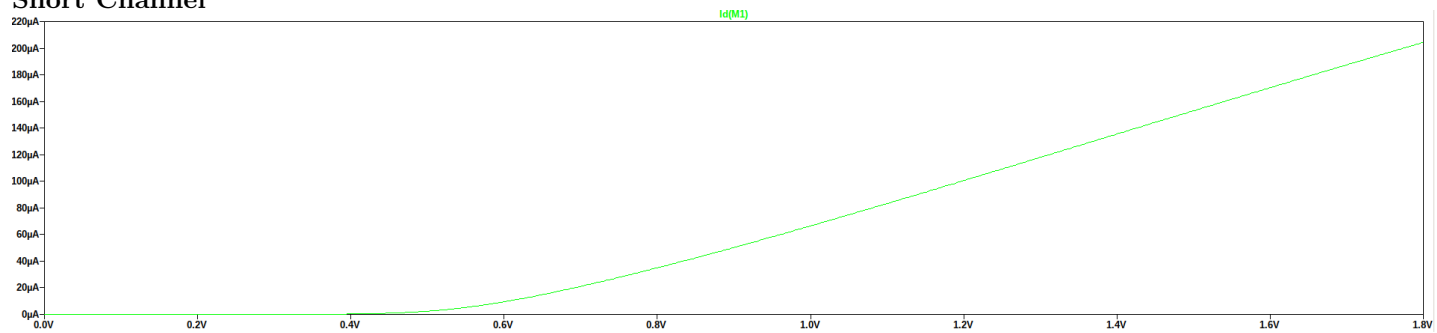


Long Channel

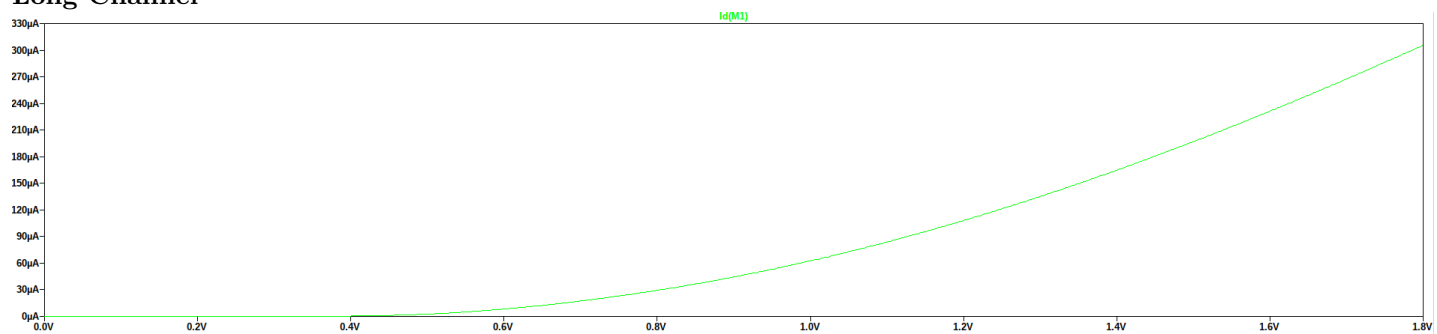


I_{ds} vs V_{gs}

Short Channel



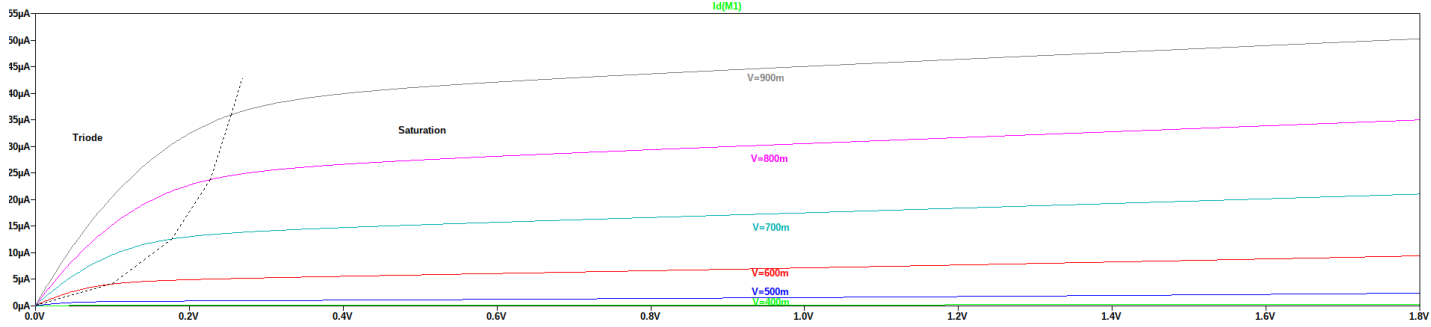
Long Channel



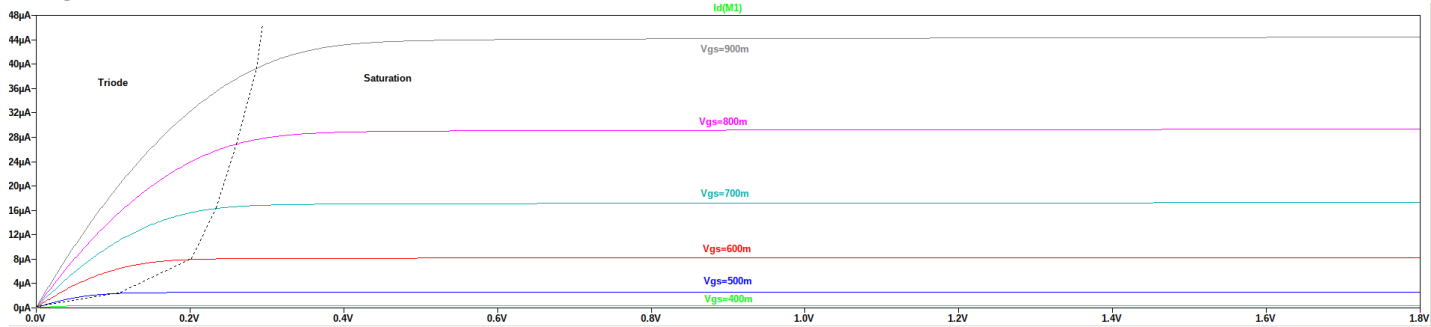
(b)

I_{ds} vs V_{ds}

Short Channel



Long Channel



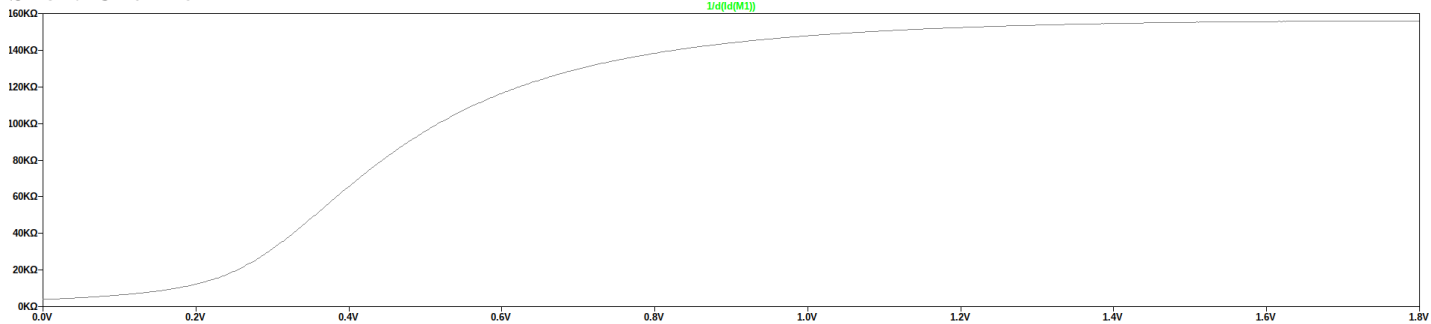
Differences

Current in saturation of short channel MOSFET is not constant but has a linear dependency on V_{ds} , which is also known as **Channel length modulation**. This effect is significant in shorter channel devices as decrement of channel length in shorter channel is significant compared to longer length channel due to depletion regions formed at higher V_{ds} .

(c)

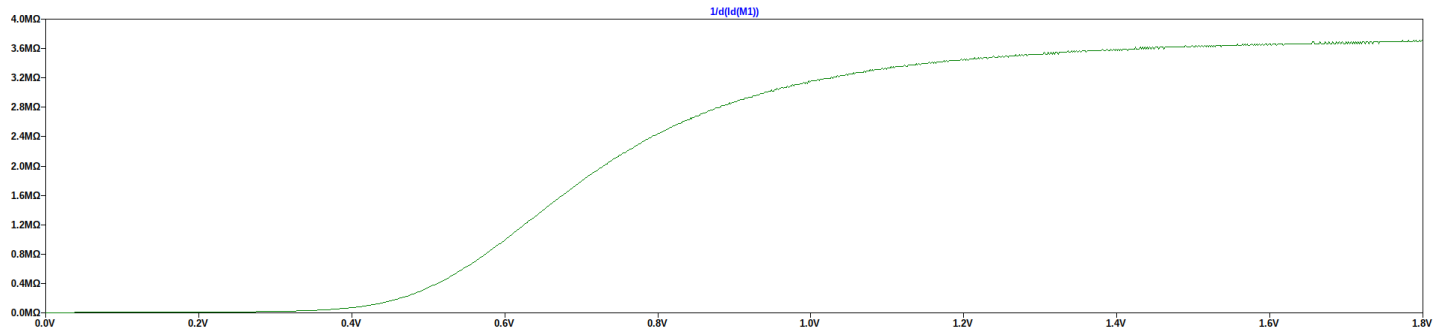
In I_{ds} vs V_{ds} characteristics, the below graphs are obtained by taking $\frac{1}{\frac{\partial I_{ds}}{\partial V_{ds}}}$.

Short Channel



It is observed that small signal output resistance is **155.65kΩ**.

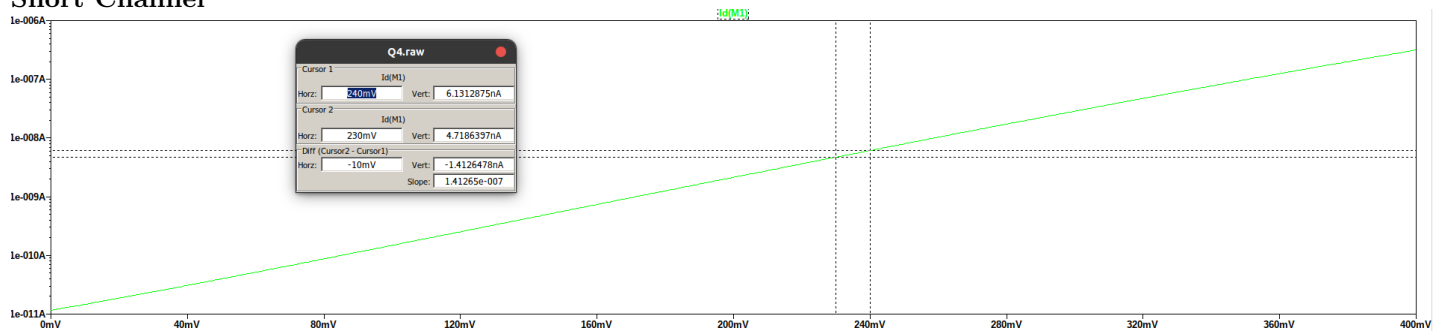
Long Channel



It is observed that small signal output resistance is **3.66MΩ**.

(d)

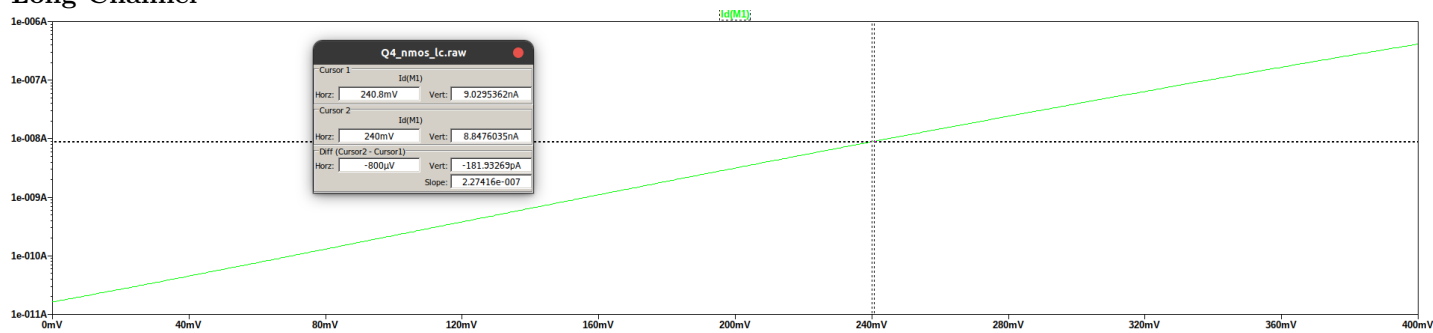
Short Channel



Slope = 1.41265×10^{-7}

$$S = n \left(\frac{kT}{q} \right) \ln(10) = 1.41265e-7 \Rightarrow n = 2.368 \times 10^{-6}$$

Long Channel



Slope = 2.27416×10^{-7}

$$S = n \left(\frac{kT}{q} \right) \ln(10) = 2.27416e-7 \Rightarrow n = 3.8133 \times 10^{-6}$$

4.2 PMOS

Short Channel

SPICE Netlist

```
* Z:\home\solomon\VLSI\Assignments\Assignment 1\Simulation\Q4_pmos_sc.asc
Vsd N001 0 1.8
M1 0 N002 N001 N001 pch_tt L = 180n W = 270n
Vsg N001 N002 {Vsg}
```

```

.model NMOS NMOS
.model PMOS PMOS
.lib C:\users\solomon\My Documents\LTspiceXVII\lib\cmp\standard.mos
.include TSMC180.lib
.step param Vsg list 0.4 0.5 0.6 0.7 0.8 0.9
.dc Vsd 0 1.8 1m
;.dc Vsg 0 1.8 1m
* Short Channel
* W = 270nm, L = 180nm
.backanno
.end

```

TestBench

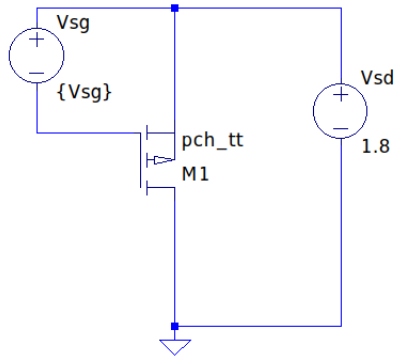
Short Channel
W = 270nm, L = 180nm

```

.include TSMC180.lib
.step param Vsg list 0.4 0.5 0.6 0.7 0.8 0.9
.dc Vsd 0 1.8 1m

;.dc Vsg 0 1.8 1m

```



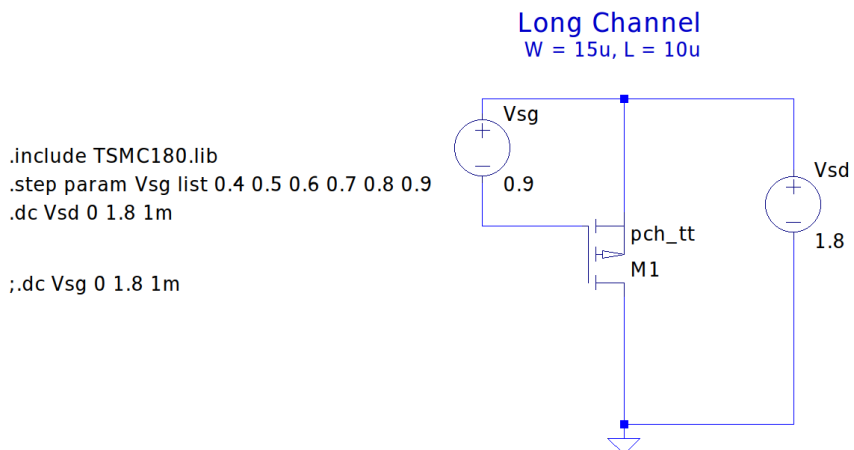
Long Channel SPICE Netlist

```

* Z:\home\solomon\VLSI\Assignments\Assignment 1\Simulation\Q4_pmos_lc.asc
Vsd N001 0 1.8
M1 0 N002 N001 N001 pch_tt L = 10u W = 15u
Vsg N001 N002 0.9
.model NMOS NMOS
.model PMOS PMOS
.lib C:\users\solomon\My Documents\LTspiceXVII\lib\cmp\standard.mos
.include TSMC180.lib
.step param Vsg list 0.4 0.5 0.6 0.7 0.8 0.9
.dc Vsd 0 1.8 1m
;.dc Vsg 0 1.8 1m
* Long Channel
* W = 15u, L = 10u
.backanno
.end

```

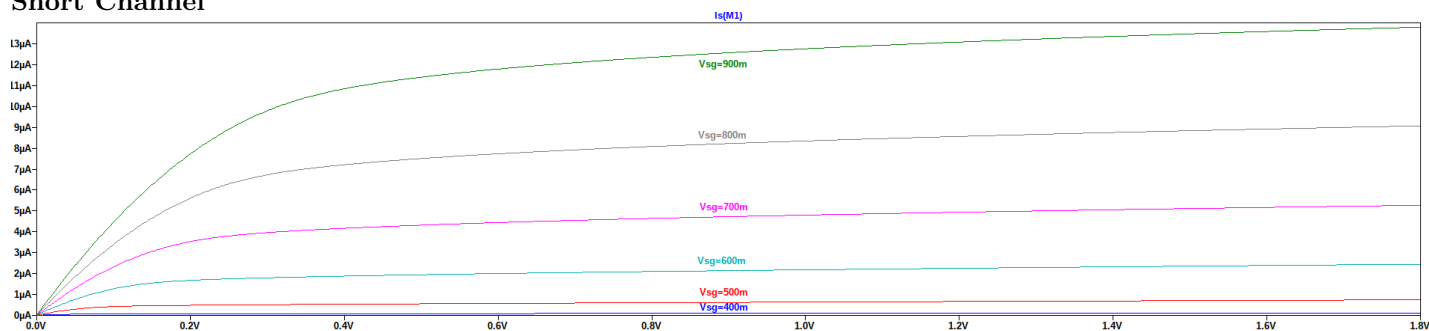
TestBench



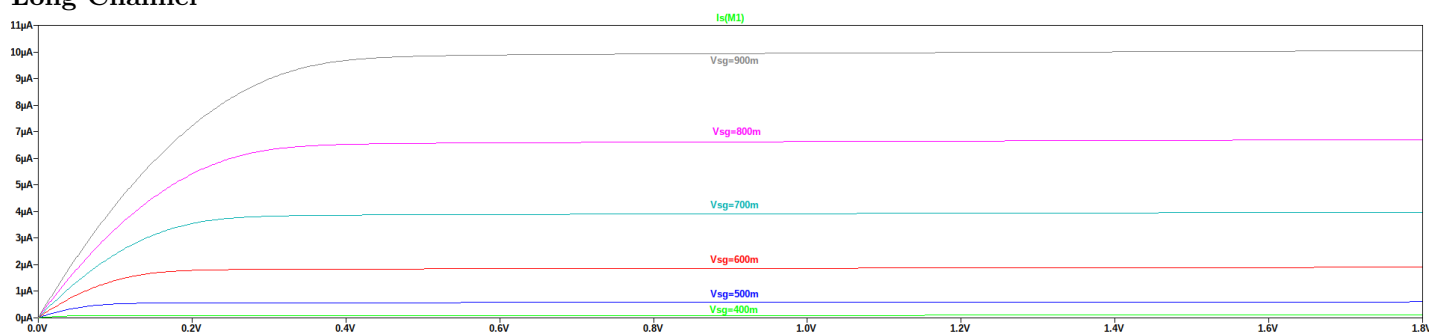
(a)

I_{ds} vs V_{ds}

Short Channel

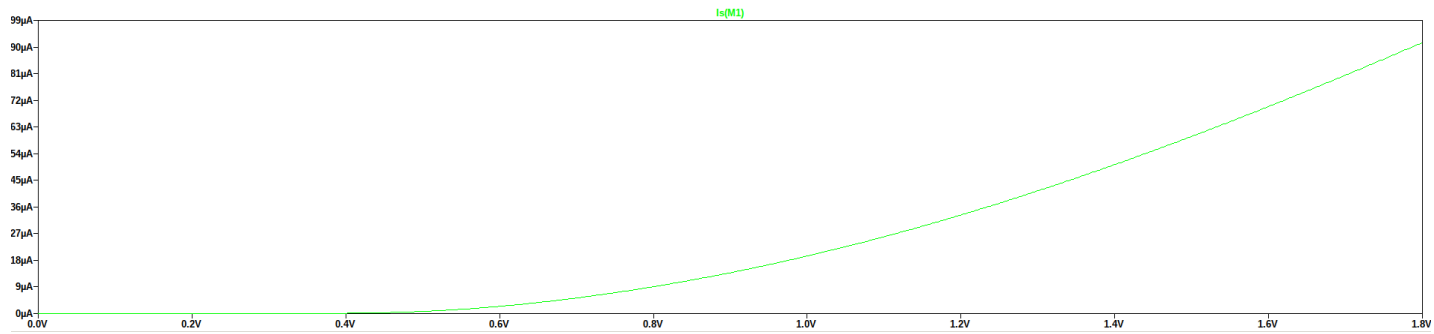


Long Channel

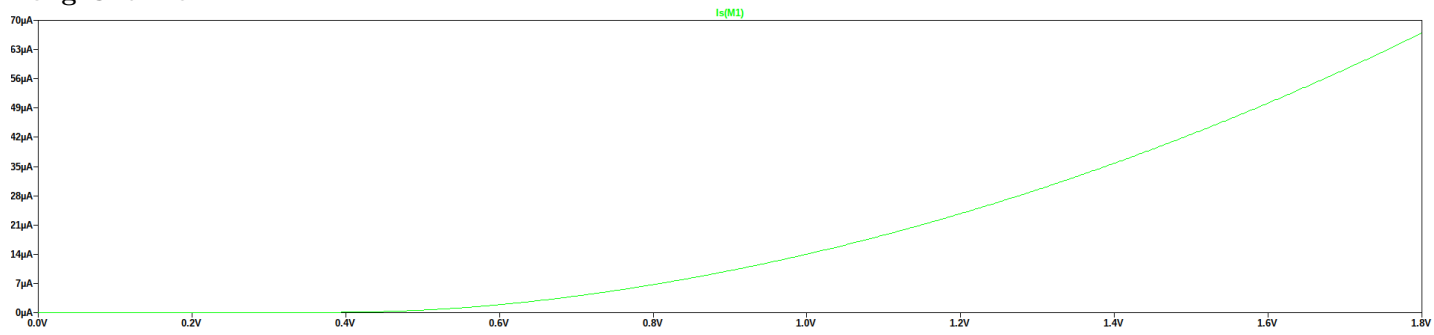


I_{ds} vs V_{gs}

Short Channel



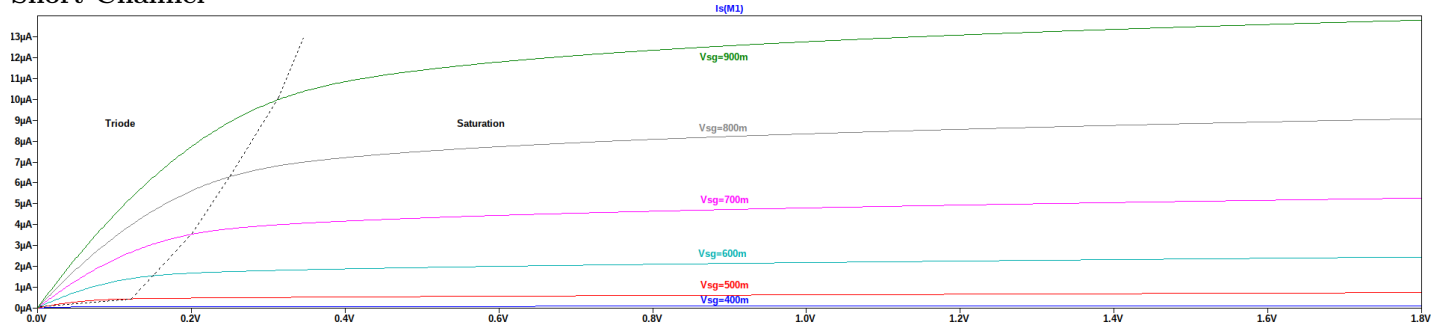
Long Channel



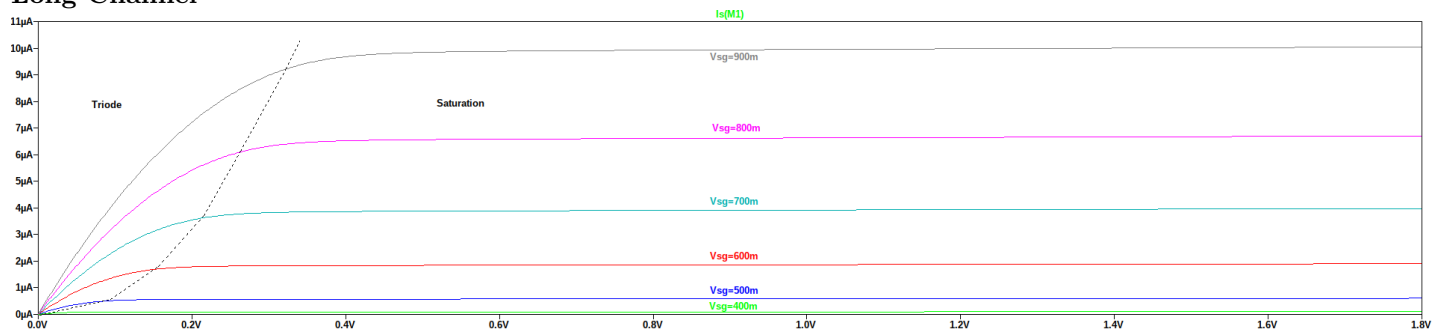
(b)

I_{ds} vs V_{ds}

Short Channel



Long Channel



Differences

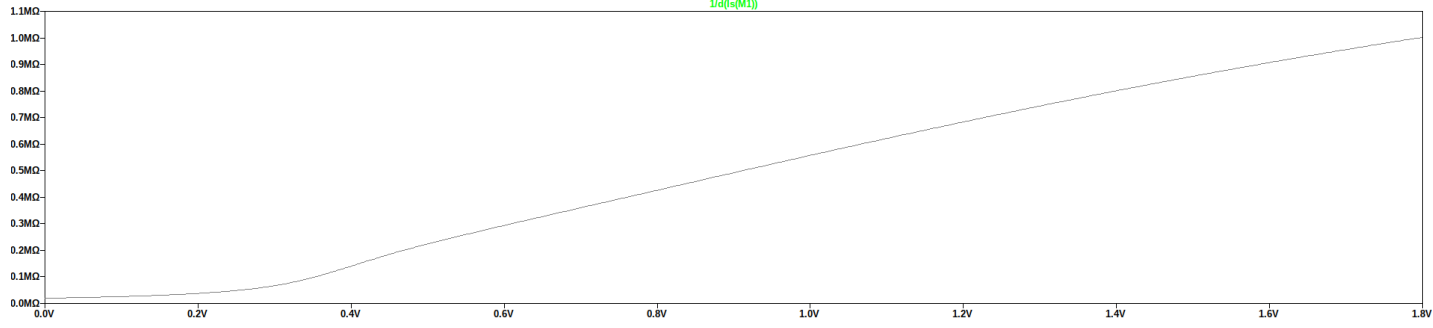
Current in saturation of short channel MOSFET is not constant but has a linear dependency on V_{ds} , which is

also known as **Channel length modulation**. This effect is significant in shorter channel devices as decrement of channel length in shorter channel is significant compared to longer length channel due to depletion regions formed at higher V_{ds} .

(c)

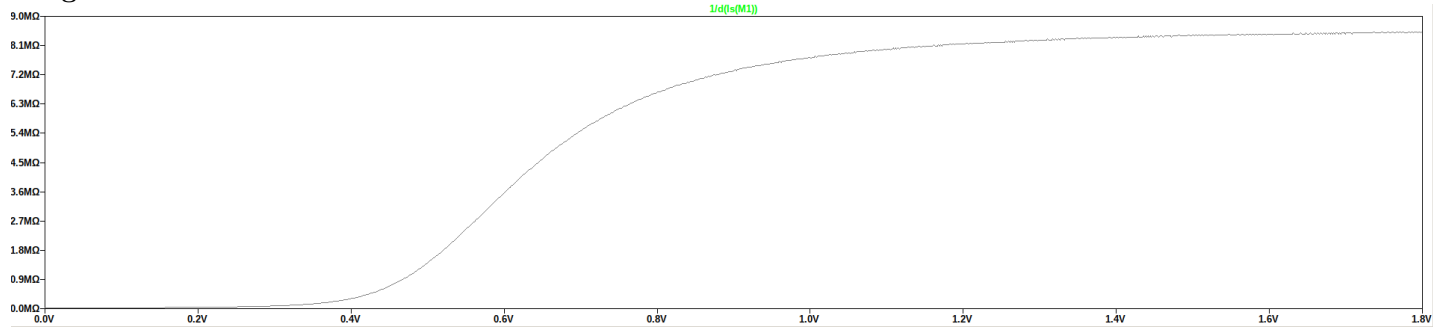
In I_{sd} vs V_{sd} characteristics, the below graphs are obtained by taking $\frac{1}{\frac{\partial i_{sd}}{\partial v_{sd}}}$.

Short Channel



It is observed that small signal output resistance is **1.1MΩ**.

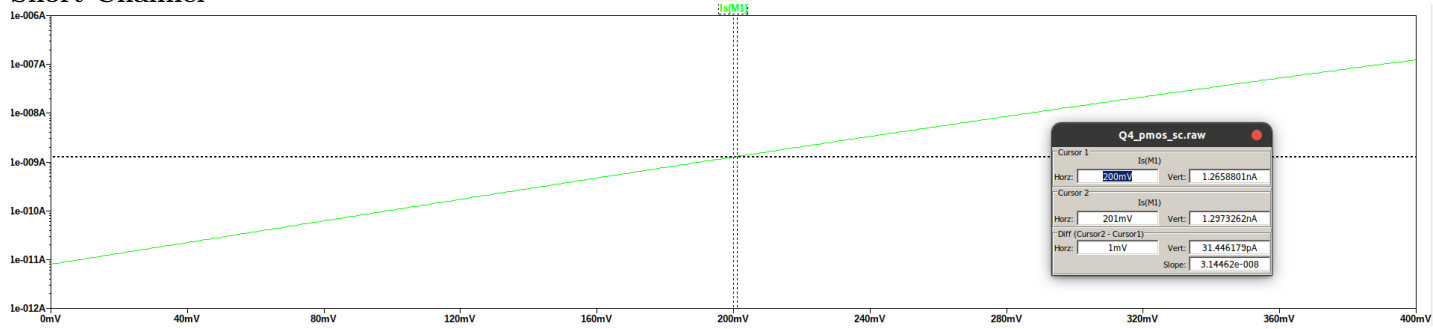
Long Channel



It is observed that small signal output resistance is **8.5MΩ**.

(d)

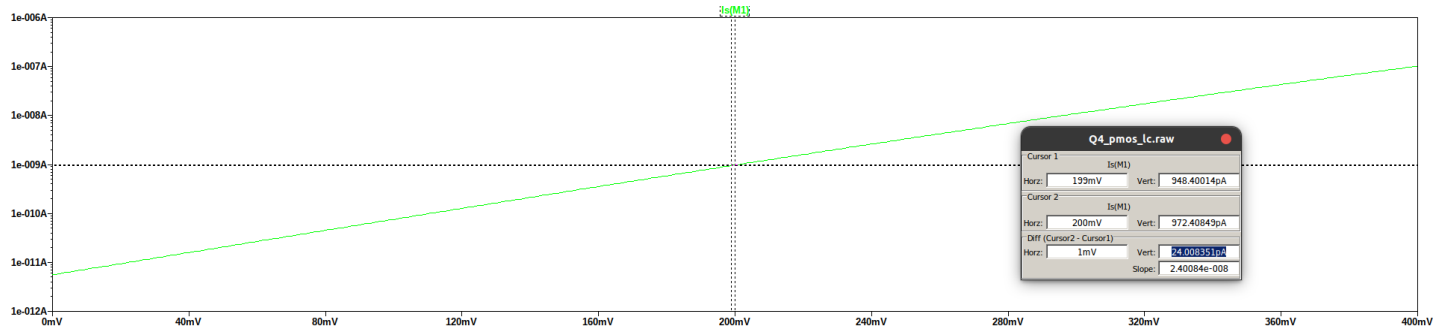
Short Channel



Slope = 1.41265×10^{-8}

$$S = n \left(\frac{kT}{q} \right) \ln(10) = 1.41265 \times 10^{-8} \Rightarrow n = 5.454 \times 10^{-7}$$

Long Channel



Slope = 3.144×10^{-8}

$$S = n \left(\frac{kT}{q} \right) \ln(10) = 3.144e-8 \Rightarrow n = 1.214 \times 10^{-6}$$

Final comparisons

Output Resistances

Device	$\frac{W}{L} = 1.5$	r_o
NMOS	L = 180nm, W = 270nm	155.65k Ω
	L = 10 μ m, W = 15 μ m	3.66M Ω
PMOS	L = 180nm, W = 270nm	1.1M Ω
	L = 10 μ m, W = 15 μ m	8.51M Ω

n

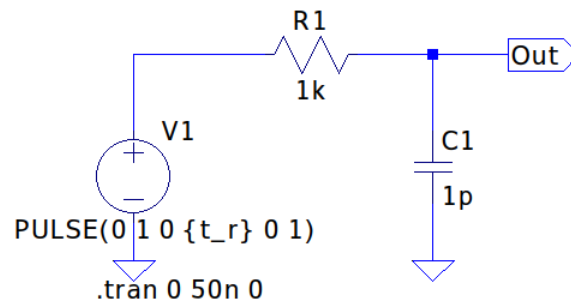
Device	$\frac{W}{L} = 1.5$	n
NMOS	L = 180nm, W = 270nm	2.368 μ
	L = 10 μ m, W = 15 μ m	3.813 μ
PMOS	L = 180nm, W = 270nm	0.5454 μ
	L = 10 μ m, W = 15 μ m	1.214 μ

5 Propagation Delay

SPICE Netlist

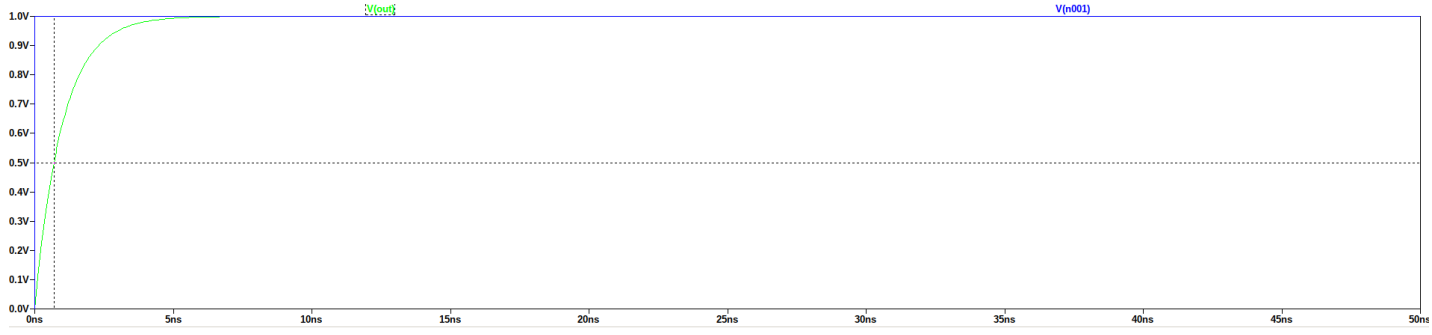
```
V1 N001 0 PULSE(0 1 0 {t_r} 0 1)
R1 Out N001 1k
C1 Out 0 1u
.tran 10m
.backanno
.end
```

TestBench



```
.step param t_r list 10p 20p 50p 100p 200p 500p 1n 2n 5n 10n
```


(a)

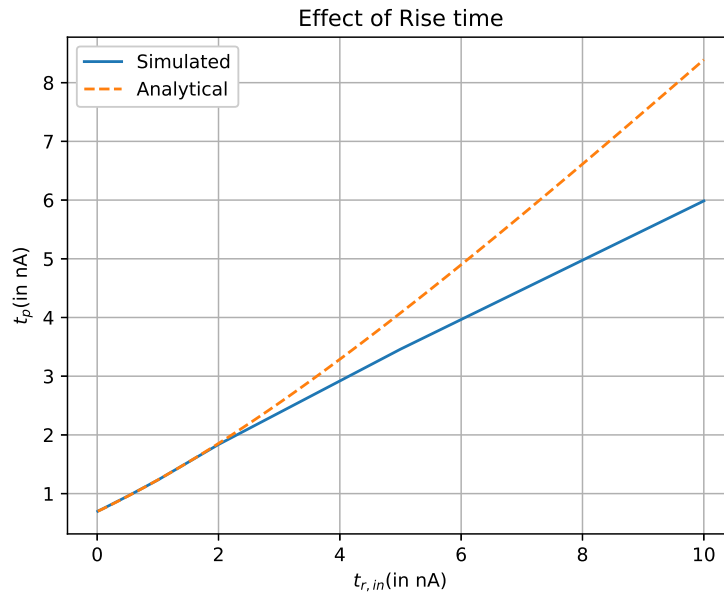
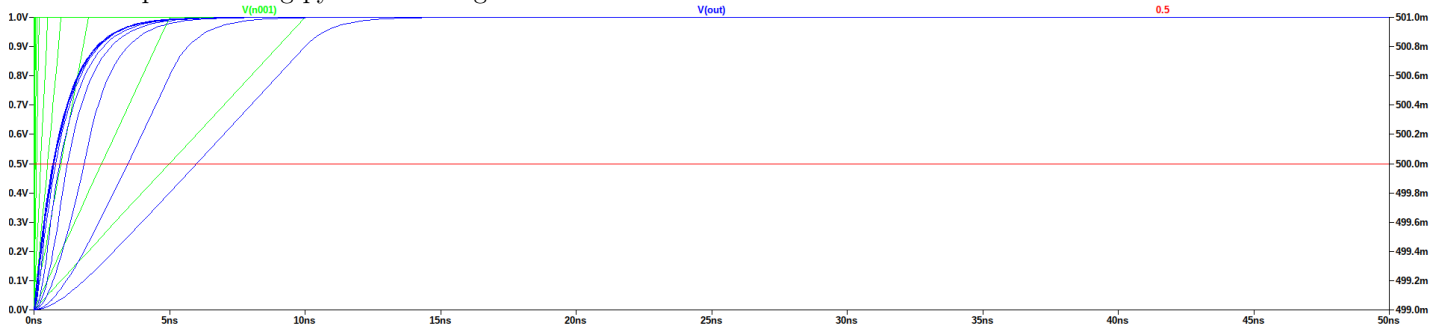


$$t_{p,simulated} = 692\text{ps}$$

$$t_{p,calculated} = RC\ln(2) = 693.14\text{ps}$$

(b)

Now from the SPICE simulations with different rise time from 10ps to 10ns, and Propagation delay is observed and plotted using python with log-lin.



The analytical expression is evaluated in (c).

(c)

The input can be interpreted as difference two ramp signals where one is delayed by t_r .

$$\begin{aligned}
 V_{in}(t) &= \frac{r(t) - r(t - t_r)}{t_r} \\
 \Rightarrow V_{in}(s) &= \frac{\frac{1}{s^2} - \frac{e^{-st_r}}{s^2}}{t_r} \Rightarrow V_{in}(s) = \frac{1}{s^2} \left(\frac{1 - e^{-st_r}}{t_r} \right) \\
 V_{out}(s) &= V_{in}(s) \frac{1}{1 + s\tau} \Rightarrow V_{out}(s) = \frac{1}{s^2} \left(\frac{1 - e^{-st_r}}{t_r} \right) \frac{1}{1 + s\tau} \\
 V_{out}(s) &= \frac{1}{t_r} \left(\left(\frac{1}{s^2(1 + s\tau)} \right) - \left(\frac{e^{-st_r}}{s^2(1 + s\tau)} \right) \right) \\
 V_{out}(t) &= \frac{1}{t_r} \left(\left(t - \tau + \tau e^{-\frac{t}{\tau}} \right) - \left(t - t_r - \tau + \tau e^{-\frac{t-t_r}{\tau}} \right) \right) \\
 \Rightarrow & \boxed{V_{out}(t) = 1 - e^{-\frac{t}{\tau}} \left(\frac{e^{\frac{t_r}{\tau}} - 1}{t_r/\tau} \right)}
 \end{aligned}$$

Where τ is RC and t_r is rise time.

According to definition of propagation delay $V_{out}(t_p) = 0.5V$.

$$\begin{aligned}
 0.5 &= 1 - e^{-\frac{t_p}{\tau}} \left(\frac{e^{\frac{t_r}{\tau}} - 1}{t_r/\tau} \right) \\
 \Rightarrow & \boxed{t_p = RC \ln \left(2 \left[\frac{e^{\frac{t_r}{RC}} - 1}{t_r/RC} \right] \right)}
 \end{aligned}$$

When $t_r \rightarrow 0$, $t_p \rightarrow RC \ln 2$.