LAB Experiment 8
Logic Gates

S.V.Harshith EE19BTECH11018

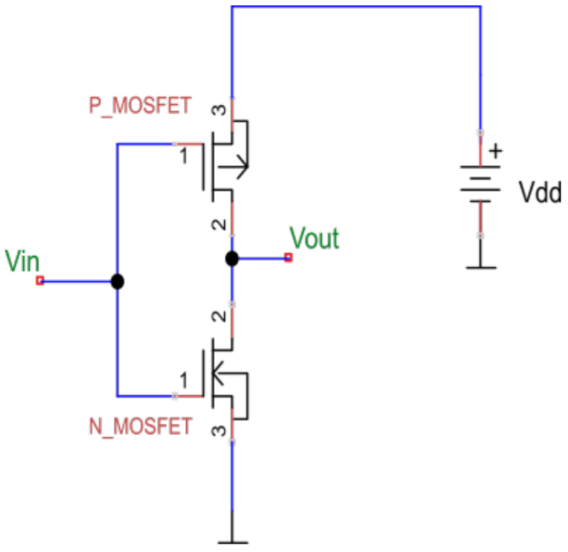
November 20,2020

1 Aim

- Implement NOT Gate in NgSPICE with $W_n = 1\mu m$, $W_p = 10\mu m$ and plot the V_{in} v/s V_{out} and explain the operation.
- Implement 2 input Nor logic gate and verify the operation. The inputs are through the pulse generator.
- Using NOR and NOT gate implement OR gate in NgSPICE (use sub-circuits). Verify the operation of the OR gate.

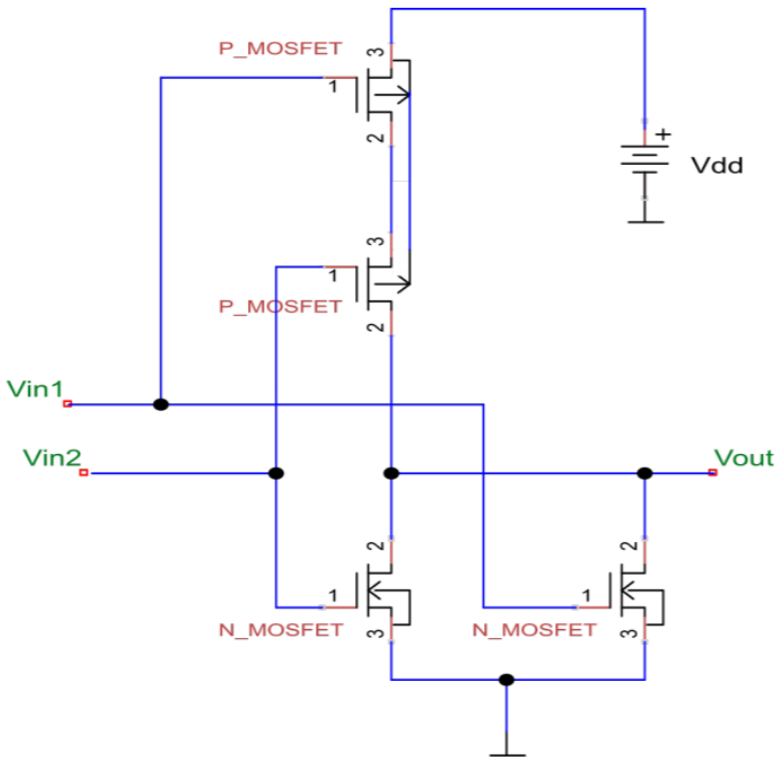
2 Procedure

2.1 NOT Gate

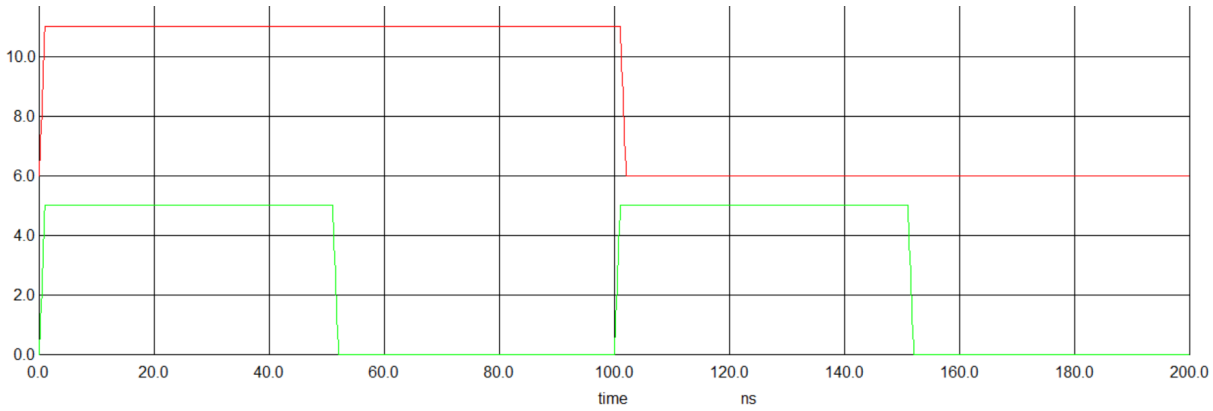


Write a NgSpice script for the above circuit shown above , take the value of $V_{dd} = 5V$ and Plot V_{in} v/s V_{out} by varying V_{in} from 0V to 5V

2.2 NOR Gate



Write a NgSpice script for the above circuit shown above , take the value of $V_{dd} = 5V$ and we can give square wave pulses with 100ns and 200ns time period as input and represent the value for 0 as 0V and 1 as 5V accordingly for V_{in1} and V_{in2} so that we get 4 different cases as shown below

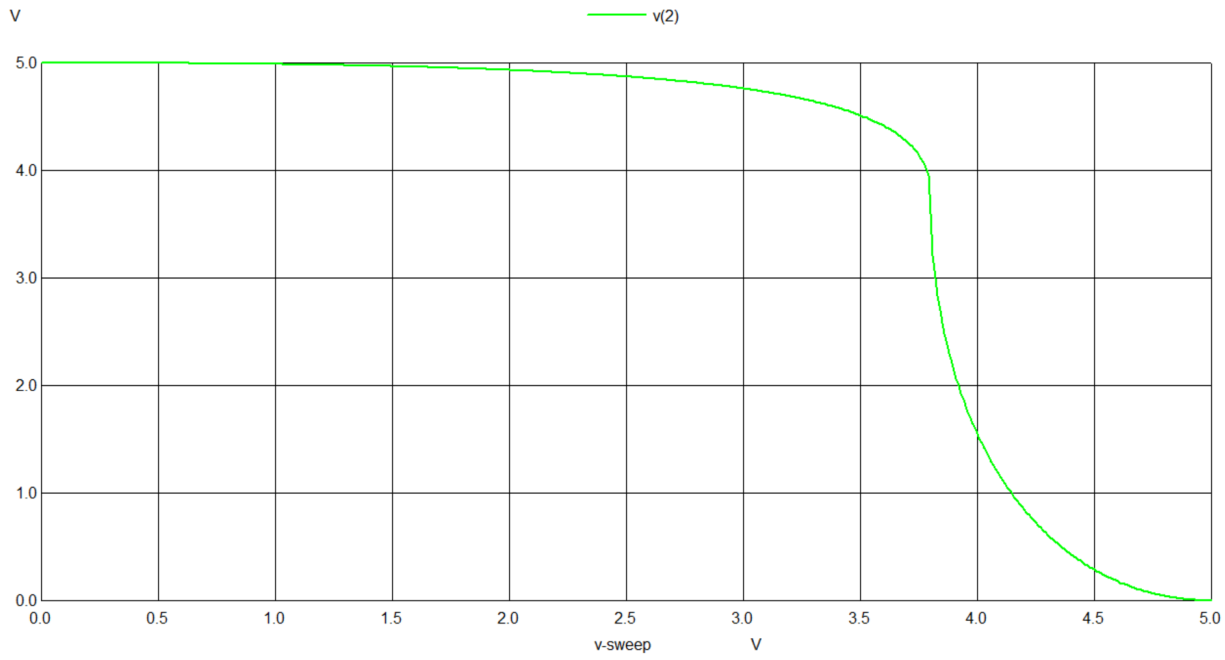


2.3 OR Gate

Write the above two scripts of NOT and NOR gates as subcircuits in NgSpice and connect them both so that we get an OR gate i.e connect the output of NOR gate to the NOT gate.

3 Results and Understanding

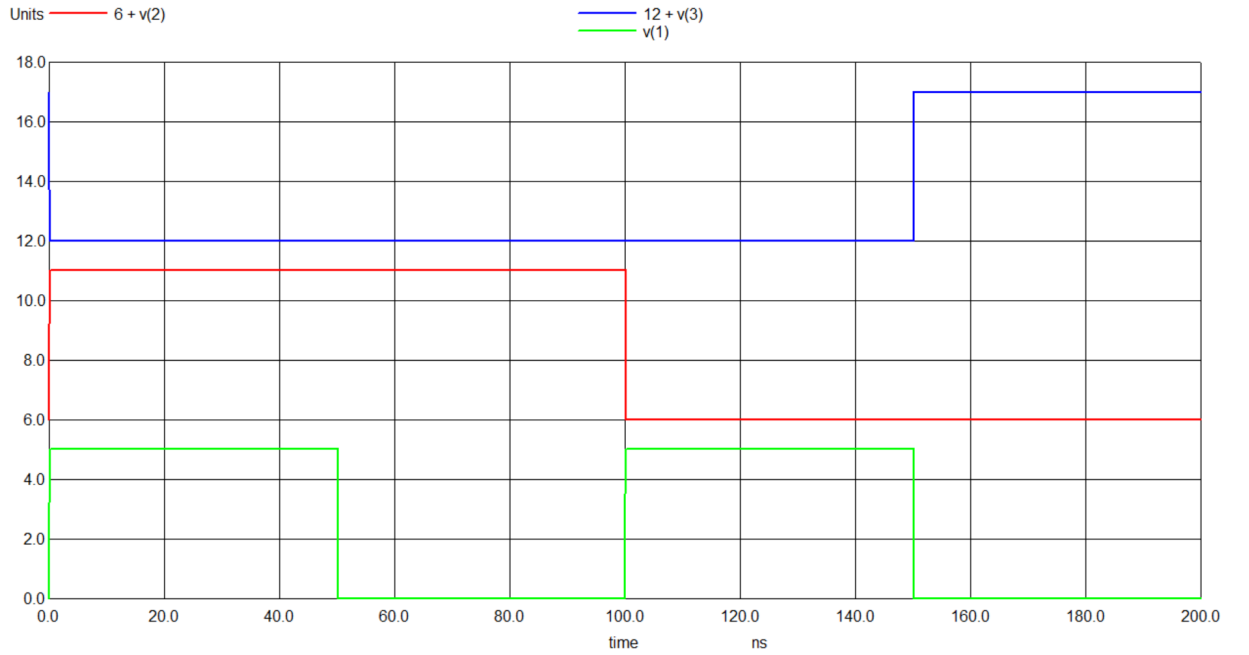
3.1 NOT Gate



- When the input is 0V, PMOSFET acts as a closed switch since its gate voltage is less than its Source voltage and it is in saturation region.
- NMOSFET acts as an open switch since it gate voltage is equal to its source voltage and it is in cut-off region.
- And since the PMOSFET is connected to $V_{dd} = 5V$ the output voltage is 5V.
- Similarly when the input is 5V the PMOSFET acts as an open switch and the NMOSFET acts as a closed switch and the output is 0V.

If we increase the width of the channel(W), the pinch-off voltage increases and the saturation current also increases.
So when $W_p > W_n$, for PMOSFET the current is high even for low value of V_{gs} and the output voltage doesn't drop even for high voltages at the gate. Thus the graph moves towards right.

3.2 NOR Gate

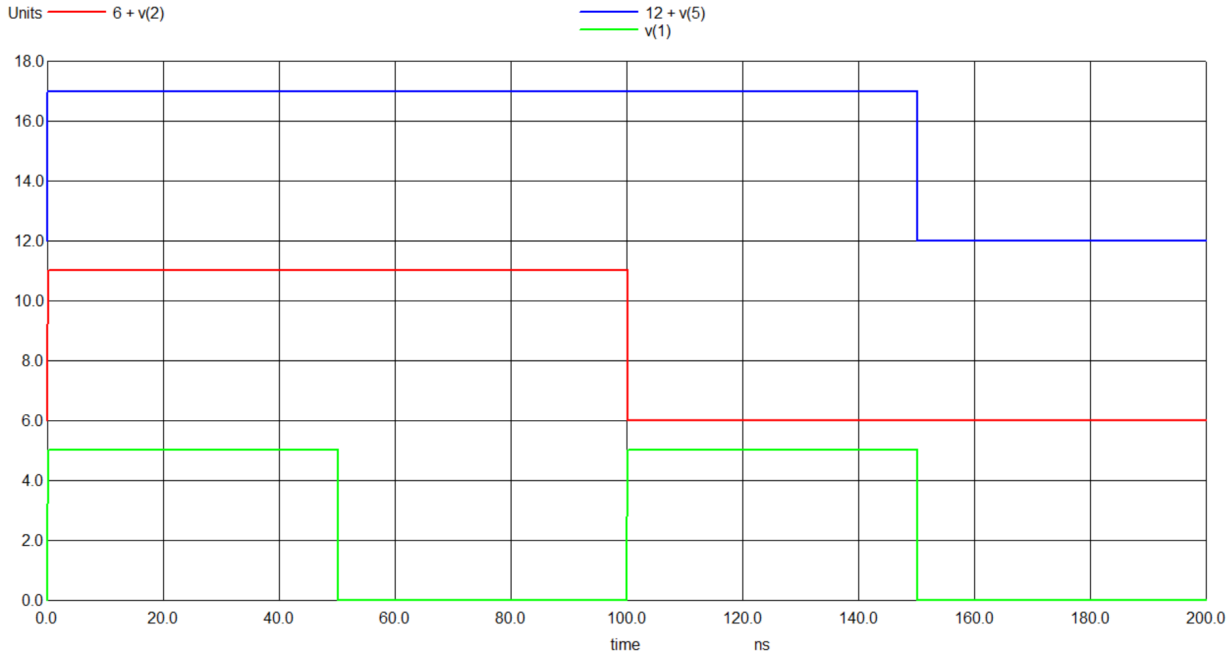


We can check that V_{out} follows according to the below truth table of NOR gate

$V_{in1}(Green)$	$V_{in2}(Red)$	$V_{out}(Blue)$
1	1	0
0	1	0
1	0	0
0	0	1

- When both V_{in1} and V_{in2} are 0V, both the parallelly connected NMOSFETs are in cut-off region and act as an open switch. But the PMOSFETs are in saturation region and act as a closed switch. Since $V_{dd} = 5V$ is connected to the PMOSFETs the output voltage is 5V.
- In rest of the cases at least one of V_{in1} and V_{in2} is 5V, so the NMOSFETs will act as closed switch and the series PMOSFETs act as open switch. So the output voltage is 0V.

3.3 OR Gate



We can check that V_{out} follows according to the below truth table of OR gate

$V_{in1}(Green)$	$V_{in2}(Red)$	$V_{out}(Blue)$
1	1	1
0	1	1
1	0	1
0	0	0

Since the NOR gate output is passed through a NOT gate the output is inverted.

$$V_{out} = NOT(NOR(V_{in1}, V_{in2})) = \overline{\overline{V_{in1} + V_{in2}}} = V_{in1} + V_{in2} = OR(V_{in1}, V_{in2})$$

4 Conclusion

Logic gates are used to develop many IC circuits and microchips these days and have become become a basic block of the modern life.
NOR and NAND gates are called as universal gates since all the other basic gates can be constructed using them.