EE3113/3301/5184: Introduction to VLSI Design

Homework Assignment 2 **Deadline: 2 Nov 2021**

1. **MOSFET Resistance**

   The MOSFET output small signal resistance is defined by the slope of the $I_D - V_D$ characteristics. However, in digital circuits we are often interested in *equivalent resistance* presented by the MOSFET during charging/discharging of a capacitor (see example 3.8 of your textbook). In this exercise you will run simulations to determine the equivalent resistance of the regular NMOS and PMOS transistors in 0.18 μm process as a function of V_{DS}.

   (a) Perform a transient simulation of the circuit in Figure 1 using $W/L = 240/180$ or $W/L = 400/180$ and $V_{DD} = 1.8\,V$. Set the initial voltage across the capacitor to be $1.8\,V$. You should submit plots of R_{eq} as a function of V_{DS} for NMOS and PMOS devices (*c. f. Figure 3.27 of course textbook*). *Note: For PMOS devices you need to modify the circuit*

   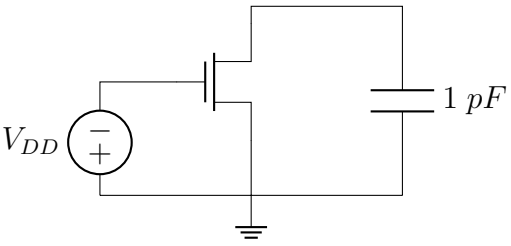

   Figure 1

   (b) Compare your answers with Table 3.3 of textbook and explain the differences.

2. **MOSFET Capacitance**

   The gate capacitance of a MOSFET can be calculated by applying a gate voltage $V_{applied} = V_{CM} + V_0 \sin(\omega t)$ in the circuit in Figure 2. Since $I = CV_0\omega\cos(\omega t)$ we can obtain the CV characteristics by sweeping V_{CM} (in ac analysis) and setting AC magnitude to $1/(2\pi f)$, where f is the frequency of choice. The capacitance will then be given by the current in gate terminal.

   Consider long and short channel MOSFETs with $L = 10\ \mu m$ and $L = 0.18\ \mu m$ respectively. Both devices have identical W/L of 1.5/2.5

   (a) Simulate the CV characteristics of NMOS devices using 180 nm technology. Generate plots of $C(V_{CM})$ for short and long channel devices, and explain the trends you observe in your simulations. (*c. f. Example 3.9 of textbook*)

   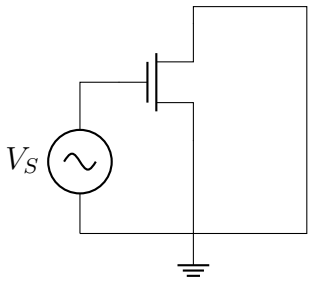

   Figure 2

   (b) Will the CV characteristics change when you set the frequency to 10 MHz and 10 GHz? Explain your results.

3. **Inverter Implementations**

   The circuits in Figure 3 show different implementations of a digital inverter ($V_{DD} = 1.2\,V$), whose output is connected to a capacitor. Assume $V_{TN} = |V_{TP}| = 0.3\,V$, and the output capacitor, C_L, is initially discharged. Ignore sub-threshold conduction and body effect. Without running simulations answer the following:

   (a) Which one(s) of the circuits consume(s) static power when the input is high ($V_{IN} = 1.2\,V$)?

(b) Which one(s) of the circuits consume(s) static power when the input is low($V_{IN} = 0\ V$)?

(c) V_{OH} of which circuit(s) is 1.2 V (if possible)?

(d) V_{OL} of which circuit(s) is 0 V (if possible)?

(e) The proper functionality of which circuit(s) depends on the size of the devices? (Note that they are designed for a digital inverter)

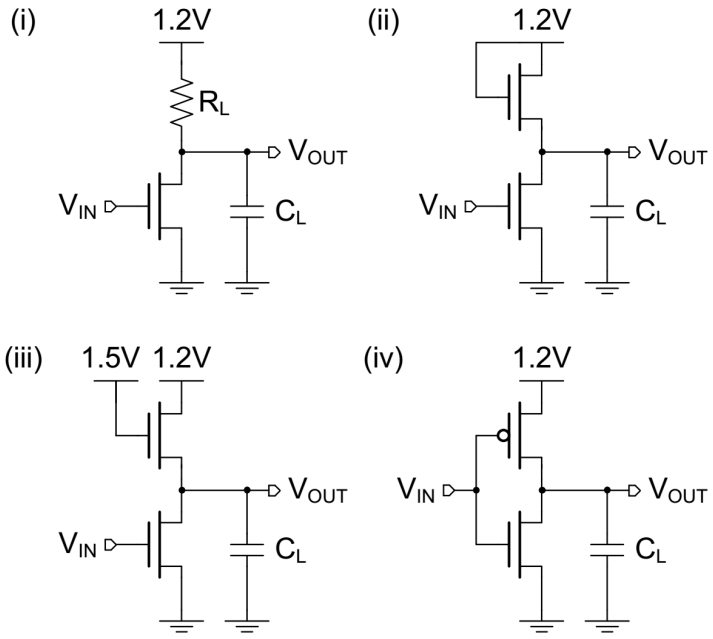

Figure 3

4. **NMOS Inverter - manual analysis**
Consider a NMOS inverter shown in Figure 4.

(a) Calculate V_{OH}, V_{OL} and V_M.

(b) Derive expressions for V_{IL}, V_{IH} and hence determine the noise margin. You may ignore channel length modulation in your analysis.

(c) Derive an expression for the peak gain and estimate the same.

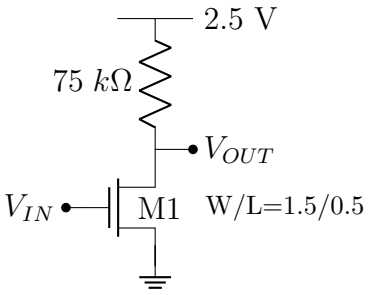

Figure 4

5. **NMOS Inverter- SPICE simulations**
Compare the results of question 4 by performing simulations in SPICE with 180 models.

(a) Simulate the VTC and plot the gain of the inverter by calculating dV_{out}/dV_{in}.

(b) How does the load resistance impact the threshold and peak gain of the inverter? Verify by simulating for a wide range of resistances.

(c) Simulate the frequency response using transient analysis at $f = 250\ kHz$, 50% duty cycle and $C_L = 3\ pF$. Calculate t_r, t_f and t_p for the inverter. Are the rise and fall times equal? Why or why not? What are the geometric parameters that influence the maximum operating frequency of the inverter? What is the dynamic power dissipation assuming that the inverter is clocked at highest possible frequency?