# Homework Assignment 2

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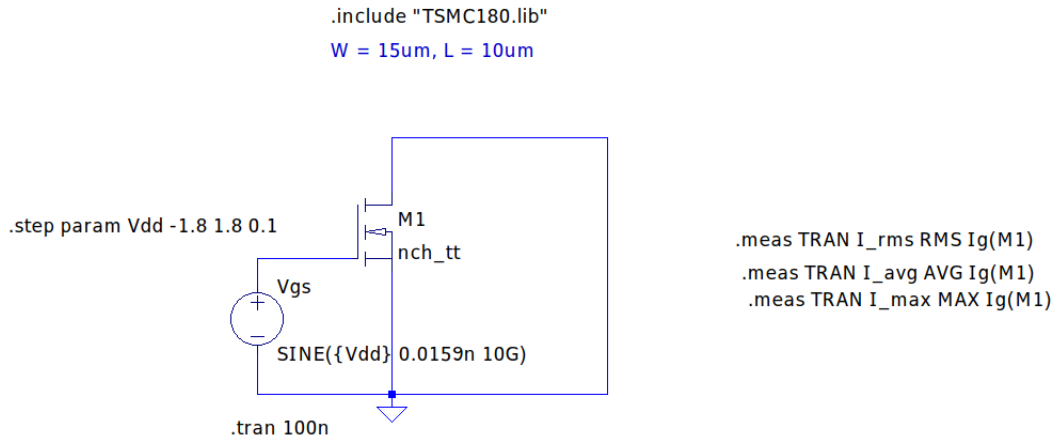
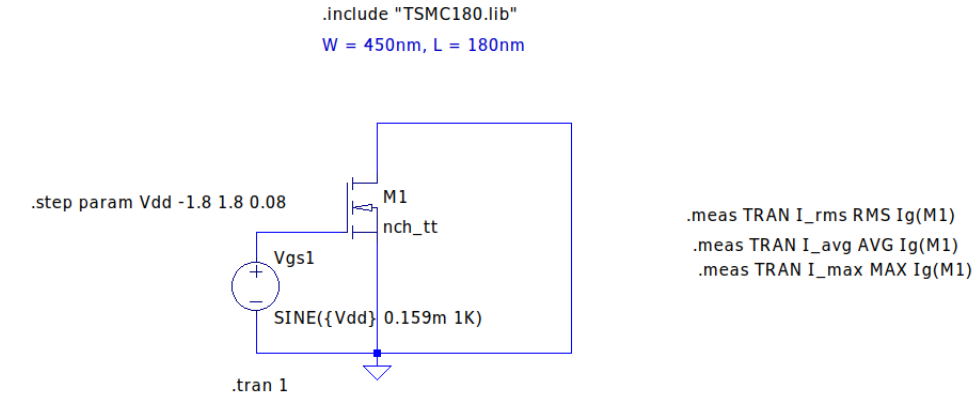
## 1 MOSFET Resistance

## 2 MOSFET Capacitance

**Long channel TestBench**

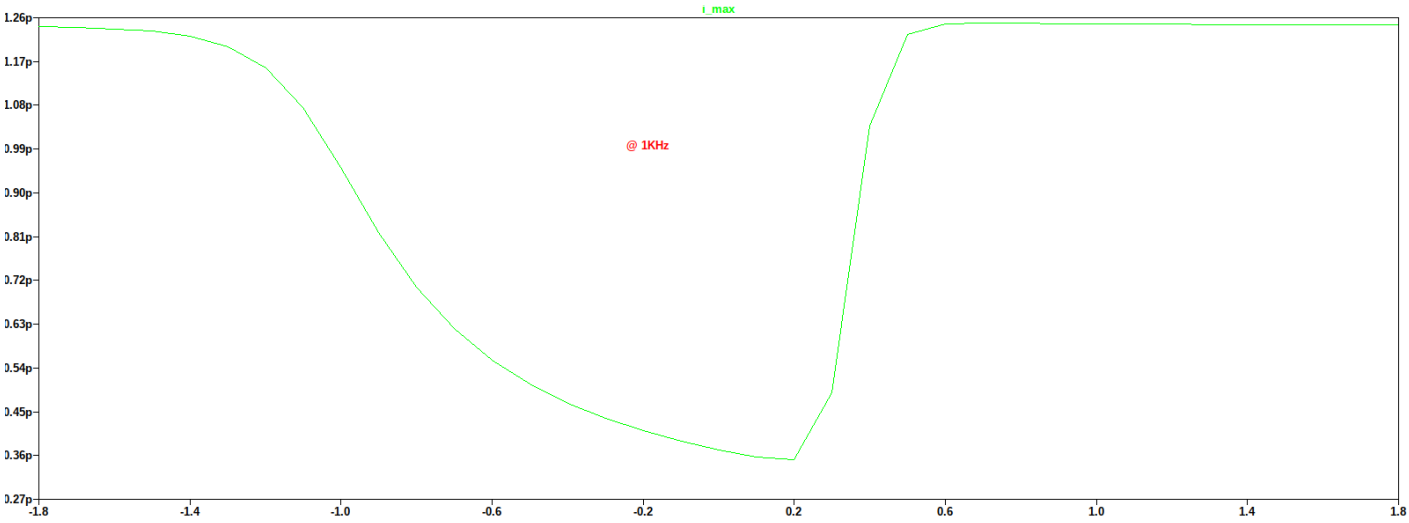



**Short channel TestBench**

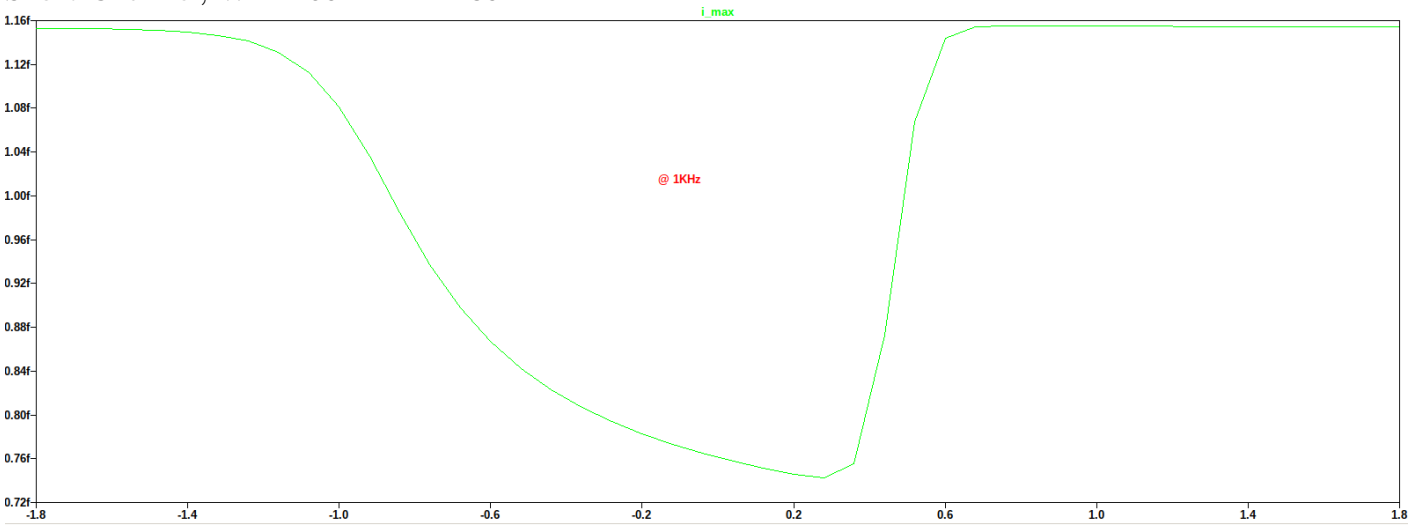



### (a)

This simulation was done @ 1KHz with AC amplitude of 0.159mV.
**Long Channel, W = 15$\mu$m L = 10$\mu$m**



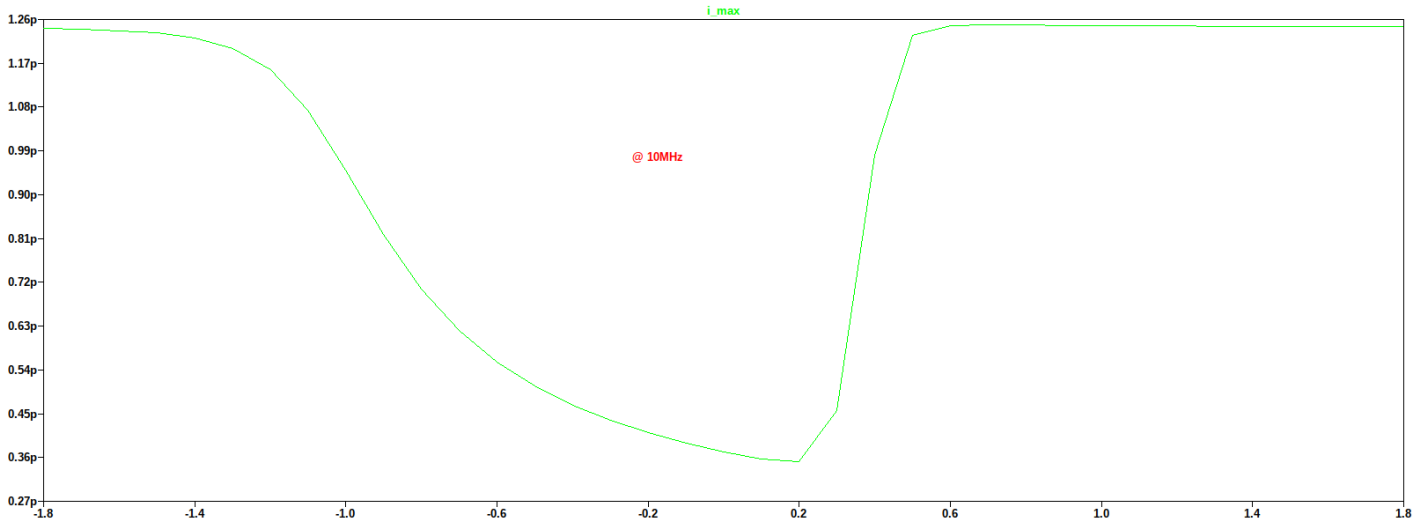

**Short Channel, W = 450nm L = 180nm**



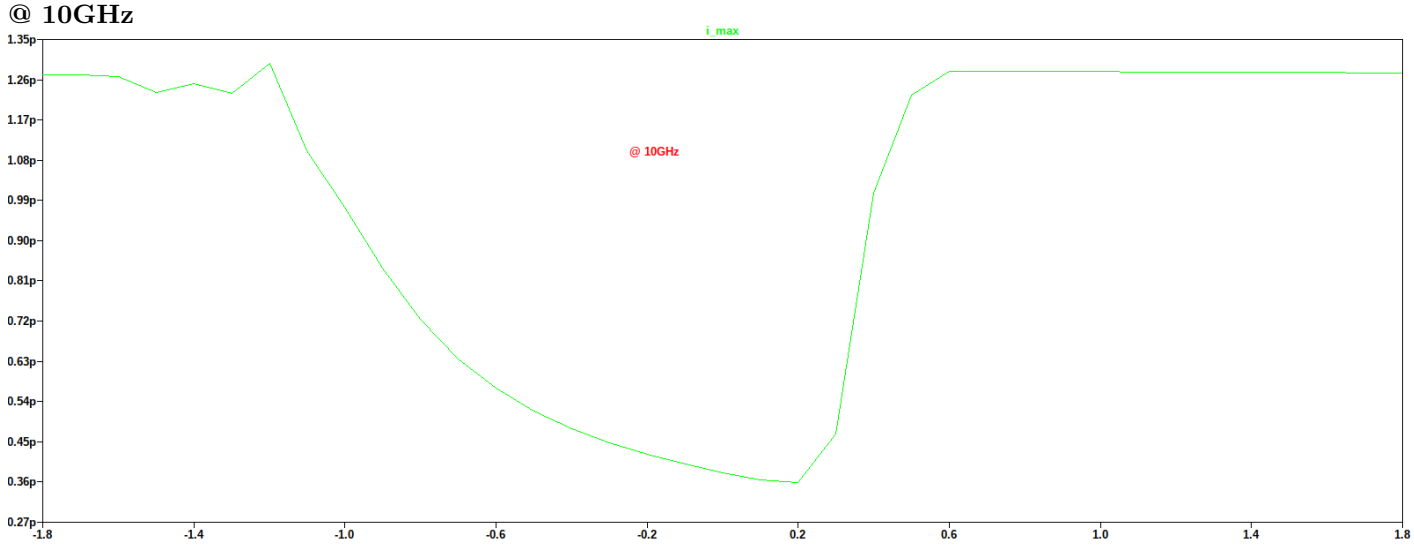

The above simulation follow same trends as *Figure 3.31(b) of Jon Rabaey*, We see that in both long and short channel the Capacitance observed to constant in regions when $V_{gs}$ is in range $[-1.8V, -1V] \bigcup [0.5V, 1.8V]$ and reduces from $[-1V, 0.2V]$ and increases in range of $[0.2V, 0.5V]$ in the case of Long channel, where as in Short channel reduces from $[-1V, 0.3V]$ and increases in range of $[0.3V, 0.5V]$.

## (b)

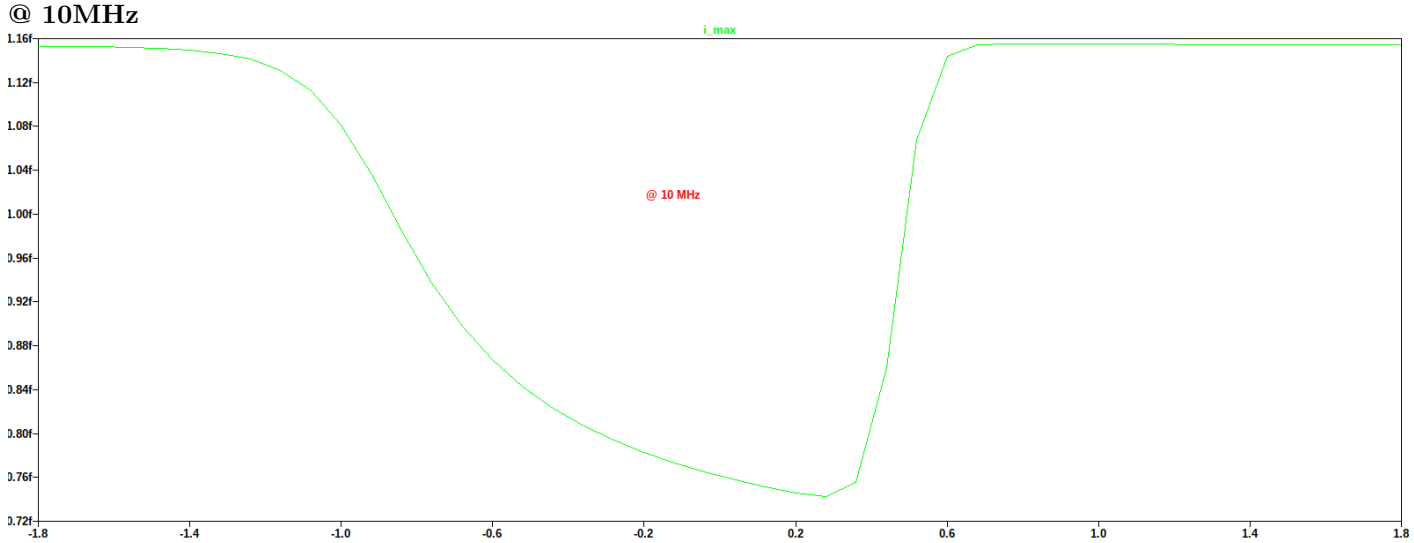
**Long Channel, W = 15$\mu$m L = 10$\mu$m**
**@ 10MHz**



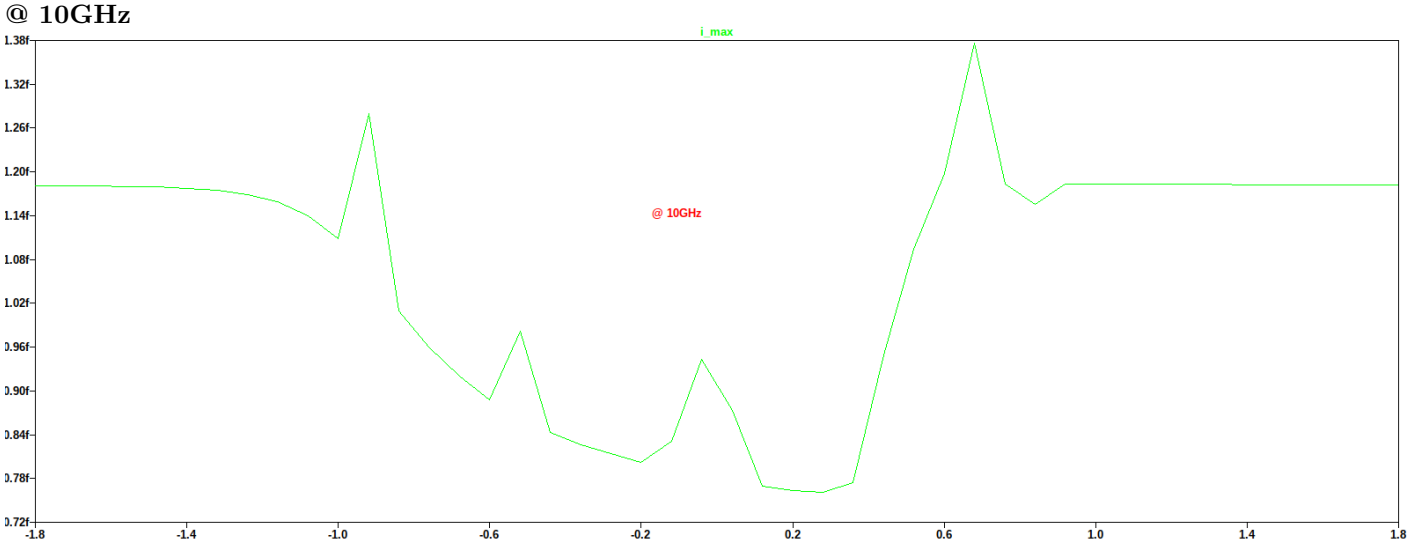

**@ 10GHz**




**Short Channel, W = 15$\mu$m L = 10$\mu$m**
**@ 10MHz**



**@ 10GHz**




In CV characteristics @ 10MHz and 10GHz we see that there is lot of bizzare behaviour, possible reasons can be due to high frequecncy behaviour of dieletic in mosfet affecting it's dielectric constant at high frequencies there by having bizzare capacitances.

# 3 Inverter Implementations

## (a) Which one(s) of the circuits consume(s) static power when the input is high ($V_{IN}$ = 1.2 V )?

***Circuit (i)***

This consumes static power as when input is HIGH, output would be LOW thus making a potential differnce across resistaor and as NMOS is in triode region it also conducts thus there would be a constant current flow accounting for ohmic losses.

***Circuit (ii)***

NMOS above is self-biased mosfet which is in saturation as $V_{ds}$=1.2-$V_{out}$ and $V_{gs}$=1.2-$V_{out}$, clearly $V_{ds} > V_{gs} - V_T$. There by a constant DC current would flow through MOS creating ohmic losses.

***Circuit (iii)***

This is same case as that Circuit (ii) but here $V_{ds} = V_{gs} - V_T$, here also a DC current flows causing ohmic loss.

## (b) Which one(s) of the circuits consume(s) static power when the input is low($V_{IN}$ = 0 V )?

***None of these circuits will draw static power when INPUT is LOW.***

## (c) $V_{OH}$ of which circuit(s) is 1.2 V (if possible)?

*Circuit (i)*

If $V_{in}$ is zero, that means NMOS is in cut-off region thus no current flows. Now this effectively is a RC circuit while output voltage is the voltage accros capacitor given sufficient time the capacitor indeed charges to max value.

*Circuit (iii)*
In circuit(ii),upper NMOS is in saturation and when $V_g = V_d = 1.2V$, the device cannot pass HIGH but has a drop of $V_T$. Whereas here in this circuit the gate has a voltage of 1.5 which is 1.2+0.3(=$V_T$). Thus here HIGH would pass without drop. There by this topology can pull HIGH.

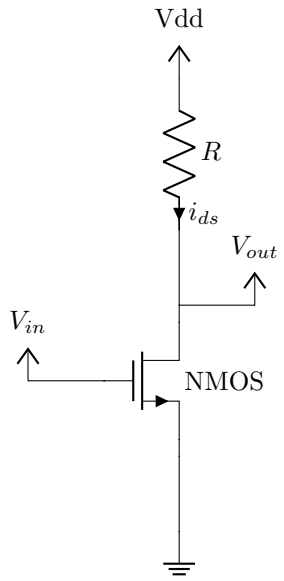
*Circuit(iv)*
Clearly PMOS passes HIGH thus pulling up the output voltage to 1.2V.

### (d) $V_{OL}$ of which circuit(s) is 0 V (if possible)?

*Circuit(i)*, *Circuit(ii)*, *Circuit(iii)* and *Circuit(iv)*
All topologies have NMOS's drain as output and we know that NMOS is very good at passing LOW, there by pulls the output or discharges the output voltage to 0V.

### (e) The proper functionality of which circuit(s) depends on the size of the devices? (Note that they are designed for a digital inverter)

## 4 NMOS Inverter - manual analysis




**Parameters**,Taken from *TSMC180.lib* file
$\beta_n$ = 2*170.1$\mu$A/$V^2$
W/L = 1.5
$V_T$ = 0.4V

Clearly,

$$V_{out} = Vdd - i_{ds}R$$

And $i_{ds}$ depends on region on operation of the NMOS.
**Case(i) $V_{in} < V_T$, Cut-off region**

$$i_{ds} = 0 \implies \boxed{V_{out} = Vdd}$$

$$\boxed{Gain = \frac{\partial V_{out}}{\partial V_{in}} = 0}$$

**Case(ii)** $V_T < V_{in} < V_{sl}$**, Saturation region**
Where $V_{sl}$ is point where MOSFET changes its region of operation from saturation to triode region.

$$i_{ds} = \beta_n \frac{W}{2L}(V_{in} - V_T)^2$$

$$\implies \boxed{V_{out} = Vdd - \beta_n \frac{W}{2L} R(V_{in} - V_T)^2}$$

$$@V_{in} = V_{sl}; V_{out} = V_{in} - V_T$$

$$\implies V_{in} - V_T = Vdd - \beta_n \frac{W}{2L} R(V_{in} - V_T)^2$$

$$V_{in} - V_T = \frac{-1 \pm \sqrt{1 + 2\beta_n \frac{W}{L} RVdd}}{\beta_n \frac{W}{L} R}$$

$$\implies \boxed{V_{sl} = V_T + \frac{\sqrt{1 + 2\beta_n \frac{W}{L} RVdd} - 1}{\beta_n \frac{W}{L} R}}$$

$$\boxed{Gain = \frac{\partial V_{out}}{\partial V_{in}} = -\beta_n \frac{W}{L} R(V_{in} - V_T)}$$

**Case(iii)** $V_{in} > V_{sl}$**, Triode region**

$$i_{ds} = \beta_n \frac{W}{L}((V_{in} - V_T)^2 V_{out} - \frac{{V^2}_{out}}{2})$$

$$\implies V_{out} = Vdd - \beta_n \frac{W}{L} R((V_{in} - V_T)^2 V_{out} - \frac{{V^2}_{out}}{2})$$

$$V_{out} = \frac{\left(1 + \beta_n \frac{W}{L} R(V_{in} - V_T)\right) \pm \sqrt{\left(1 + \beta_n \frac{W}{L} R(V_{in} - V_T)\right)^2 - 2\beta_n \frac{W}{L} RVdd}}{\beta_n \frac{W}{L} R}$$

Intutively $V_{out}$ should decrease when $V_{in}$ increase thus we should take only the - case root, as its slope might be negative but in + case root the slope is always +ve there by increasing $V_{out}$ with $V_{in}$. This is contradiction with our assumption thus - case root is only possible solution.

$$V_{out} = \frac{\left(1+\beta_n \frac{W}{L} R(V_{in}-V_T)\right) - \sqrt{\left(1+\beta_n \frac{W}{L} R(V_{in}-V_T)\right)^2 - 2\beta_n \frac{W}{L} RVdd}}{\beta_n \frac{W}{L} R}$$

$$\implies \quad Gain = \frac{\partial V_{out}}{\partial V_{in}} = 1 - \frac{\left(1+\beta_n \frac{W}{L} R(V_{in}-V_T)\right)}{\sqrt{\left(1+\beta_n \frac{W}{L} R(V_{in}-V_T)\right)^2 - 2\beta_n \frac{W}{L} RVdd}}$$

Finally puting everything in a compact form we get,

$$V_{out} = \begin{cases} Vdd & V_{in} < V_T \\ Vdd - \beta_n \frac{W}{2L} R(V_{in}-V_T)^2 & V_T < V_{in} < V_{sl} \\ V_{out} = \frac{\left(1+\beta_n \frac{W}{L} R(V_{in}-V_T)\right) - \sqrt{\left(1+\beta_n \frac{W}{L} R(V_{in}-V_T)\right)^2 - 2\beta_n \frac{W}{L} RVdd}}{\beta_n \frac{W}{L} R} & V_{in} > V_{sl} \end{cases} \tag{1}$$

$$Gain = \frac{\partial V_{out}}{\partial V_{in}} = \begin{cases} 0 & V_{in} < V_T \\ -\beta_n \frac{W}{L} R(V_{in}-V_T) & V_T < V_{in} < V_{sl} \\ 1 - \frac{\left(1+\beta_n \frac{W}{L} R(V_{in}-V_T)\right)}{\sqrt{\left(1+\beta_n \frac{W}{L} R(V_{in}-V_T)\right)^2 - 2\beta_n \frac{W}{L} RVdd}} & V_{in} > V_{sl} \end{cases} \tag{2}$$

Where,

$$V_{sl} = V_T + \frac{\sqrt{1+2\beta_n \frac{W}{L} RVdd} - 1}{\beta_n \frac{W}{L} R} \tag{3}$$

## (a)

Switching threshould is when $V_{in} = V_{out} = V_M$, clearly this intersection point occurs only in saturation region.

$$V_M = Vdd - \beta_n \frac{W}{2L} R(V_M - V_T)^2 \implies V_M = V_T + \frac{-1 \pm \sqrt{1+2\beta_n \frac{W}{L} R(Vdd - V_T)}}{\beta_n \frac{W}{L} R}$$

Since voltage always is positive

$$V_M = V_T + \frac{\sqrt{1+2\beta_n \frac{W}{L} R(Vdd - V_T)} - 1}{\beta_n \frac{W}{L} R} \tag{4}$$

Using the specification of device, we get $V_M$ **= 706mV**.

$V_{OH}$ and $V_{OL}$ are output voltages when Gain=-1. One point occurus in Saturation and other in Triode.
**Case(i) In Saturation region**,

$$-1 = -\beta_n \frac{W}{L} R(V_{IL} - V_T)$$

$$\implies V_{IL} = V_T + \frac{1}{\beta_n \frac{W}{L} R} \tag{5}$$

Then corresponding $V_{OH}$ is,

$$V_{OH} = Vdd - \beta_n \frac{W}{2L} R(V_{IL} - V_T)^2$$

$$V_{OH} = Vdd - \frac{1}{2\beta_n \frac{W}{L} R} \tag{6}$$

Then $V_{OH}$ **is 2.487V**.

**Case(ii) In Triode region**,

$$-1 = 1 - \frac{\left(1 + \beta_n \frac{W}{L} R(V_{IH} - V_T)\right)}{\sqrt{\left(1 + \beta_n \frac{W}{L} R(V_{IH} - V_T)\right)^2 - 2\beta_n \frac{W}{L} RVdd}}$$

$$\implies \frac{\sqrt{\left(1 + \beta_n \frac{W}{L} R(V_{IH} - V_T)\right)^2 - 2\beta_n \frac{W}{L} RVdd}}{\left(1 + \beta_n \frac{W}{L} R(V_{IH} - V_T)\right)} = 2$$

Solving the above quadratic equation we get,

$$V_{IH} = V_T + 2\sqrt{\frac{2Vdd}{3\beta_n \frac{W}{L} R}} - \frac{1}{\beta_n \frac{W}{L} R} \tag{7}$$

Then corresponding $V_{OL}$ is,

$$V_{OL} = \frac{\left(1 + \beta_n \frac{W}{L} R(V_{IH} - V_T)\right) - \sqrt{\left(1 + \beta_n \frac{W}{L} R(V_{IH} - V_T)\right)^2 - 2\beta_n \frac{W}{L} RVdd}}{\beta_n \frac{W}{L} R}$$

$$V_{OL} = \frac{\left(1 + \beta_n \frac{W}{L} R(V_T + 2\sqrt{\frac{2Vdd}{3\beta_n \frac{W}{L} R}} - \frac{1}{\beta_n \frac{W}{L} R} - V_T)\right) - \sqrt{\left(1 + \beta_n \frac{W}{L} R(V_T + 2\sqrt{\frac{2Vdd}{3\beta_n \frac{W}{L} R}} - \frac{1}{\beta_n \frac{W}{L} R} - V_T)\right)^2 - 2\beta_n \frac{W}{L} RVdd}}{\beta_n \frac{W}{L} R}$$

$$\implies V_{OL} = \sqrt{\frac{2Vdd}{3\beta_n \frac{W}{L} R}} \tag{8}$$

Plugging the specification in to the above equation we get, $V_{OL}$ **as 209mV**.

## (b)

$V_{IL}$ and $V_{IH}$ are determined in equation (5) and (7) respectively.
Therefore Noise margins are obtained from equations (5), (7), (8) and (6),

$$NM_L = V_{IL} - V_{OL}$$

$$NM_L = V_T + \frac{1}{\beta_n \frac{W}{L} R} - \sqrt{\frac{2Vdd}{3\beta_n \frac{W}{L} R}} \tag{9}$$

Similary for $NM_H$

$$NM_H = V_{IH} - V_{OH}$$

$$NM_H = V_T - Vdd + 2\sqrt{\frac{2Vdd}{3\beta_n \frac{W}{L} R}} - \frac{1}{2\beta_n \frac{W}{L} R} \tag{10}$$

Plugging the specs in the above equations we get, $NM_L$ **as 217mV** and $NM_H$ **as -1.696V**.

### (c)

Peak gain occurs only when NMOS, swicthes from saturation to triode, as in saturaion the gain is linear and decreases with increase in $V_{in}$. And in triode region the gain increases with increase with $V_{in}$. Therefore, Gain@$V_{in} = V_{sl}$ is maximum(speaking in absolute terms).
Then from equation (3) we get,

$$gain_{max} = -\beta_n \frac{W}{L} R(V_{sl} - V_T)$$

$$\implies gain_{max} = 1 - \sqrt{1 + 2\beta_n \frac{W}{L} RVdd} \tag{11}$$

For this device we get, $gain_{max}$ **as -12.869**.

## 5 MOS Inverter- SPICE simulations

| **Parameter** | **Simulated** | **Calculated** | **Error(in %)** |
|---|---|---|---|
| $V_M$ | 709.162mV | 706mV | -0.446% |
| $V_{IL}$ | 409.587mV | 426mV | -4% |
| $V_{HL}$ | 818.226mV | 791mV | -3.327% |
| $V_{OL}$ | 159.3742mV | 209mV | **31.13%** |
| $V_{OH}$ | 2.454V | 2.487V | 1.345% |
| $NM_L$ | 250.2128mV | 217mV | **-13.27%** |
| $NM_H$ | -1.63577V | -1.696V | 3.68% |
| Peak gain | -8.758 | -12.869 | **46.9%** |