Homework Assignment 2

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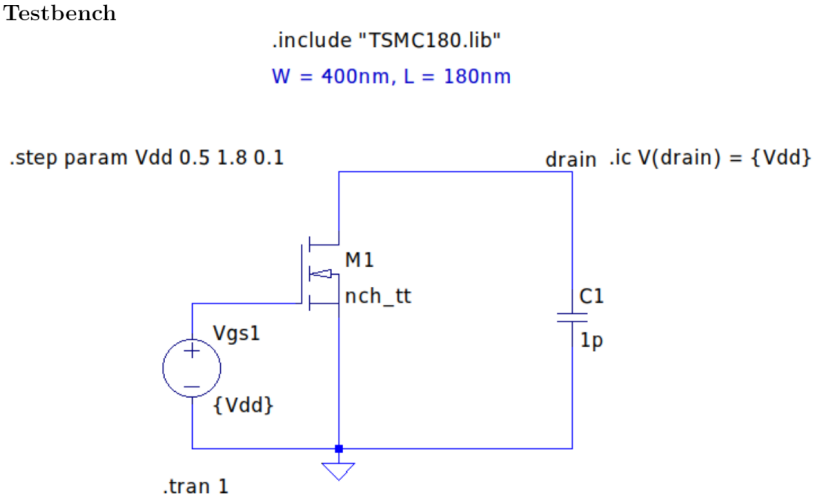
November 8, 2021

1 MOSFET Resistance

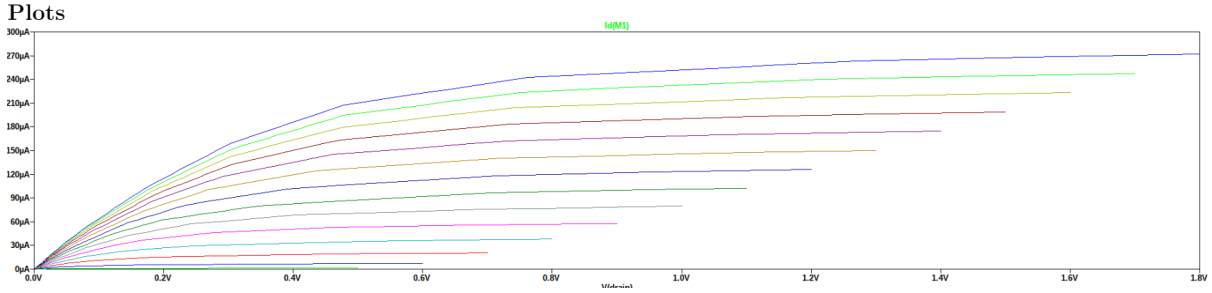
Taking W = 400nm and L = 180nm

(a)

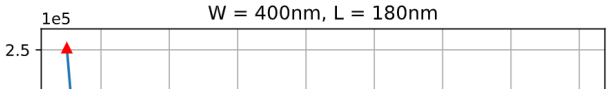
NMOS
Testbench

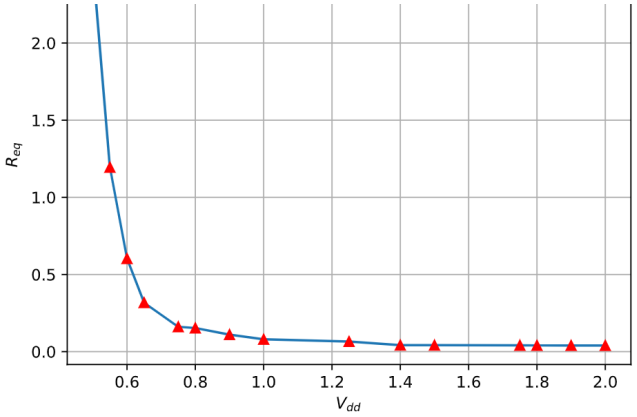


Plots



Here for different Vdd the transient simulation is done and the data is exported to python for integration from Vdd/2 to Vdd.



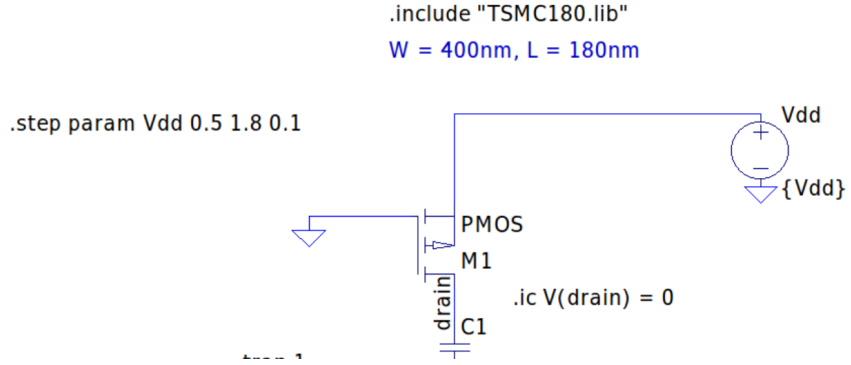


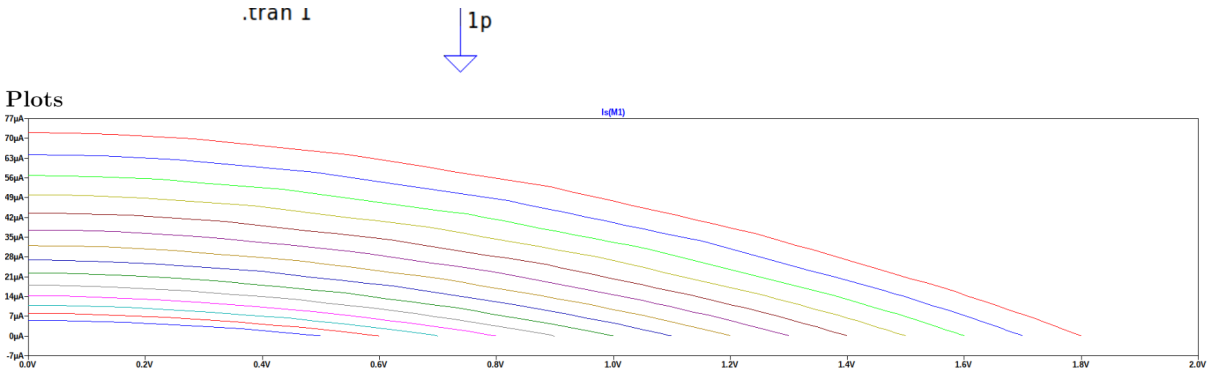
Python script for computing Req

```
import numpy as np
import matplotlib.pyplot as plt
from scipy import integrate
import matplotlib.ticker as ticker

data_points = [0.5, 0.55, 0.6, 0.65, 0.75, 0.8, 0.9, 1, 1.25, 1.4, 1.50, 1.75, 1.8, 1.9, 2]



def read_txt(data_point):
  file = open('Q1_nmos_400_180_{}.txt'.format(data_point), 'r')
  string = file.read()
  string = string.split('\n')
  n = len(string)
  vdd = []
  ids = []
  for i in range(1, n-1):
    d = string[i].split("\t")
    vdd.append(float(d[1]))
    ids.append(float(d[2]))
  vdd = np.array(vdd)
  ids = np.array(ids)
  idx = vdd >= (data_point/2)
  Req = -2*integrate.cumtrapz(vdd[idx]/ids[idx], vdd[idx])/data_point
  file.close()
  return np.max(np.absolute(Req))

Req = []
for d in data_points:
  print("_____________{}___________".format(d))
  Req.append(read_txt(d))
fig = plt.figure()
plt.title(r'W = 400nm, L = 180nm')
plt.plot(data_points, Req)
plt.plot(data_points, Req, "^", color='r')
plt.xlabel(r'$V_{dd}$')
plt.ylabel(r'$R_{eq}$')
plt.ticklabel_format(axis="y", style="sci", scilimits=(0,0))
plt.grid()
plt.savefig('../tex/figs/Q1_nmos_400_180_Req.eps')
plt.show()
```

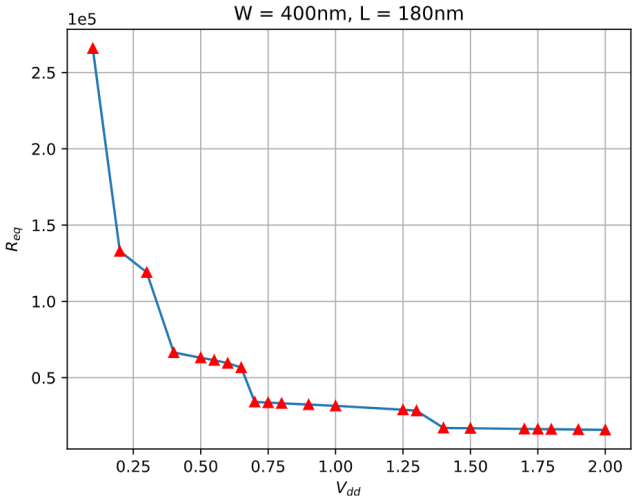

PMOS

Testbench





Here for different Vdd the transient simulation is done and the data is exported to python for integration from Vdd/2 to Vdd.

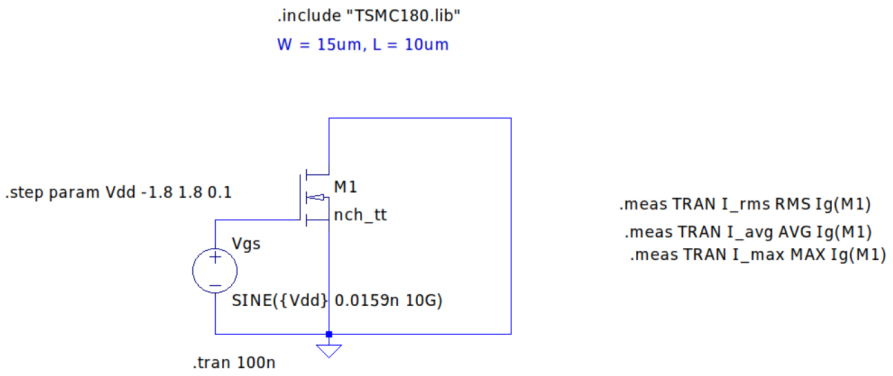


(b)

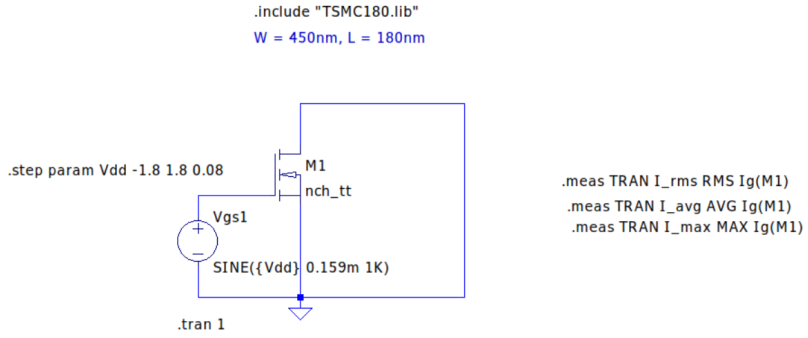
We see that in both NMOS and PMOS, Equivalent resistance is reducing with increase in Vdd hereby reducing propagation delay.But it is not the reducing Vdd improves the circuit but also increases the power consumption.
The simulation obtained here is similar that of *Figure 3.27.*

2 MOSFET Capacitance

Long channel TestBench

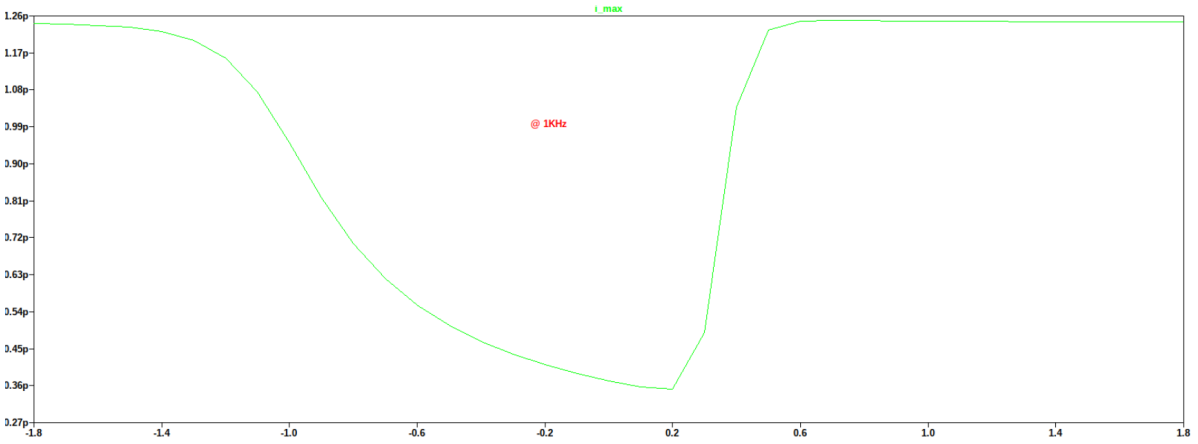


Short channel TestBench

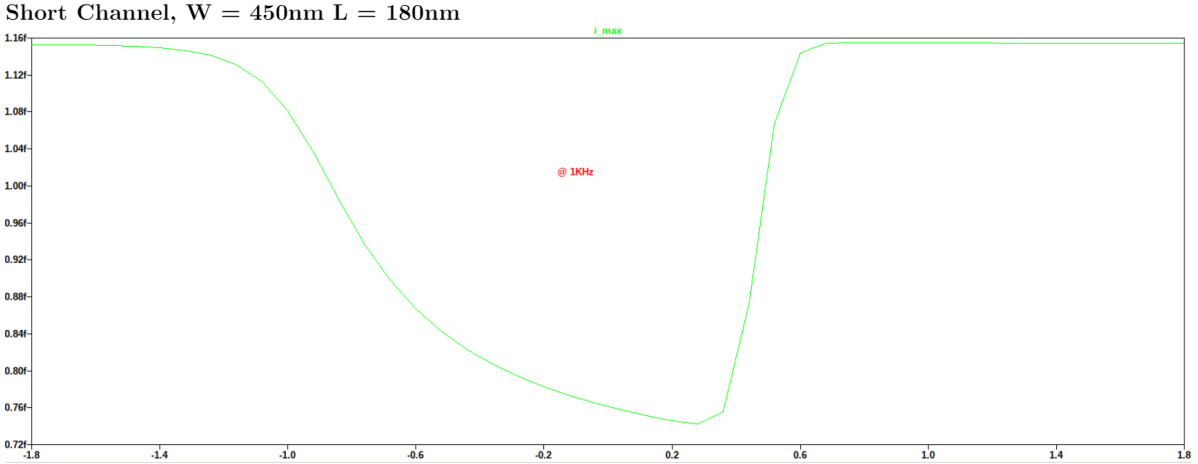


(a)

This simulation was done @ 1KHz with AC amplitude of 0.159mV.
Long Channel, W = 15μm L = 10μm



Short Channel, W = 450nm L = 180nm

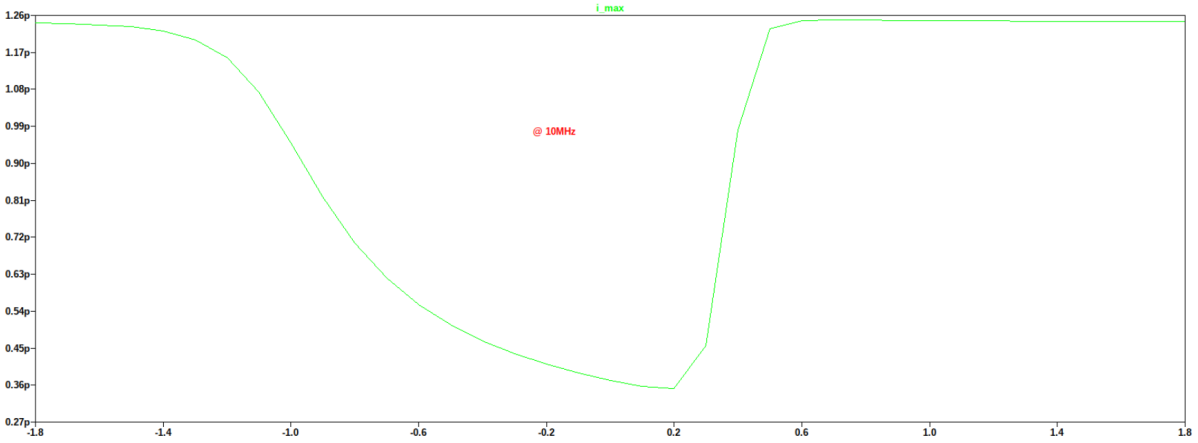


The above simulation follow same trends as *Figure 3.31(b) of Jon Rabaey*. We see that in both long and short

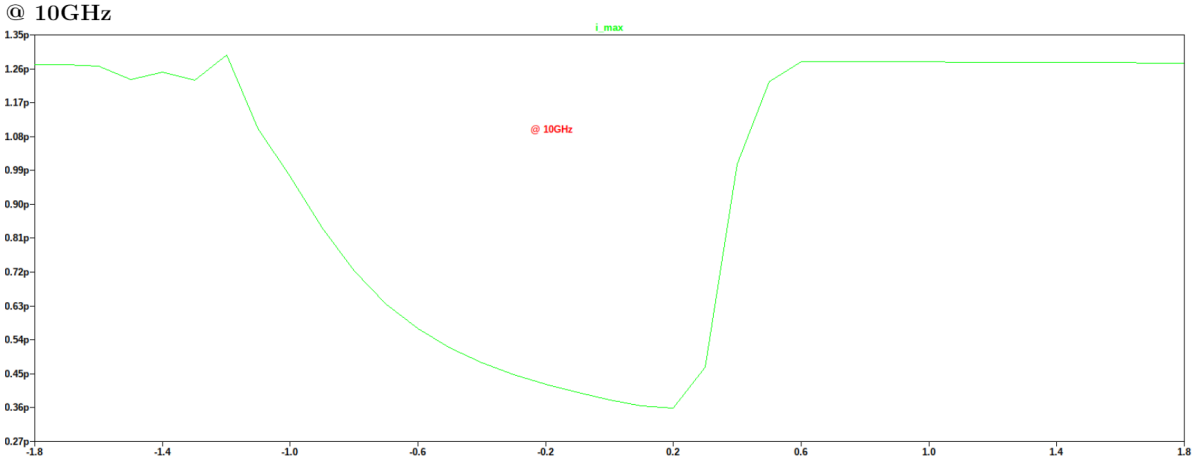
channel the Capacitance observed to constant in regions when V_{gs} is in range $[-1.8V, -1V] \bigcup [0.5V, 1.8V]$ and reduces from $[-1V, 0.2V]$ and increases in range of $[0.2V, 0.5V]$ in the case of Long channel, where as in Short channel reduces from $[-1V, 0.3V]$ and increases in range of $[0.3V, 0.5V]$.

(b)

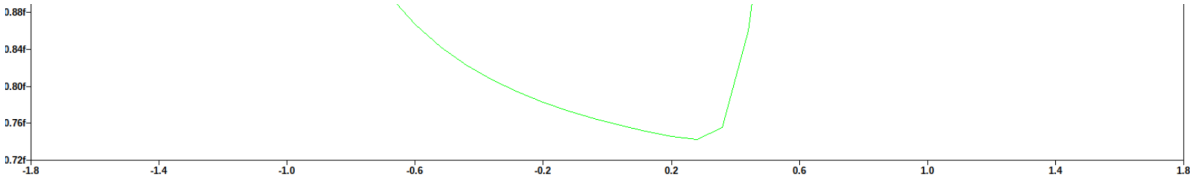
Long Channel, W = 15μm L = 10μm
@ 10MHz



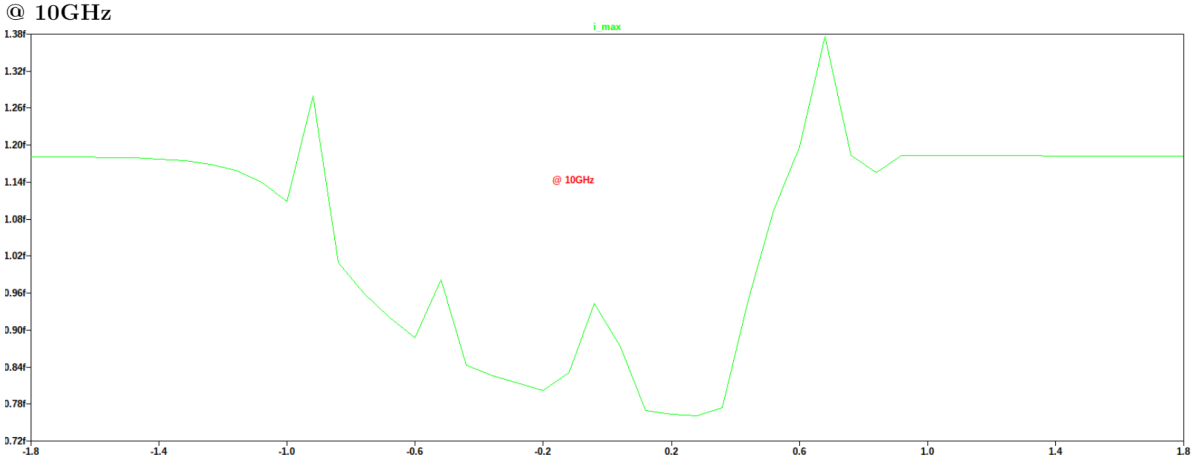
@ 10GHz



Short Channel, W = 15μm L = 10μm
@ 10MHz



@ 10GHz



In CV characteristics @ 10MHz and 10GHz we see that there is lot of bizzare behaviour, possible reasons can be due to high frequecncy behaviour of dieletic in mosfet affecting it's dielectric constant at high frequencies there by having bizzare capacitances.

3 Inverter Implementations

(a) Which one(s) of the circuits consume(s) static power when the input is high (V_{IN} = 1.2 V)?

Circuit (i)
This consumes static power as when input is HIGH, output would be LOW thus making a potential differnce across resistaor and as NMOS is in triode region it also conducts thus there would be a constant current flow accounting for ohmic losses.

Circuit (ii)
NMOS above is self-biased mosfet which is in saturation as V_{ds}=1.2-V_{out} and V_{gs}=1.2-V_{out}, clearly $V_{ds} > V_{gs} - V_T$. There by a constant DC current would flow through MOS creating ohmic losses.

Circuit (iii)
This is same case as that Circuit (ii) but here $V_{ds} = V_{gs} - V_T$, here also a DC current flows causing ohmic loss.

(b) Which one(s) of the circuits consume(s) static power when the input is low(V_{IN} = 0 V)?

None of these circuits will draw static power when INPUT is LOW.

(c) V_{OH} of which circuit(s) is 1.2 V (if possible)?

Circuit (i)
If V_{in} is zero, that means NMOS is in cut-off region thus no current flows. Now this effectively is a RC circuit while output voltage is the voltage accros capacitor given sufficient time the capacitor indeed charges to max value.

Circuit (iii)
In circuit(ii),upper NMOS is in saturation and when $V_g = V_d = 1.2V$, the device cannot pass HIGH but has a drop of V_T. Whereas here in this circuit the gate has a voltage of 1.5 which is 1.2+0.3(=V_T). Thus here HIGH would pass without drop. There by this topology can pull HIGH.

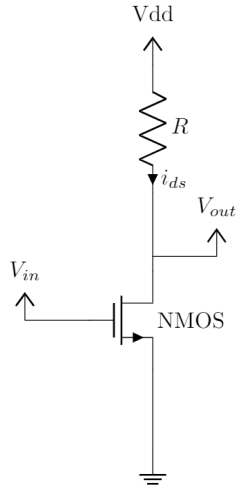
Circuit(iv)
Clearly PMOS passes HIGH thus pulling up the output voltage to 1.2V.

(d) V_{OL} of which circuit(s) is 0 V (if possible)?

Circuit(i), *Circuit(ii)*, *Circuit(iii)* and *Circuit(iv)*
All topologies have NMOS's drain as output and we know that NMOS is very good at passing LOW, there by pulls the output or discharges the output voltage to 0V.

(e) The proper functionality of which circuit(s) depends on the size of the devices? (Note that they are designed for a digital inverter)

4 NMOS Inverter - manual analysis



Parameters,Taken from *TSMC180.lib* file
β_n = 2*170.1μA/V^2
W/L = 1.5
V_T = 0.4V

Clearly,

$$V_{out} = Vdd - i_{ds}R$$

And i_{ds} depends on region on operation of the NMOS.
Case(i) $V_{in} < V_T$**, Cut-off region**

$$i_{ds} = 0 \implies \boxed{V_{out} = Vdd}$$

$$\boxed{Gain = \frac{\partial V_{out}}{\partial V_{in}} = 0}$$

Case(ii) $V_T < V_{in} < V_{sl}$**, Saturation region**
Where V_{sl} is point where MOSFET changes its region of operation from saturation to triode region.

$$i_{ds} = \beta_n \frac{W}{2L}(V_{in} - V_T)^2$$

$$\implies \boxed{V_{out} = Vdd - \beta_n \frac{W}{2L} R(V_{in} - V_T)^2}$$

$$@V_{in} = V_{sl}; V_{out} = V_{in} - V_T$$

$$\implies V_{in} - V_T = Vdd - \beta_n \frac{W}{2L} R(V_{in} - V_T)^2$$

$$V_{in} - V_T = \frac{-1 \pm \sqrt{1 + 2\beta_n \frac{W}{L} RVdd}}{\beta_n \frac{W}{L} R}$$

$$\implies \boxed{V_{sl} = V_T + \frac{\sqrt{1 + 2\beta_n \frac{W}{L} RVdd} - 1}{\beta_n \frac{W}{L} R}}$$

$$\boxed{Gain = \frac{\partial V_{out}}{\partial V_{in}} = -\beta_n \frac{W}{L} R(V_{in} - V_T)}$$

Case(iii) $V_{in} > V_{sl}$**, Triode region**

$$i_{ds} = \beta_n \frac{W}{L}((V_{in} - V_T)^2 V_{out} - \frac{{V^2}_{out}}{2})$$

$$\implies V_{out} = Vdd - \beta_n \frac{W}{L} R((V_{in} - V_T)^2 V_{out} - \frac{{V^2}_{out}}{2})$$

$$V_{out} = \frac{\left(1 + \beta_n \frac{W}{L} R(V_{in} - V_T)\right) \pm \sqrt{\left(1 + \beta_n \frac{W}{L} R(V_{in} - V_T)\right)^2 - 2\beta_n \frac{W}{L} RVdd}}{\beta_n \frac{W}{L} R}$$

Intutively V_{out} should decrease when V_{in} increase thus we should take only the - case root, as its slope might be negative but in + case root the slope is always +ve there by increasing V_{out} with V_{in}. This is contradiction with our assumption thus - case root is only possible solution.

$$\boxed{V_{out} = \frac{\left(1 + \beta_n \frac{W}{L} R(V_{in} - V_T)\right) - \sqrt{\left(1 + \beta_n \frac{W}{L} R(V_{in} - V_T)\right)^2 - 2\beta_n \frac{W}{L} RVdd}}{\beta_n \frac{W}{L} R}}$$

$$\implies \boxed{Gain = \frac{\partial V_{out}}{\partial V_{in}} = 1 - \frac{\left(1 + \beta_n \frac{W}{L} R(V_{in} - V_T)\right)}{\sqrt{\left(1 + \beta_n \frac{W}{L} R(V_{in} - V_T)\right)^2 - 2\beta_n \frac{W}{L} RVdd}}}$$

Finally puting everything in a compact form we get,

$$V_{out} = \begin{cases} Vdd & V_{in} < V_T \\ Vdd - \beta_n \frac{W}{2L} R(V_{in} - V_T)^2 & V_T < V_{in} < V_{sl} \\ V_{out} = \frac{\left(1+\beta_n \frac{W}{L} R(V_{in}-V_T)\right) - \sqrt{\left(1+\beta_n \frac{W}{L} R(V_{in}-V_T)\right)^2 - 2\beta_n \frac{W}{L} RVdd}}{\beta_n \frac{W}{L} R} & V_{in} > V_{sl} \end{cases} \tag{1}$$

$$Gain = \frac{\partial V_{out}}{\partial V_{in}} = \begin{cases} 0 & V_{in} < V_T \\ -\beta_n \frac{W}{L} R(V_{in} - V_T) & V_T < V_{in} < V_{sl} \\ 1 - \frac{\left(1+\beta_n \frac{W}{L} R(V_{in}-V_T)\right)}{\sqrt{\left(1+\beta_n \frac{W}{L} R(V_{in}-V_T)\right)^2 - 2\beta_n \frac{W}{L} RVdd}} & V_{in} > V_{sl} \end{cases} \tag{2}$$

Where,

$$V_{sl} = V_T + \frac{\sqrt{1 + 2\beta_n \frac{W}{L} RVdd} - 1}{\beta_n \frac{W}{L} R} \tag{3}$$

(a)

Switching threshould is when $V_{in} = V_{out} = V_M$, clearly this intersection point occurs only in saturation region.

$$V_M = Vdd - \beta_n \frac{W}{2L} R(V_M - V_T)^2 \implies V_M = V_T + \frac{-1 \pm \sqrt{1 + 2\beta_n \frac{W}{L} R(Vdd - V_T)}}{\beta_n \frac{W}{L} R}$$

Since voltage always is positive

$$V_M = V_T + \frac{\sqrt{1 + 2\beta_n \frac{W}{L} R(Vdd - V_T)} - 1}{\beta_n \frac{W}{L} R} \tag{4}$$

Using the specification of device, we get V_M **= 706mV**.

V_{OH} and V_{OL} are output voltages when Gain=-1. One point occurus in Saturation and other in Triode.

V_{OH} occurs when input is zero, from equation (1) we conclude that,

$$V_{OH} = Vdd \tag{5}$$

Similary when input is Vdd, Output is V_{OL}, then from equation (1) we get,

$$V_{OL} = \frac{\left(1 + \beta_n \frac{W}{L} R(Vdd - V_T)\right) - \sqrt{\left(1 + \beta_n \frac{W}{L} R(Vdd - V_T)\right)^2 - 2\beta_n \frac{W}{L} RVdd}}{\beta_n \frac{W}{L} R} \tag{6}$$

Using above equation and and plugging in the specification of device we get,
V_{OL} **as 31mV** and V_{OH} **as 2.5V**.

(b)

Case(i) In Saturation region,

$$\begin{aligned} -1 &= -\beta_n \frac{W}{L} R(V_{IL} - V_T) \\ \implies V_{IL} &= V_T + \frac{1}{\beta_n \frac{W}{L} R} \end{aligned} \tag{7}$$

Then corresponding V_{out} is,

$$\begin{aligned} V_{out} &= Vdd - \beta_n \frac{W}{2L} R(V_{IL} - V_T)^2 \\ V_{out} &= Vdd - \frac{1}{2\beta_n \frac{W}{L} R} \end{aligned} \tag{8}$$

Then V_{IL} **is 426mV**.

Case(ii) In Triode region,

$$-1 = 1 - \frac{\left(1 + \beta_n \frac{W}{L} R(V_{IH} - V_T)\right)}{\sqrt{\left(1 + \beta_n \frac{W}{L} R(V_{IH} - V_T)\right)^2 - 2\beta_n \frac{W}{L} RVdd}}$$

$$\sqrt{\left(1 + \beta_n \frac{W}{L} R(V_{IH} - V_T)\right)^2 - 2\beta_n \frac{W}{L} RVdd}$$

$$\implies \frac{}{\left(1+\beta_n\frac{W}{L}R(V_{IH}-V_T)\right)} = 2$$

Solving the above quadratic equation we get,

$$V_{IH} = V_T + 2\sqrt{\frac{2Vdd}{3\beta_n\frac{W}{L}R}} - \frac{1}{\beta_n\frac{W}{L}R} \tag{9}$$

Then corresponding V_{out} is,

$$V_{out} = \frac{\left(1+\beta_n\frac{W}{L}R(V_{IH}-V_T)\right) - \sqrt{\left(1+\beta_n\frac{W}{L}R(V_{IH}-V_T)\right)^2 - 2\beta_n\frac{W}{L}RVdd}}{\beta_n\frac{W}{L}R}$$

$$V_{OL} = \frac{\left(1+\beta_n\frac{W}{L}R(V_T+2\sqrt{\frac{2Vdd}{3\beta_n\frac{W}{L}R}}-\frac{1}{\beta_n\frac{W}{L}R}-V_T)\right) - \sqrt{\left(1+\beta_n\frac{W}{L}R(V_T+2\sqrt{\frac{2Vdd}{3\beta_n\frac{W}{L}R}}-\frac{1}{\beta_n\frac{W}{L}R}-V_T)\right)^2 - 2\beta_n\frac{W}{L}RVdd}}{\beta_n\frac{W}{L}R}$$

$$\implies V_{out} = \sqrt{\frac{2Vdd}{3\beta_n\frac{W}{L}R}} \tag{10}$$

Plugging the specification in to the above equation we get, V_{IH} **as 791mV**.

V_{IL} and V_{IH} are determined in equation (7) and (9) respectively.
Therefore Noise margins are obtained from equations (7), (9), (4) and (4),

$$NM_L = V_{IL} - V_{OL}$$

$$NM_L = V_T + \frac{1}{\beta_n\frac{W}{L}R} - \sqrt{\frac{2Vdd}{3\beta_n\frac{W}{L}R}} \tag{11}$$

Similary for NM_H

$$NM_H = V_{IH} - V_{OH}$$

$$NM_H = V_T - Vdd + 2\sqrt{\frac{2Vdd}{3\beta_n\frac{W}{L}R}} - \frac{1}{2\beta_n\frac{W}{L}R} \tag{12}$$

Plugging the specs in the above equations we get, NM_L **as 425mV** and NM_H **as -1.666V**.

(c)

Peak gain occurs only when NMOS, swicthes from saturation to triode, as in saturaion the gain is linear and decreases with increase in V_{in}. And in triode region the gain increases with increase with V_{in}. Therefore, Gain@$V_{in} = V_{sl}$ is maximum(speaking in absolute terms).
Then from equation (3) we get,

$$gain_{max} = -\beta_n\frac{W}{L}R(V_{sl}-V_T)$$

$$\implies gain_{max} = 1 - \sqrt{1+2\beta_n\frac{W}{L}RVdd} \tag{13}$$

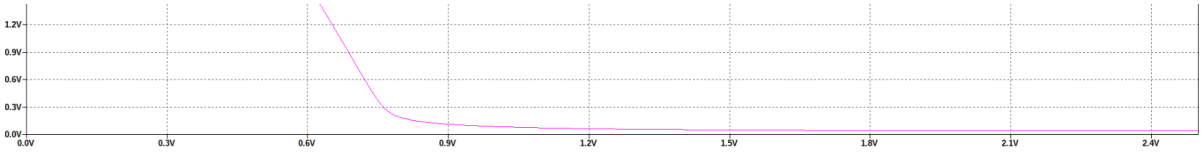
For this device we get, $gain_{max}$ **as -12.869**.

5 MOS Inverter- SPICE simulations

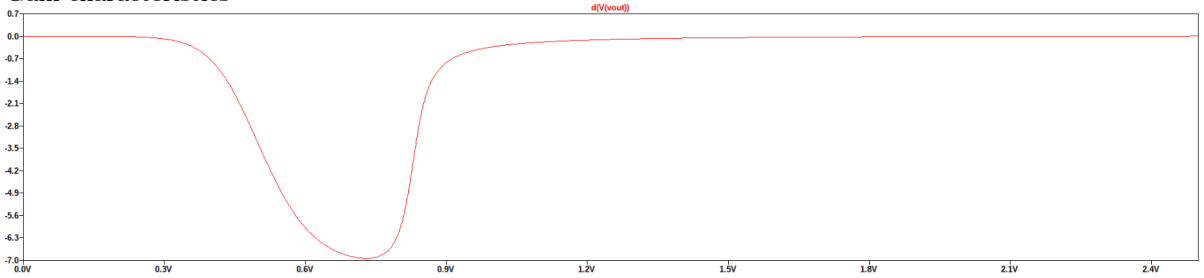
Parameter	Simulated	Calculated	Error(in %)
V_M	755mV	706mV	-6.5%
V_{IL}	414.74mV	426mV	-2.7%
V_{IH}	818.226mV	791mV	-3.327%
V_{OL}	57.8mV	31mV	1.13%
V_{OH}	2.5V	2.5V	0%
NM_L	250.2128mV	425mV	**-13.27%**
NM_H	-1.63577V	-1.666V	3.68%
Peak gain	-6.935	-12.869	**46.9%**

(a)

VTC

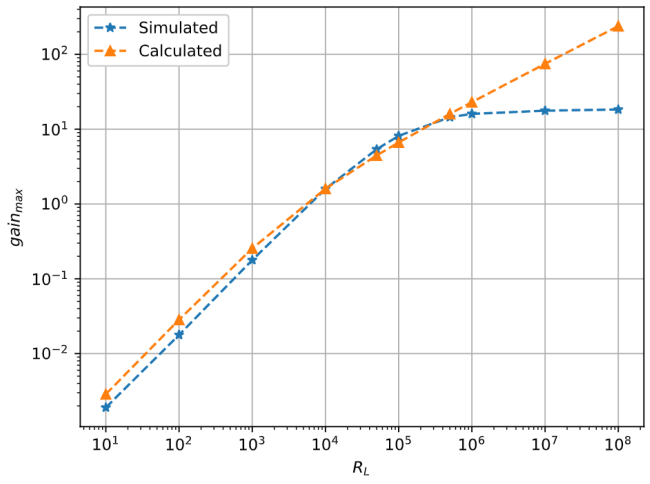


Gain characteristics



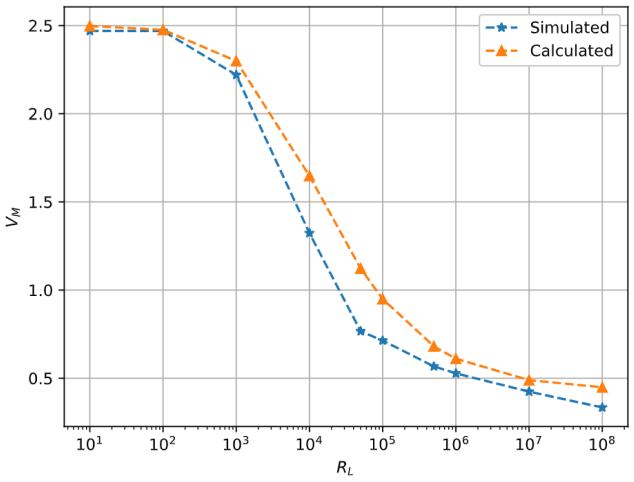
(b)

Gain variation with Load resistance



Load resistance	Simulated	Calculated
10Ω	-1.9m	-12.6m
100Ω	-17.8m	-120.03m
1KΩ	-178m	-880m
10KΩ	-1.59	-4.49
50KΩ	-5.39	-10.34
100KΩ	-8.14	-15
500KΩ	-14.46	-34.73
1MΩ	-16.01	-49.52
10MΩ	-17.67	-158.73
100MΩ	-18.34	-504.124

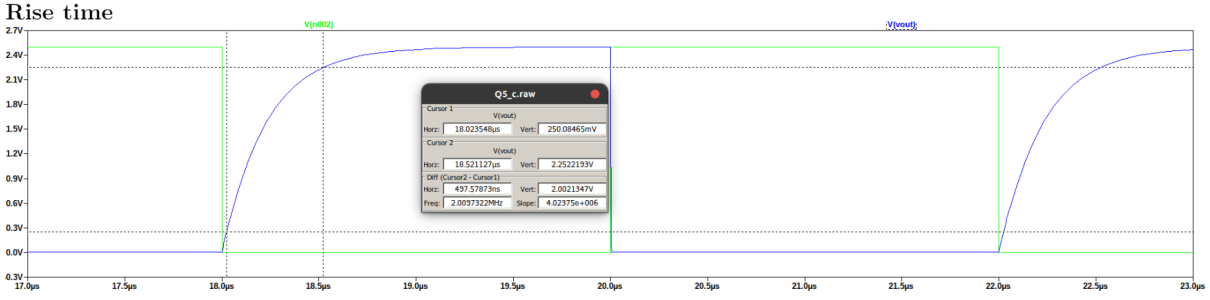
V_M variation with Load resistance



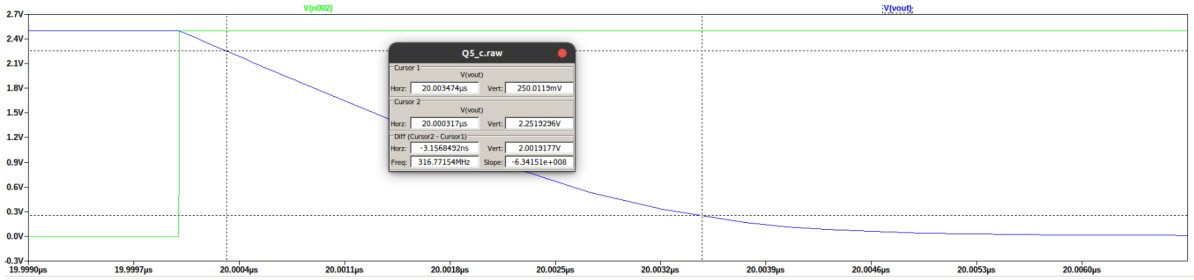
V_M	**Simulated**	**Calculated**
10Ω	2.496V	2.488V
100Ω	2.469V	2.398V
1KΩ	2.22V	1.9146V
10KΩ	1.323V	1.13V
50KΩ	766.796mV	768.416mV
100KΩ	713.73mV	667.95mV
500KΩ	567.32mV	524.44mV
1MΩ	527.65mV	488.7833mV
10MΩ	424mV	428.49mV
100MΩ	334.34mV	409.05mV

(c)

Rise time



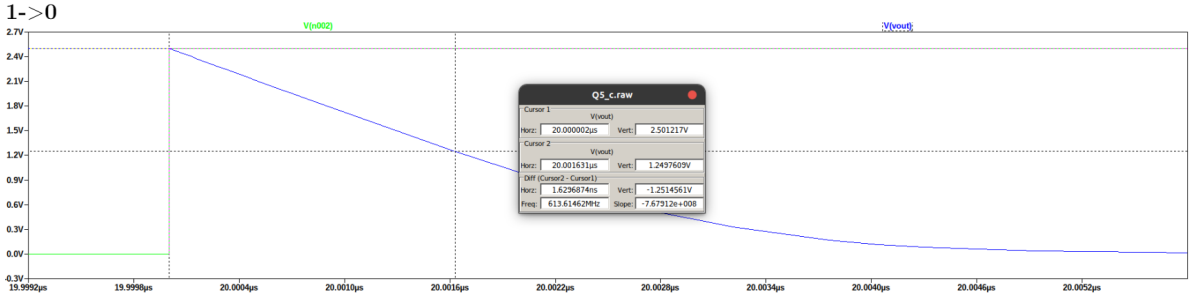
Fall time



Propagation delay

0− >1

1->0



Metric	Simulated	Calculated
t_r	497.58ns	
t_f	3.157ns	
t_p	80.93ns	