# Introduction (*Heading 1*)

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New spice netlist was generated. Now we need the library files of nmos and pmos for skywater pdk. From the workshop we only get sky\_fd\_sc\_hd pdk. We need to use sky\_fd\_pr. There are multiple n type fets and I decided to go with 1.8 nfet. I assume it means it operates on a VDD of 1.8V. Here, from corners.spice we can see there only a fixed W,L combinations of nfets. The paper I am referring to uses 0.5u meter technology and the initial goal was to scale those widths and lengths but appropriate weights and lengths are to be chosen from what's available and yet make sure functionality doesn’t change.

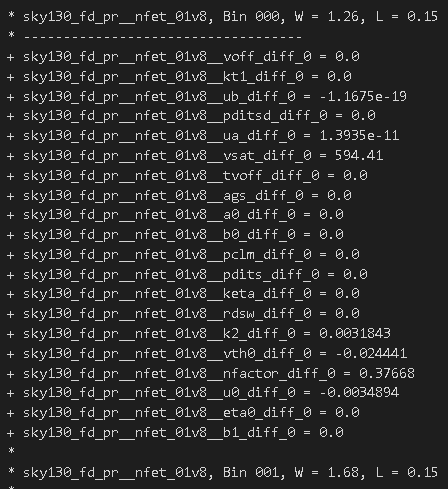
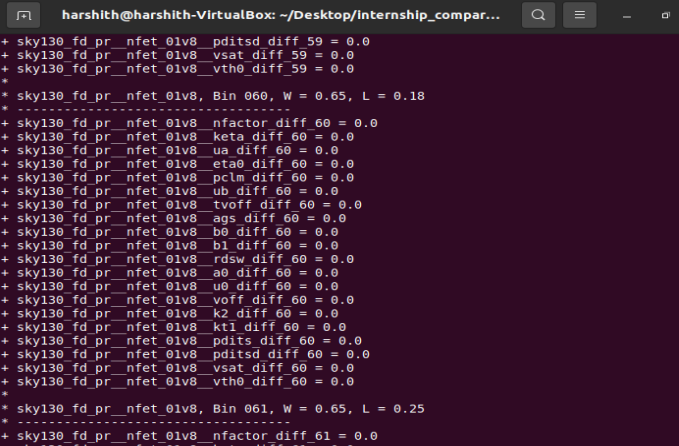


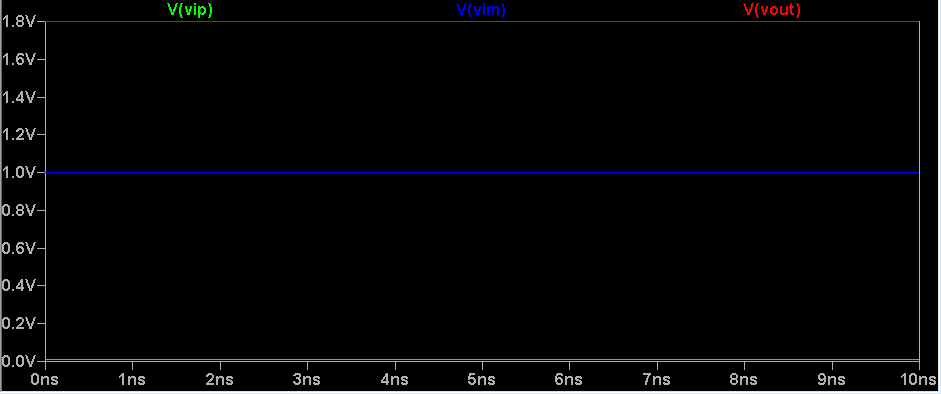
figure: screenshot of corners.spice file for slow corner and typical corner.

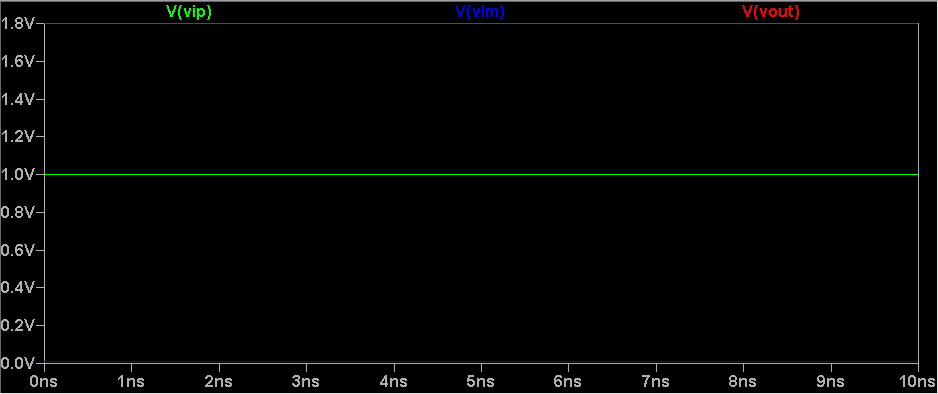
Although we might need to build our comparator for different corners. For now I’ve decided to do it for tt (typical) corner.

Vin is the input and Vim is the reference voltage.

1. **SIMULATION**

After I ran a simulation and got the following graph for vip > vim and vip < vim but the output stays high.





III. CONCLUSION

I think the weights are very limited. Design should be well understood and other W/L ratios from given lists should be used. More W/L exploration needs to be done.

IV. References

1. P. M. Furth, Y. Tsen, V. B. Kulkarni and T. K. Poriyani House Raju, "On the design of low-power CMOS comparators with programmable hysteresis," *2010 53rd IEEE International Midwest Symposium on Circuits and Systems*, Seattle, WA, 2010, pp. 1077-1080, doi: 10.1109/MWSCAS.2010.5548836.
2. https://wordpress.nmsu.edu/pfurth/files/2015/06/Comparators\_With\_Hysteresis\_Kulkarni\_2005.pdf