MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
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Manipal Institute of Technology

Department of Electronics and Communication Engineering

Course: ECE 5112 DIGITAL VLSI DESIGN

Assignment 2(Part A)

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Submitted to,

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Professor
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1. **Design a six-transistor CMOS SRAM cell and perform its simulation.**
    i. **Do the transistor sizing and calculate the cell ratio. Check the design for various modes of operation**
        a. **Standby mode**
        b. **Write Mode for both logic 0 and 1**
        c. **Read mode for both logic 0 and 1**
    ii. **Draw the stick diagram and layout of the cell. Perform the post-layout simulation and check whether both the results are relatively equal or not. If so, highlight the cause and possible remedies.**
    iii. **Calculate the various power dissipations during read and write mode.**
    iv. **Calculate the static noise margin (SNM) of your cell using the "butterfly curve."**
    v. **Perform the process corner analysis and discuss the effects of transistor sizing in the cell qualitatively.**
    vi. **Finally, Generate a GDS II file for your design.**

After all the analysis, Can you develop the design specification of your proposed SRAM cell?

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Static Random Access Memory, or SRAM, is a crucial component in VLSI chips due to its compact design, fast access speeds, and efficiency—especially useful in low-power applications like laptops, mobile devices, and IoT gadgets. As the demand for energy-efficient, high-performance electronics grows, researchers are working to create SRAM technology that balances low-voltage operation with stable, quick data access.

The 6T SRAM cell, named for its six-transistor design, stores each bit using a bistable latch, meaning it doesn't need the continuous refreshing required by Dynamic RAM (DRAM). While SRAM is still volatile and loses data when power is turned off, it offers much faster performance than DRAM, making it ideal for cache memory and applications where quick access is critical.

However, SRAM's six-transistor structure takes up more silicon area than DRAM, which has limited its use primarily to high-performance, low-power applications rather than as a main storage solution.

The cell's six transistors serve distinct roles:

- **2 Pull-Up Transistors** connect the storage nodes to the power supply (VDD).
- **2 Pull-Down Transistors** connect the storage nodes to the ground (GND).
- **2 Access Transistors** control the reading and writing of data through the bit lines (BL and BLB).

This design makes SRAM a robust choice for scenarios that need fast and efficient data retrieval.

1. ***Transistor Sizing, Cell Ratio and Modes of Operation:***

Transistors in SRAM are sized according to how effectively they can handle different operations, and SRAM cells can be optimized based on the specific performance goals. Here are the typical configurations:

High Density: When prioritizing compact design, the transistors are sized equally with a ratio of PU:AC:PD = 1:1:1.

High Current: To achieve higher current capacity, the access and pull-down transistors are larger relative to the pull-up transistor, using ratios like PU:AC:PD = 1:2:2 or 2:3:3.

High Performance: For high-speed performance, the pull-down transistor is made even larger to improve read and write speeds, with ratios such as PU:AC:PD = 1:2:3 or 2:3:4.

Here, PU, PA, and PD stand for the pull-up, access, and pull-down transistors, respectively, each adjusted based on the specific demands of density, current, or performance.

Here, the design has been done for High-performance mode.

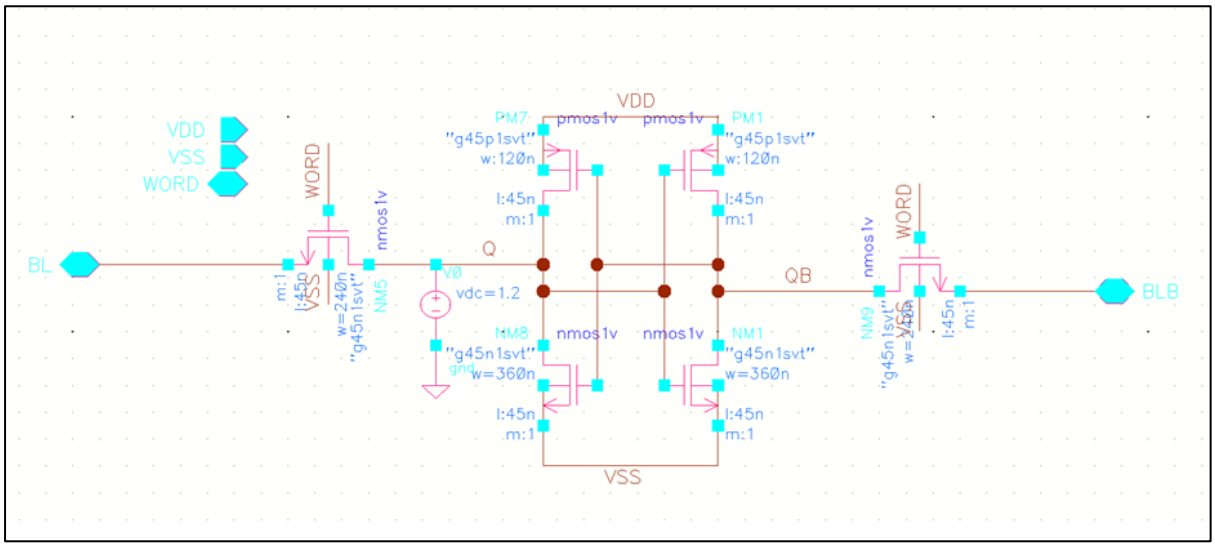


Fig.1: 6T SRAM Cell Schematic

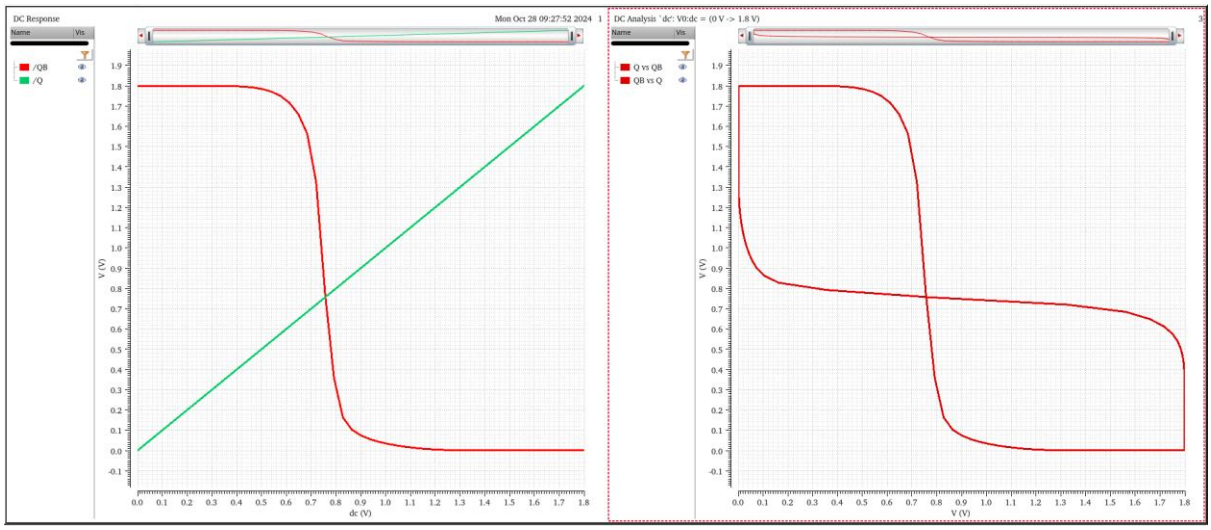


Fig. 2: DC Response and Butterfly Curve

To determine the Cell Ratio and Pull-up Ratio in an SRAM cell, we use widths (W) and lengths (L) of the transistors:

Cell Ratio: This is the ratio of the pull-down transistor size to the access transistor size.

$$\text{Cell Ratio} = \frac{\frac{W}{L}(\text{Pull} - \text{down})}{\frac{W}{L}(\text{Access})}$$

Pull-up Ratio: This is the ratio of the pull-up transistor size to the access transistor size

$$\text{Pull} - \text{up Ratio} = \frac{\frac{W}{L}(\text{Pull} - \text{up})}{\frac{W}{L}(\text{Access})}$$

W_{PU}=120nm, W_{AC}=240nm, W_{PD}= 360nm and L =45nm

$$\textbf{Cell Ratio} = \frac{360nm}{240nm} = \textbf{3:2 = 1.5}$$

$$\textbf{Pull-up Ratio} = \frac{120nm}{240nm} = \textbf{1:2 = 0.5}$$

Thus, the **Cell Ratio** is 1.5, and the **Pull-up Ratio** is 0.5.

6T SRAM CELL OPERATION MODES :

a) *Standby mode:*

It is retention or hold mode.

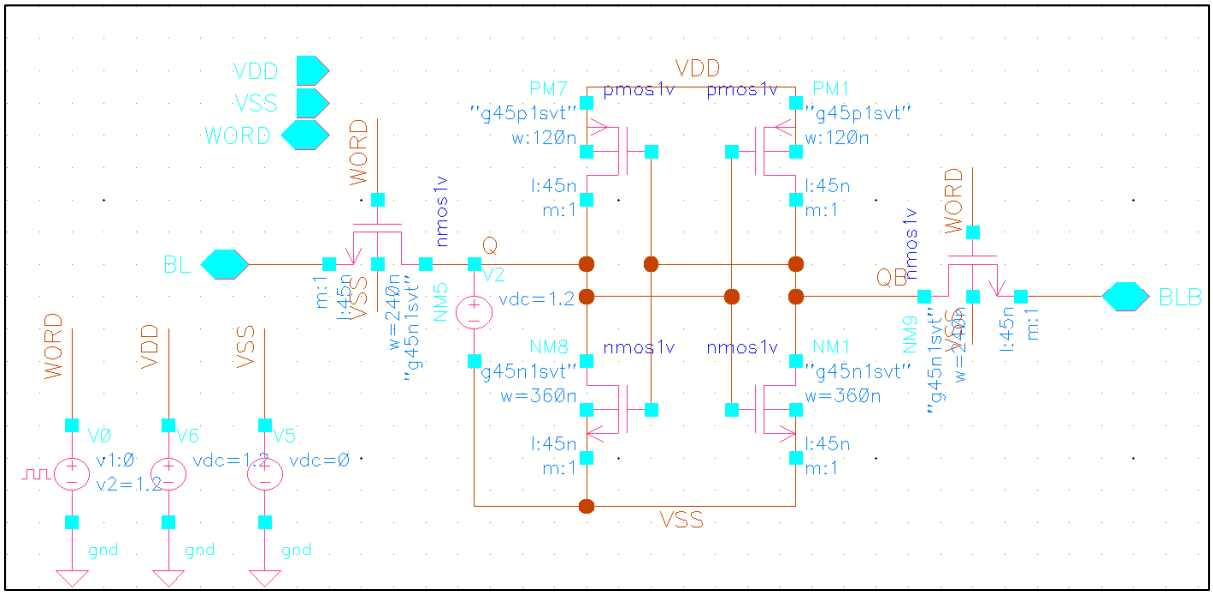


Fig. 3: Schematic of 6T SRAM for Standby Mode

Access transistors are cut-off by making WORD line = 0

Q and QB will retain the voltage levels they already possess.

Here Q=1.2 V and QB= 0V

This value is retained when WORD line=0

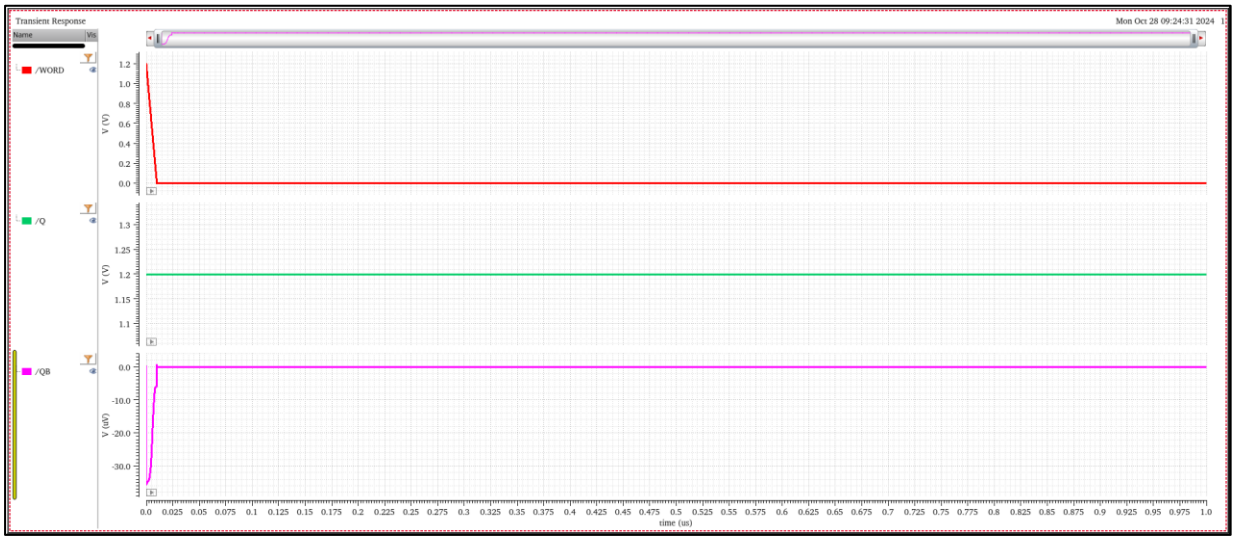


Fig. 4: Waveform of 6T SRAM for Standby Mode

b) *Write Mode for logic 0:*

In an SRAM cell, a pre-charge circuit sets the bit lines for writing data: **BLB** is pulled up to **VDD** (high voltage), and **BL** is pulled down to **0 V** to prepare for writing a '0'. In this case:

- **Q** is set at **1.2V** and **QB** at **0V**.

When the **WORD Line** (set to 1) is activated, current flows through the access transistors, allowing data to be written into the bit cell. After writing '0', **BL** is charged to **VDD**, and **BLB** is discharged to **0V**.

In the SRAM schematic, considering the left side:

- As the access transistor attempts to discharge **Q**, the pull-up transistor simultaneously tries to charge it. This creates a "tug-of-war" between the access transistor and the pull-up transistor.

On the right side:

- The pull-down network tries to discharge **QB**, while the access transistor tries to charge it. To hold a '1' at **QB**, **Q** must be pulled down enough so that the right-side pull-down network remains off.

For a successful write operation, **Q** should be discharged by the access transistor faster than the pull-up network can recharge it, effectively beginning the write process by setting '0' on the side where '1' was previously stored.

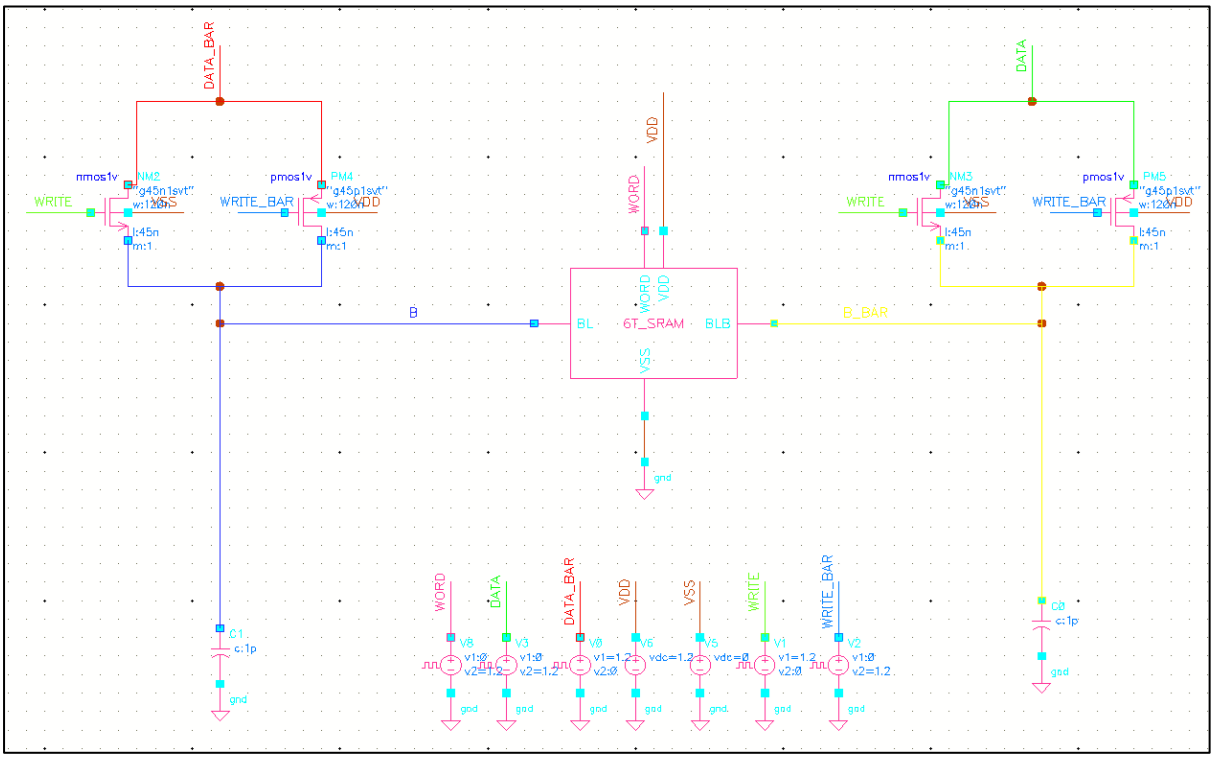


Fig. 5: Schematic of 6T SRAM for Write ‘0’ Operation

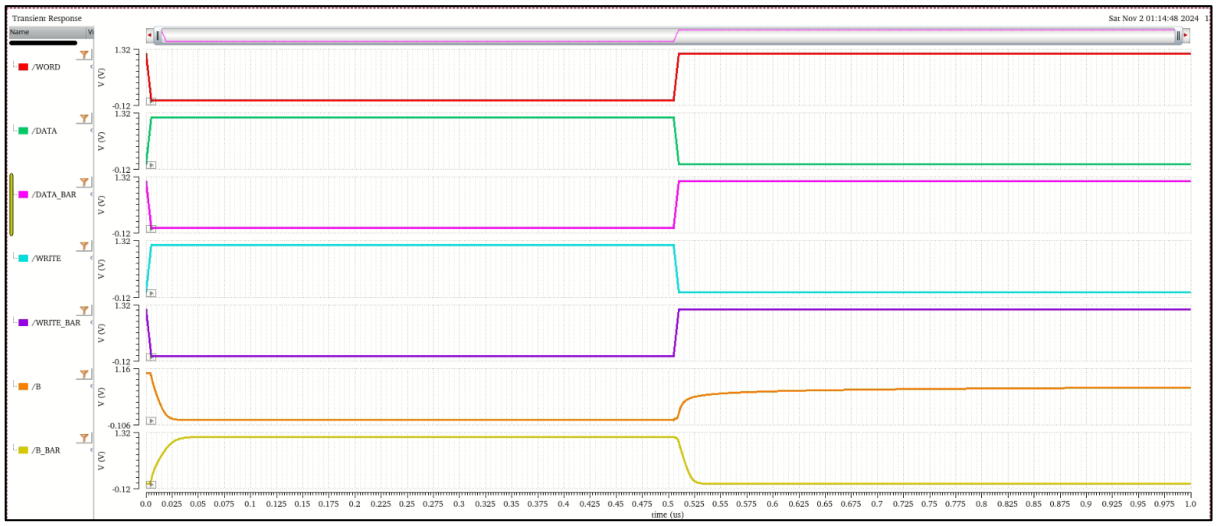


Fig. 6: Waveform of 6T SRAM for Write ‘0’ Operation

c) Write Mode for logic 1:

For writing a '1' in an SRAM cell, the pre-charge circuit sets the bit lines as follows:

- **BL** is pulled up to **VDD** (high voltage), and **BLB** is pulled down to **0 V**.
- Initially, **Q** is at **0V** and **QB** at **1.2V**.

When the **WORD Line** (set to 1) is activated, current flows through the access transistors, allowing the data to be written into the bit cell. After successfully writing a '1':

- **BL** will discharge to **0V**, and
- **BLB** will charge up to **VDD**.

This configuration successfully stores '1' in the cell.

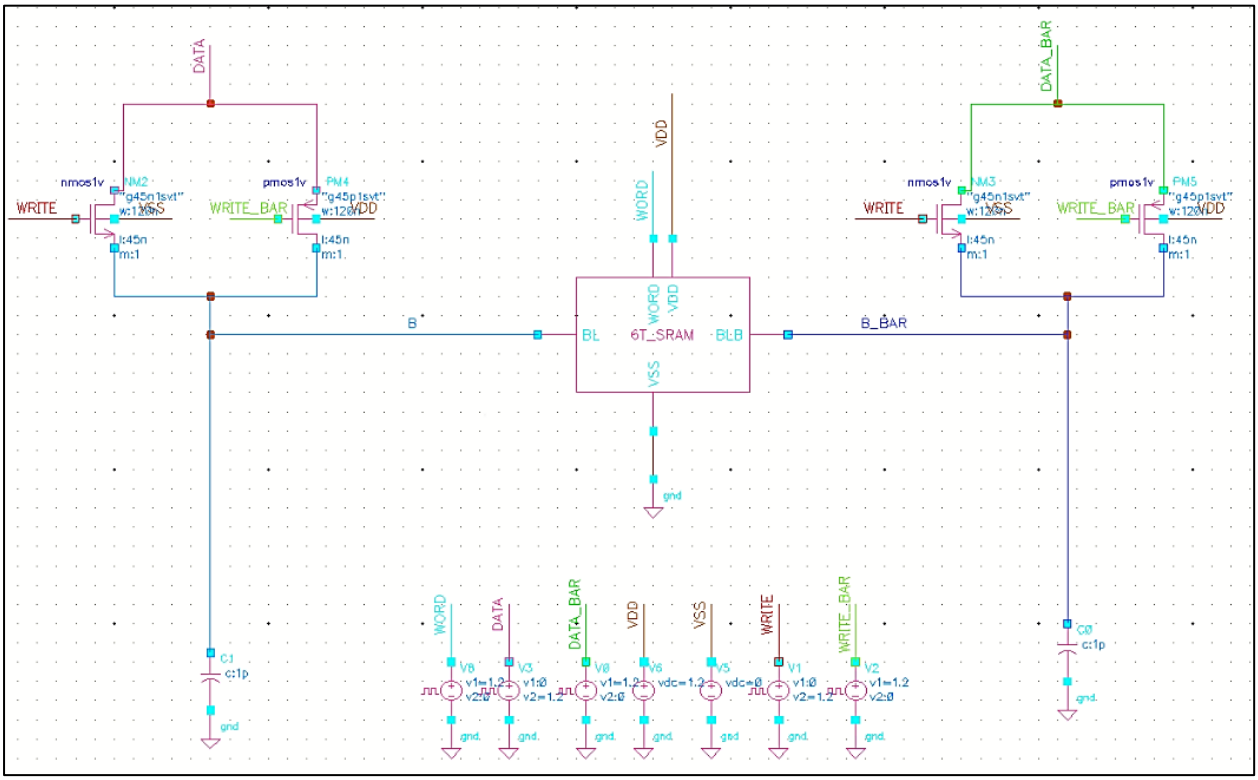


Fig. 7: Schematic of 6T SRAM for Write '1' Operation

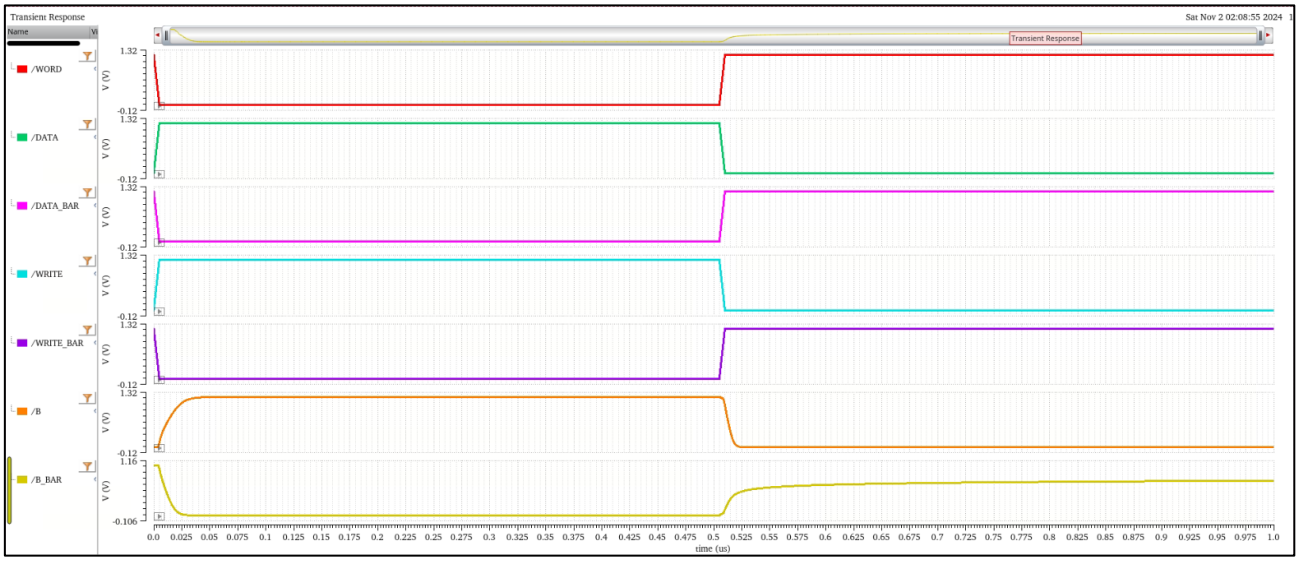


Fig. 8: Waveform of 6T SRAM for Write '1' Operation

d) Read Mode for logic 0 and logic 1:

Before each read operation in an SRAM cell:

- BL and BLB are precharged to VDD (high voltage).

When the WORD Line is activated, current flows through one of the access transistors based on the stored data:

- If QB stores '0', BLB will discharge, indicating a '0', while BL stays at VDD, confirming a stable read.
- Inversely, if Q stores '0', BL discharges, while BLB remains at VDD.

This differential discharge between BL and BLB allows for reliable data reading based on the stored values.

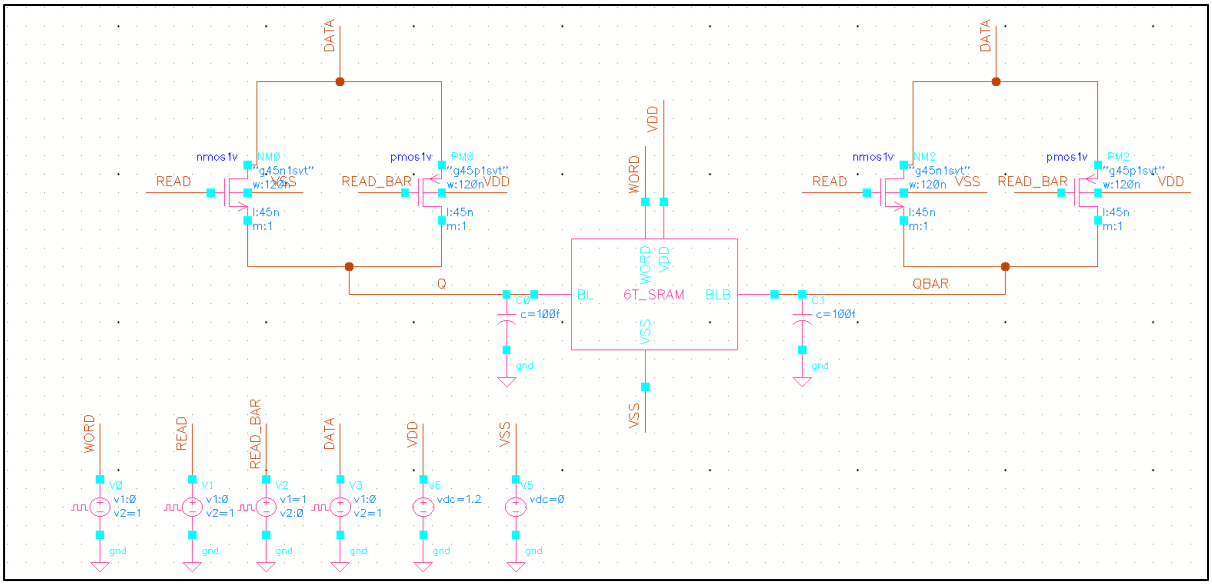


Fig. 9: Schematic of 6T SRAM for Read Operation

Read 0:

- Q is at 0V, and QB is at 1.2V.
- Since QB and BLB are at the same potential, no current flows on the BLB side when the WORD Line is high.
- On the left side (LHS), however, the access transistor and pull-down network are both active, creating a path to ground. This causes BL to discharge, indicating a read value of ‘0’.

Thus, the read operation successfully retrieves '0' from the SRAM cell by detecting the discharge on BL.

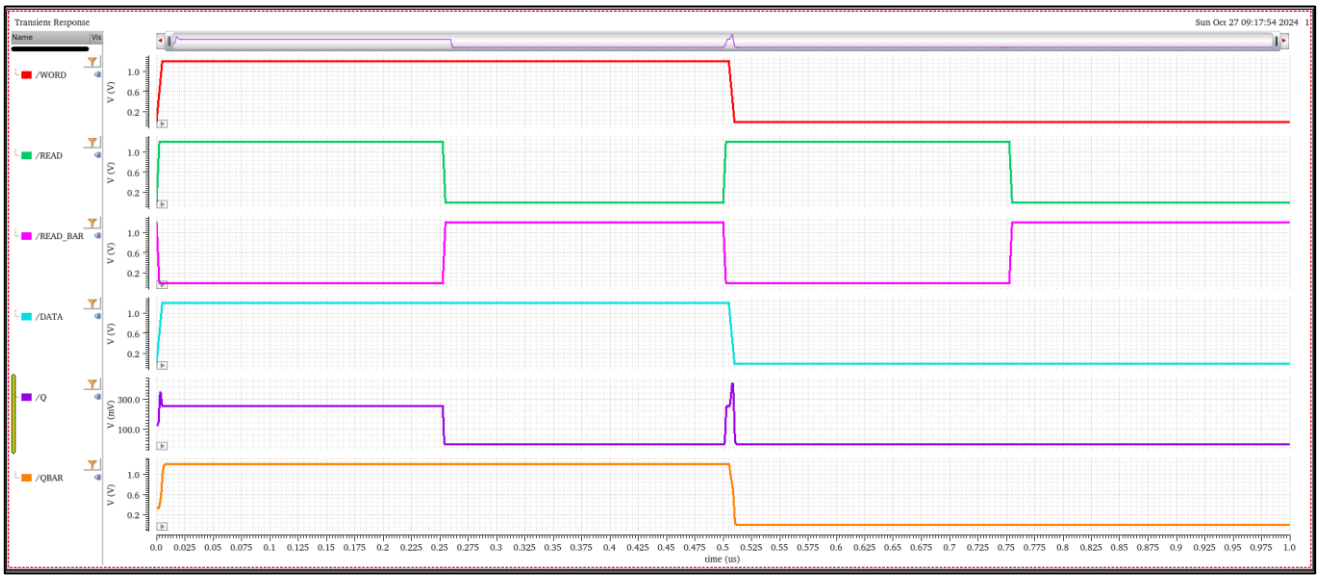


Fig. 10: Waveform of 6T SRAM for Read ‘0’ Operation

Read 1:

- Q is at 1.2V and QB is at 0V.
- Since Q and BL share the same potential, no current flows on the BL side when the WORD Line is high.
- On the right side (RHS), the access transistor and pull-down network are both active, creating a path to ground. This causes BLB to discharge, indicating a read value of ‘1’.

Therefore, the read operation retrieves '1' from the SRAM cell by detecting the discharge on BLB.

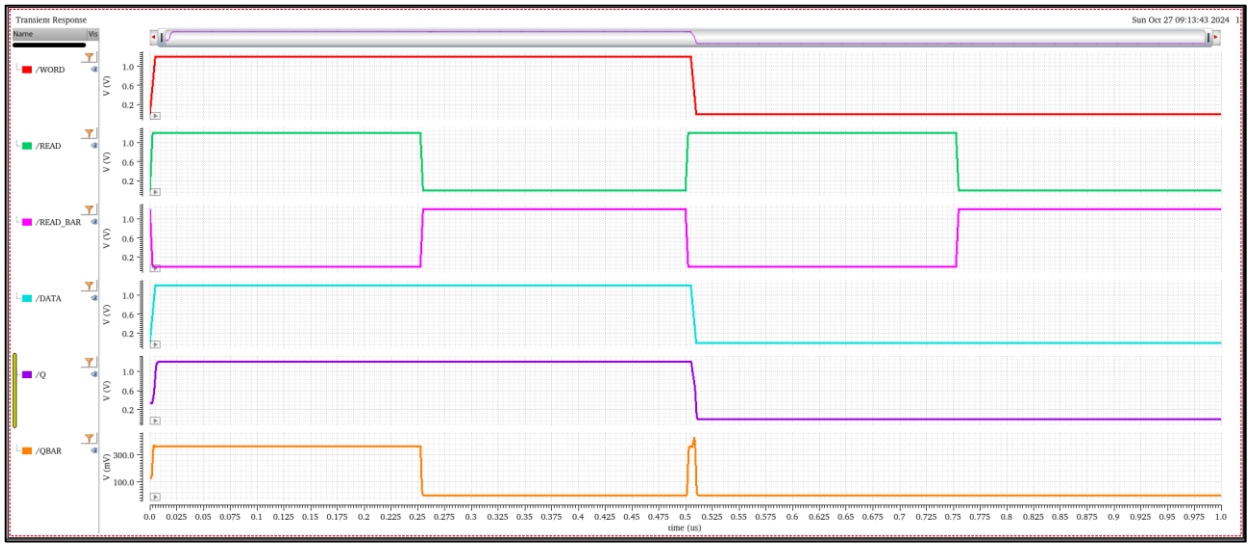


Fig. 11: Waveform of 6T SRAM for Read ‘1’ Operation

2. ***Stick Diagram, Layout and Post Layout simulation***

Stick Diagram:

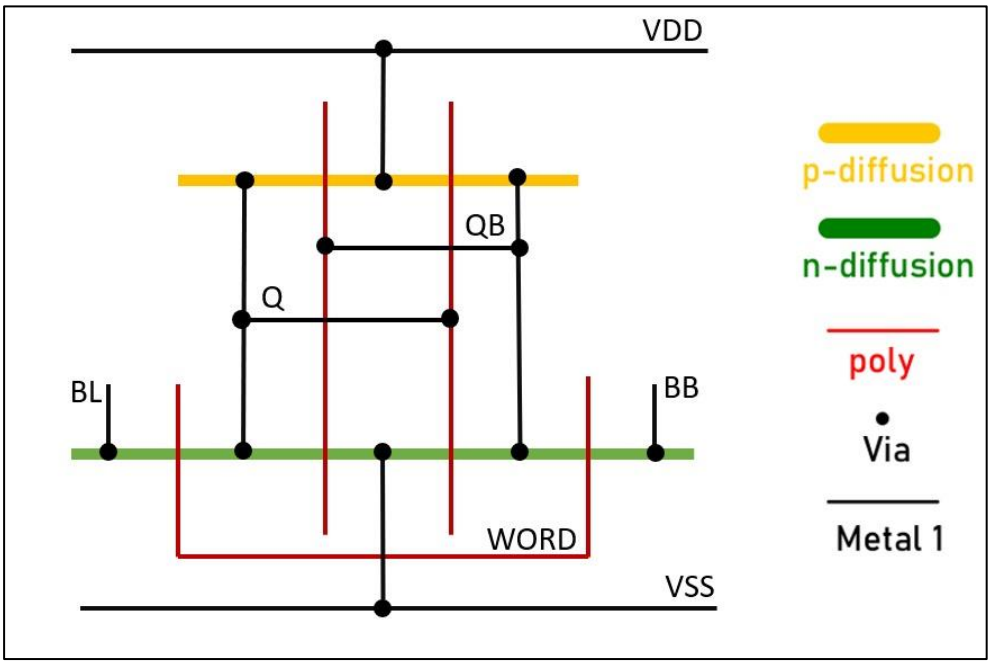


Fig. 12: Stick Diagram of 6T SRAM Cell

Layout:

The designed layout aims to reduce speed, area, and power consumption.

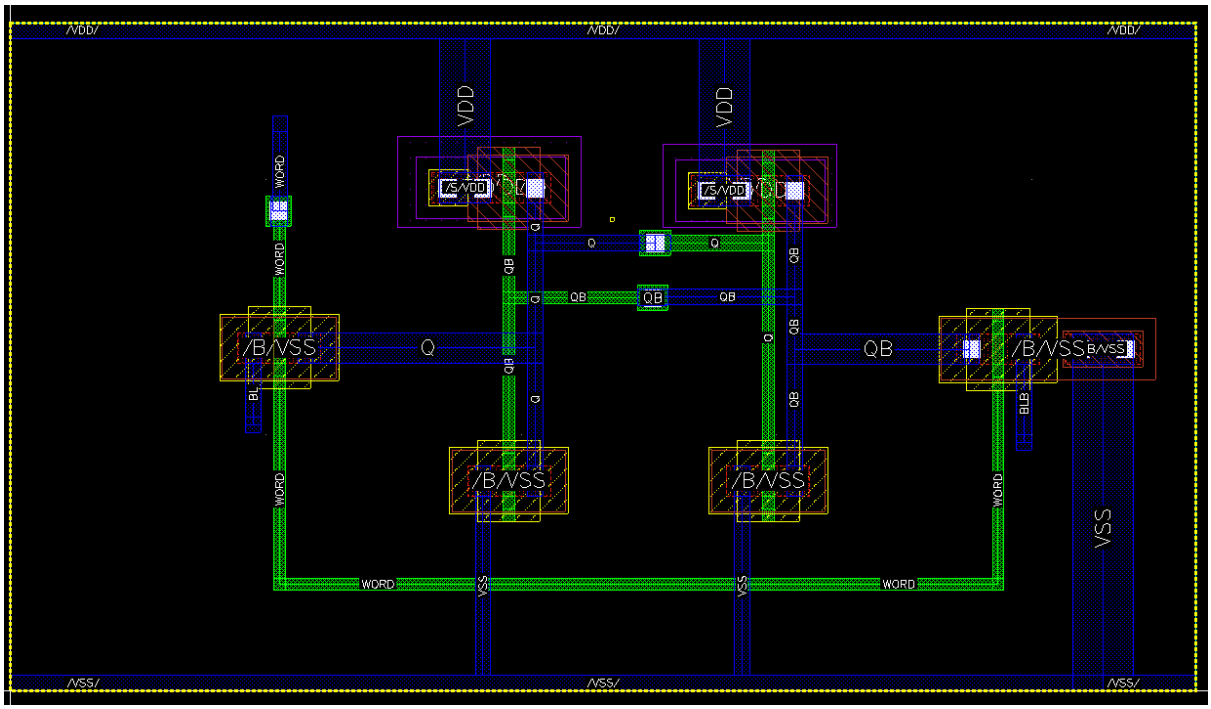
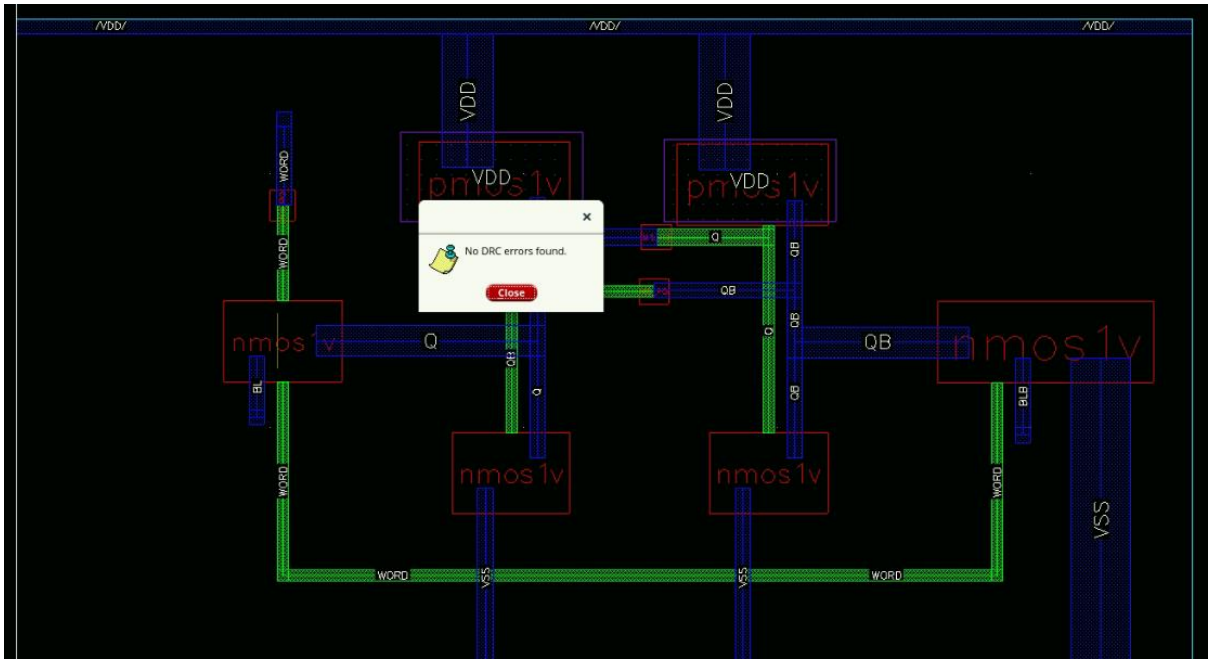


Fig. 13: Layout of 6T SRAM Cell in Cadence Virtuoso

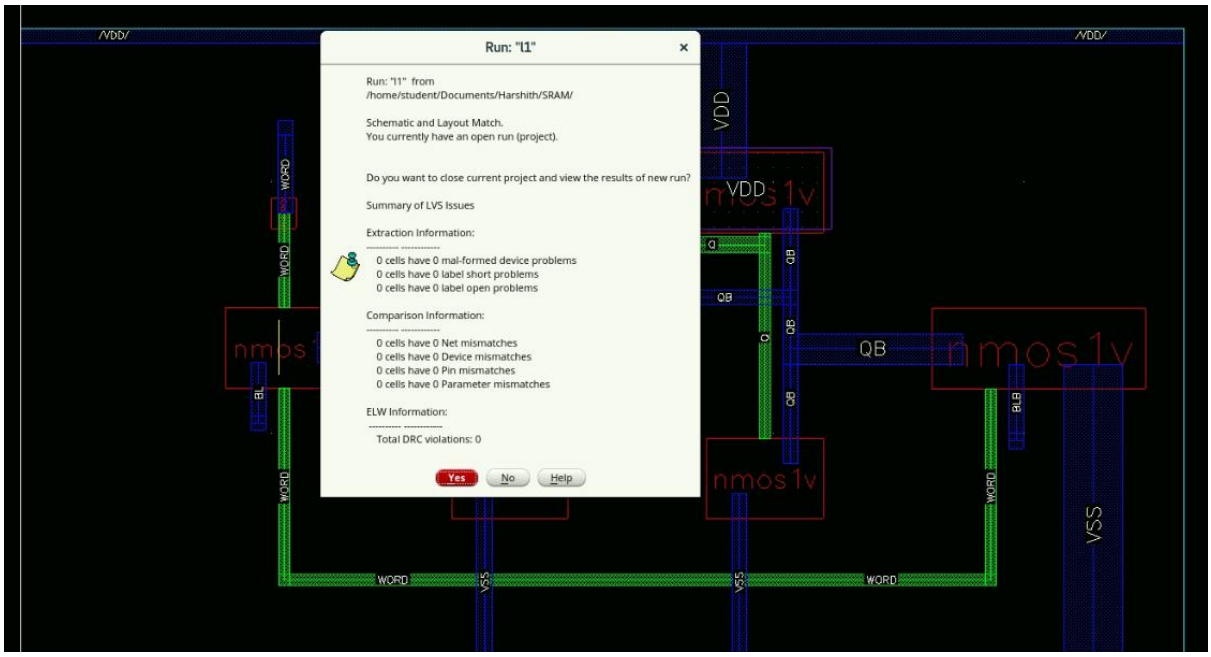
DRC (DESIGN RULE CHECK)



All design rule checks were passed, ensuring that the layout complies with the foundry's rules for manufacturability.

Fig. 14: DRC of 6T SRAM Cell in Cadence Virtuoso

LVS (LAYOUT VERSUS SCHEMATIC)



The layout was verified against the schematic to ensure that the physical implementation matches the intended design. The LVS check passed, confirming the integrity of the design.

Fig. 15: LVS of 6T SRAM Cell in Cadence Virtuoso

QUANTUS RUN AND AV EXTRACTED VIEW

Here, we can see that parasitic capacitors and resistors were included.

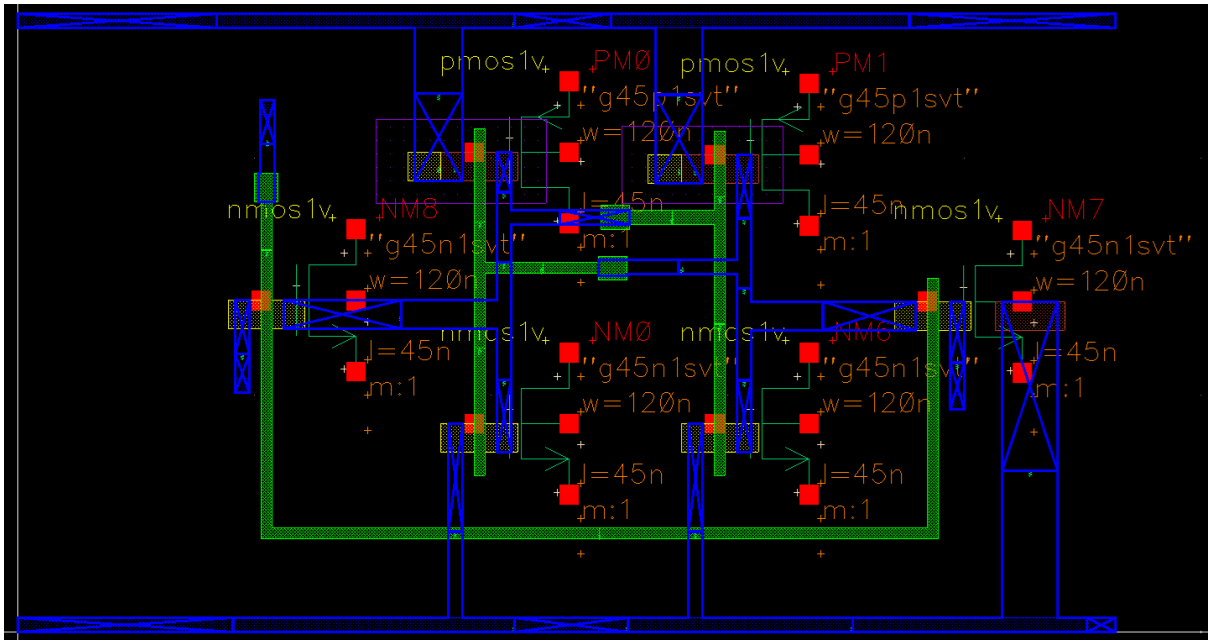


Fig. 16: av_extracted view of 6T SRAM Cell in Cadence Virtuoso

Pre-Layout and Post-Layout Simulation:

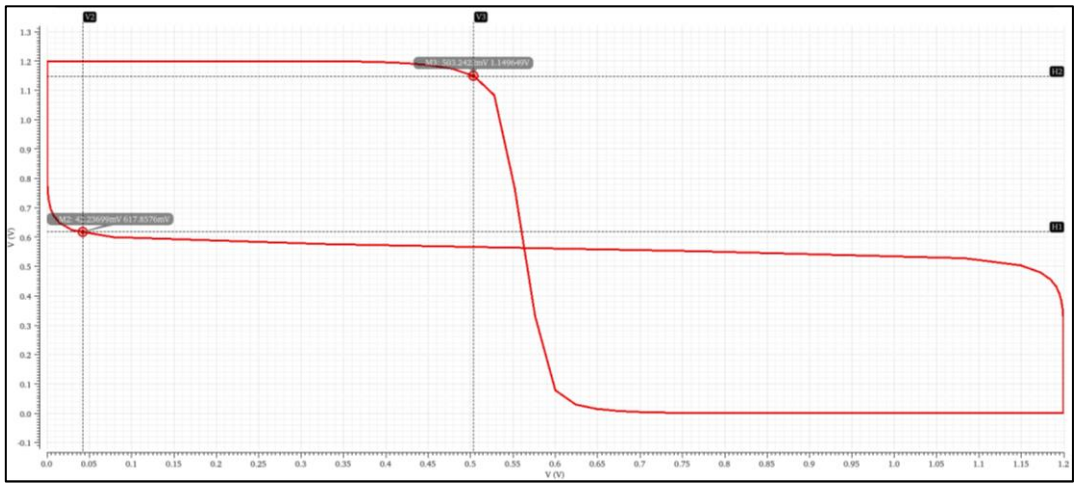


Fig. 17: Butterfly Curve (Pre-Layout Simulation)

Fig. 18: Butterfly Curve (Post-Layout Simulation)

Curve Comparison:

- **Pre-Layout Simulation:** The pre-layout butterfly curve displays sharper and more symmetric bistable behavior with consistent threshold voltages, indicating ideal switching characteristics with minimal interference from resistive and capacitive effects.
- **Post-Layout Simulation:** In the post-layout butterfly curve, deviations appear, such as shifts in switching points and reduced sharpness in the bistable regions. These changes are due to parasitic resistances and capacitances introduced by the layout, which impact the cell's stability and robustness.

Effect on Static Noise Margin (SNM):

- **Pre-Layout Simulation:** The SNM is generally higher in pre-layout simulations since parasitic effects are minimal. This enables the SRAM cell to maintain ideal symmetry and sharp switching characteristics. The larger area between the two lobes of the butterfly curve reflects greater stability and higher noise tolerance.
- **Post-Layout Simulation:** Parasitic resistance and capacitance from the layout lower the SNM by shifting threshold voltages and making the curves less sharp and asymmetric. A reduced SNM means the cell is more susceptible to noise, as less interference is needed to disrupt the stored value, which could lead to potential data corruption in noisy environments.

Causes of Deviation:

- **Parasitic Capacitance and Resistance:** Post-layout simulations account for parasitics in the layout, especially at interconnections, which can slow down the switching response, shift the threshold voltages, and reduce the noise margin.
- **Mismatch and Variability:** Process variations and device placement in the physical layout can introduce mismatches, creating asymmetry and threshold shifts in the butterfly curve.

Remedies:

- **Optimize Layout:** Minimize interconnect lengths and ensure balanced routing for critical nodes to reduce parasitic resistance and capacitance.
- **Increase Drive Strength:** Adjust transistor sizing to enhance robustness against parasitic effects.
- **Guard Bands and Dummy Structures:** Place dummy structures around the cell layout to minimize edge effects and enhance layout uniformity.

3. ***Power dissipations during Read and Write mode***

Here we are considering both Static as well as Dynamic Power Dissipation happening during Read and Write Operations.

Power Dissipation during Read Operation:

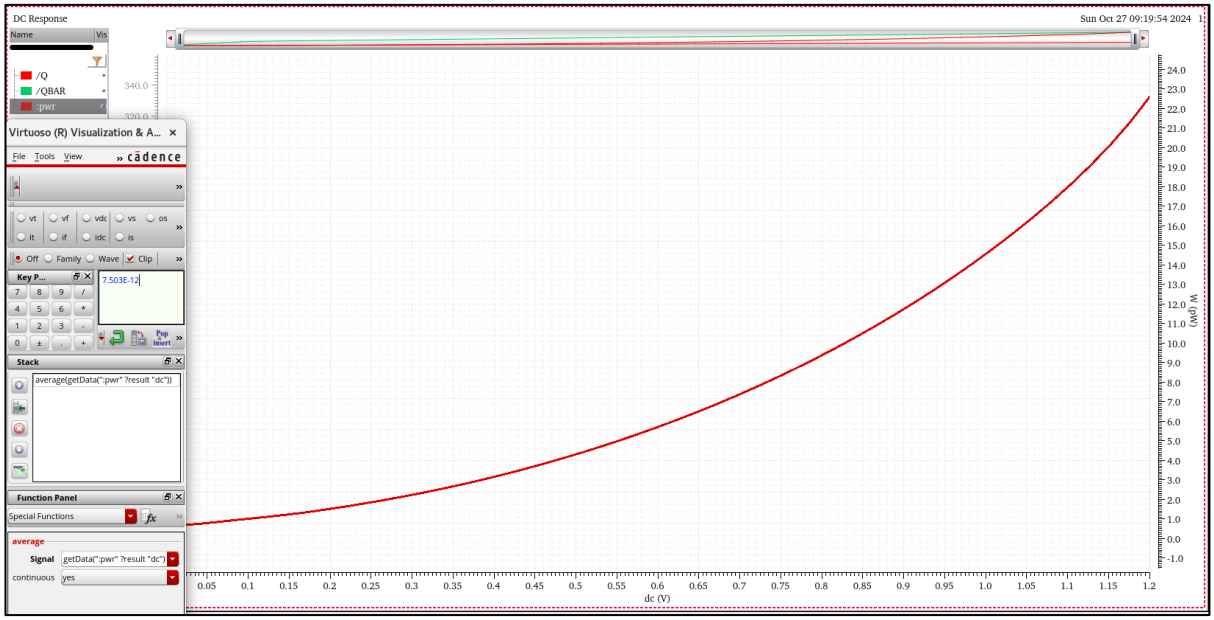


Fig. 19: Static Power Dissipation during Read 0 operation

The average static power dissipation during Read operation is 7.503pW.

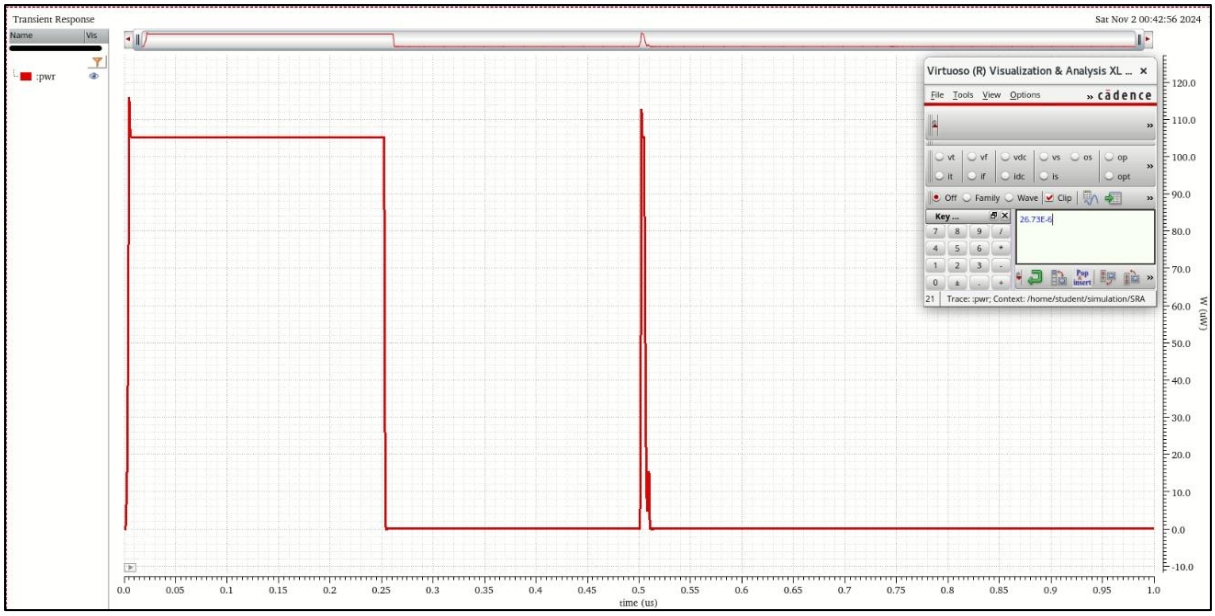


Fig. 20: Dynamic Power Dissipation during Read 0 operation

The average dynamic power dissipation during Read operation is 26.73µW

Thus, **Total Power Dissipation** = P_{Static} + $P_{Dynamic}$ = 7.503pW + 26.73µW = **26.73µW**

Power Dissipation during Write Operation:

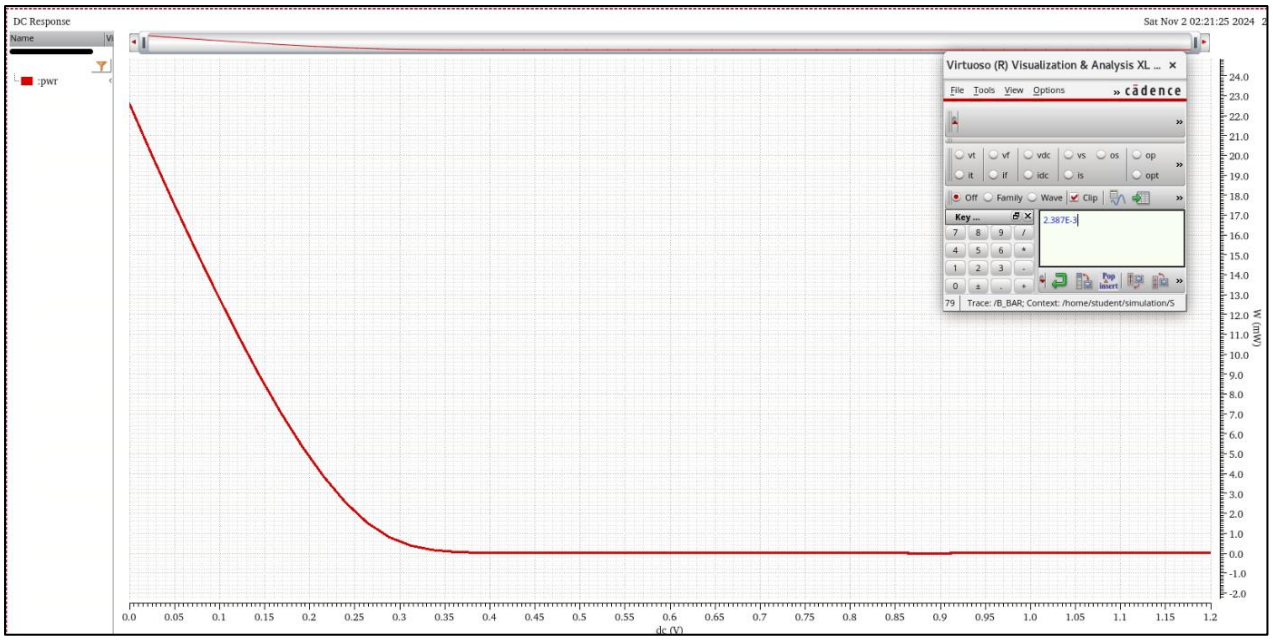


Fig. 21: Static Power Dissipation during Write 1 operation

The average static power dissipation during the Write operation is 2.387mW.

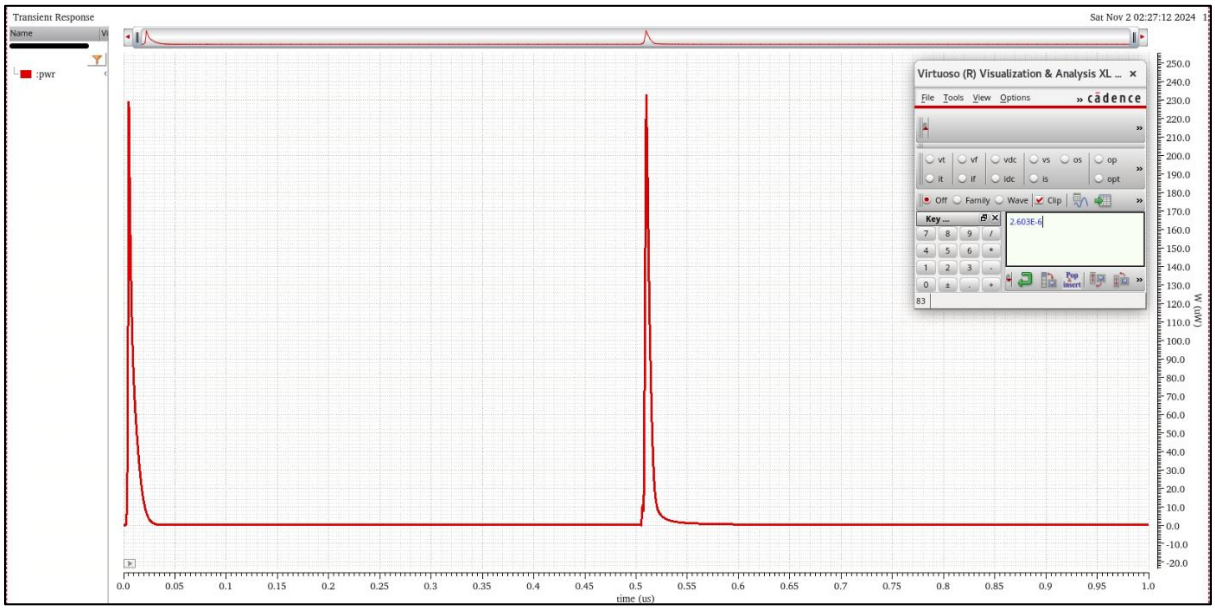


Fig. 22: Dynamic Power Dissipation during Write 1 operation

The average dynamic power dissipation during Write operation is 2.603µW

Thus, **Total Power Dissipation** = P_{Static} + $P_{Dynamic}$ = 2.387mW + 2.603µW = **2.389mW**

4. ***Static Noise Margin Calculation from Butterfly Curve:***

The Static Noise Margin (SNM) is a key metric for evaluating the stability of an SRAM cell:

- **SNM Definition:** SNM represents the minimum noise voltage required to flip the cell's state. It indicates the highest level of DC noise that the cell can tolerate while reliably holding its stored data.
- **SNM Calculation via Butterfly Curve:** The SNM is derived from the butterfly curve, which shows the voltage transfer characteristics (VTCs) of the two cross-coupled inverters within the SRAM cell.
- **Butterfly Curve:** This curve is obtained by sweeping the input voltage at one storage node and plotting the corresponding output voltage at the other node. The resulting shape resembles butterfly wings, with the two lobes representing the bistable states.
- **SNM Calculation Method:** The SNM is measured by determining the side length of the largest possible square that can fit between the two lobes of the butterfly curve. This square represents the maximum noise tolerance before the cell's stability is compromised.

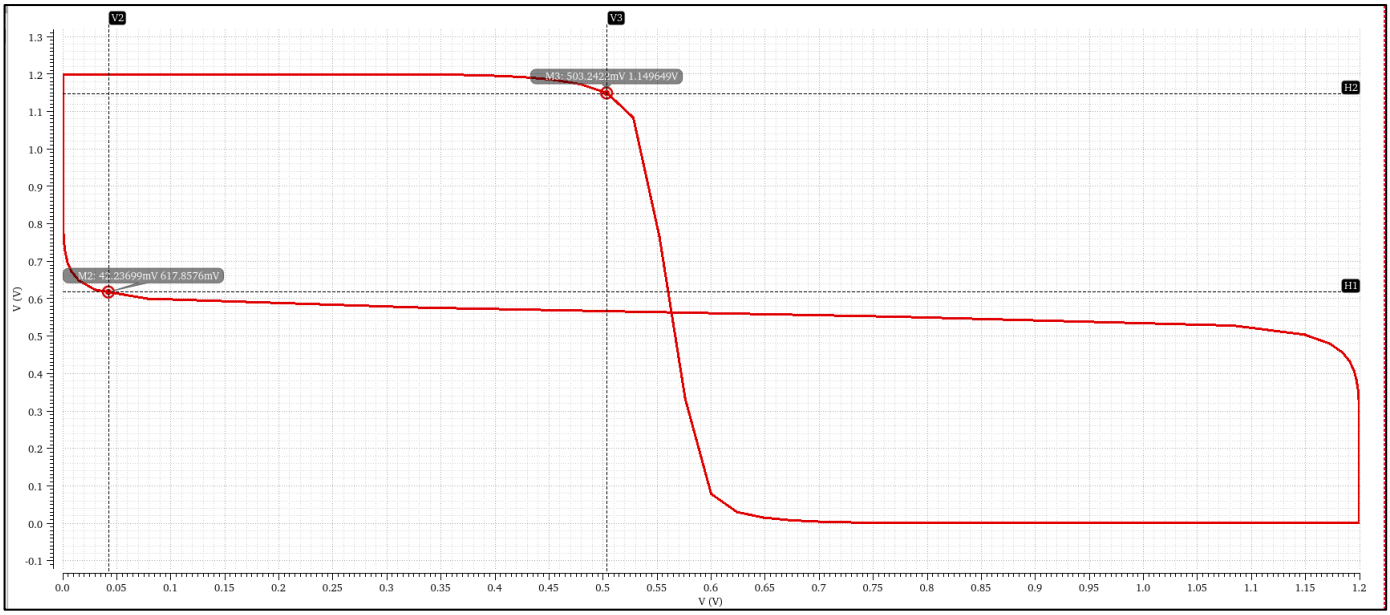


Fig. 23: Butterfly Curve

The calculated SNM for the designed SRAM is,

SNM = 503.2422 mV - 42.23699mV = **461.00521mV** (Indicates strong noise immunity.)

5. ***Process corner analysis and Effects of transistor sizing in the cell***

The SRAM cell was tested across various process corners to observe its performance under different transistor speed conditions:

- **Slow-Slow (SS):** Both NMOS and PMOS transistors operate slowly, resulting in a higher delay in the circuit.
- Fast-Fast (FF): Both NMOS and PMOS transistors are fast, which allows the cell to operate quickly. However, this corner also results in higher power consumption.
- Slow-Fast (SF): In this configuration, NMOS transistors are slow, while PMOS transistors are fast, creating an imbalance in speed that can affect timing and stability.
- Fast-Slow (FS): Here, NMOS transistors are fast, while PMOS transistors are slow. This corner also introduces an imbalance, impacting the cell's performance and stability.

Testing across these corners provides insights into the cell's robustness and ensures reliable operation across different manufacturing variations.

The analysis is done in ADE XL in Cadence Virtuoso.

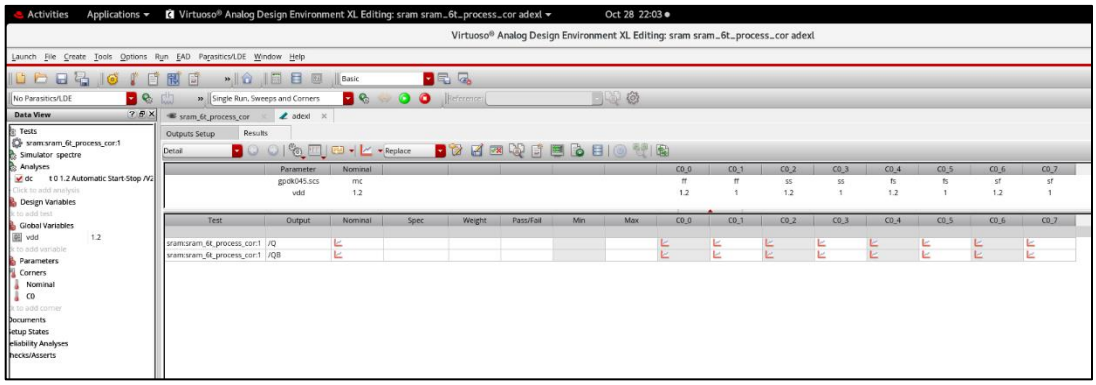


Fig. 24: Processor Corner Analysis in ADE XL Window

Here the analysis was done for two different transistor sizing.

Here, the global variable is selected as VDD, and the corner analysis is performed for two voltages, 1.2V and 1V.

Case 1:

W_{PU}= 120nm, W_{AC}= 180nm, W_{PD}= 240nm and L =45nm

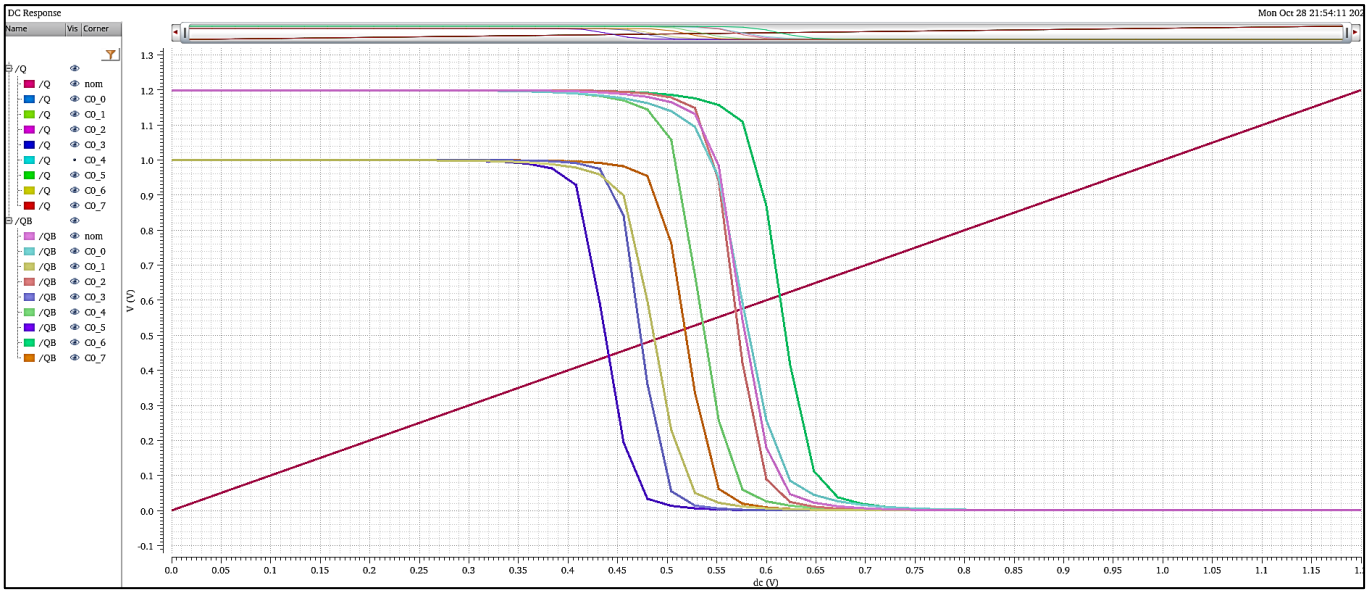


Fig. 25: Process Corner Analysis graph

Case 2:

W_{PU}=120nm, W_{AC}=240nm, W_{PD}= 360nm and L =45nm

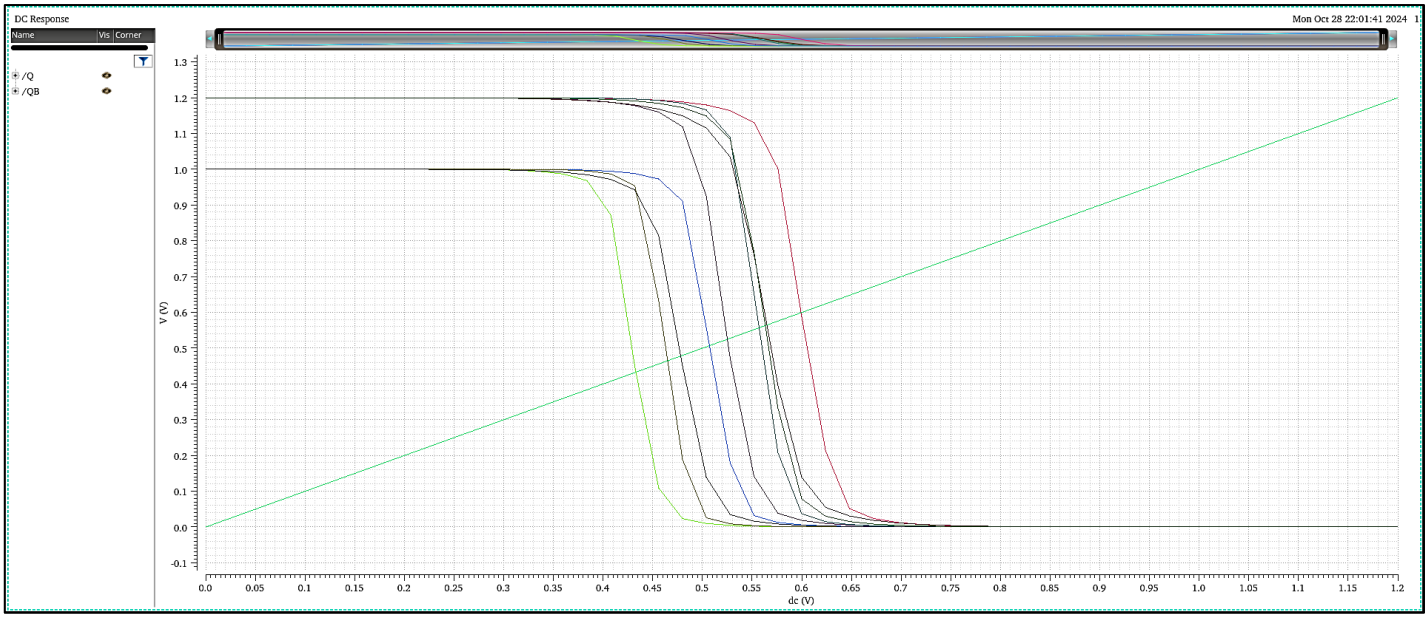


Fig. 26: Process Corner Analysis graph

Impact of Transistor Sizing in SRAM Cells

Transistor sizing is a critical factor in achieving a balanced performance, stability, and power efficiency in SRAM cells. Here's how sizing affects each type of transistor:

- **Pull-Up Transistor Size:** Smaller PMOS transistors in the pull-up network can reduce power consumption but may weaken the cell's ability to hold a '1'. In the Slow-Slow (SS) corner, a weaker pull-up can help maintain a stable Static Noise Margin (SNM) but may slow down cell operations.

- **Pull-Down Transistor Size:** Larger NMOS transistors in the pull-down path strengthen the cell's ability to retain a '0' during a read operation. However, in the Fast-Fast (FF) corner, larger pull-down transistors may lead to excessive leakage, which can reduce the SNM, impacting cell stability.

- **Access Transistor Size:** The size of the pass-gate (access) transistors affects read and write margins. A larger access transistor makes it easier to read and write data but can reduce SNM due to increased coupling between the bit lines and storage nodes. This effect is more pronounced in Fast-Slow (FS) and Slow-Fast (SF) corners, where asymmetry in transistor speeds can further impact stability.

Effects of Transistor Sizing on Read/Write Stability

- **Read Stability:** The pull-down NMOS transistor needs to be strong enough to keep the internal node low during a read operation without inverting the stored value. While increasing the pull-down NMOS size improves read stability, it can come at the cost of increased power consumption and area.

- **Write Stability:** To reliably change the internal node to the desired value during a write operation, the access transistor must be strong enough to overpower the opposing inverter. Increasing the access transistor size improves write performance but may decrease read stability due to increased coupling effects.

- **Cell Ratio and Pull-Up Ratio:** Adjusting the cell ratio (pull-down to access transistor size ratio) and pull-up ratio (pull-up to access transistor size ratio) helps balance read and write margins across different process corners. A larger cell ratio enhances read stability, while a larger pull-up ratio supports write stability, providing a more flexible design that maintains robustness across manufacturing variations.

6. *GDS II file*

The GDS II file, which uses industry-standard mask generating formats, includes the design's geometry and layer information.

Fig. 27: GDS II file of SRAM

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Reference:

1. Jan M, Rabaey, et al, Digital Integrated Circuits: A Design Perspective, Prentice Hall, 2003.
2. Neil Weste and K. Eshragian, Principles of CMOS VLSI Design: A System Perspective, Pearson Education, 2000.

Team Member	Contribution
Abhiram K M	**Design Specifications and Application Relevance:** Defined the roles of pull-up, pull-down, and access transistors in SRAM, emphasizing stability and power efficiency.
	Simulation Modes and Transistor Sizing: Calculated transistor sizing (cell and pull-up ratios) for optimal performance and simulated standby, read, and write modes.
	Stick Diagram & Layout Creation: Developed the stick diagram and transferred it to Cadence Virtuoso for layout, ensuring compliance with layout rules and zero DRC violations.
	Static Noise Margin (SNM) Analysis: Analyzed SNM through pre- and post-layout butterfly curves to evaluate noise immunity and stability.
	Simulations and Parasitic Analysis: Conducted pre- and post-layout simulations, observing ideal and real-world performance.
	Power Dissipation Calculations: Calculated static and dynamic power dissipation during read and write operations.
	Process Corner Analysis: Conducted process corner analysis for conditions like slow-slow (SS) and fast-fast (FF).
	Documentation and Reporting: Compiled all data into a comprehensive final report, integrating specifications, simulation results, and SNM analysis.
Harshith Gowda B V	**Design Specifications and Application Relevance:** Provided insights into SRAM's advantages for low-power applications compared to DRAM and addressed layout constraints for area efficiency.
	Simulation Modes and Transistor Sizing: Simulated standby, read, and write modes, documenting the impact of sizing on stability in each mode.
	Stick Diagram & Layout Creation: Verified layout integrity by performing Layout Versus Schematic (LVS) checks to ensure accuracy.
	Static Noise Margin (SNM) Analysis: Recommended layout adjustments to minimize parasitic effects and maintain strong SNM.
	Power Dissipation Calculations: Compared power metrics across operations to recommend efficiency improvements.
	Process Corner Analysis: Assessed how different corners impact stability and suggested sizing adjustments to maintain performance across process variations.
	Documentation and Reporting: Finalized and formatted the GDS II file for submission, ensuring the report met project requirements.

SRAM

ORIGINALITY REPORT

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SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS

PRIMARY SOURCES

1	Naeem Maroof, Muhammad Sohail, Hyunchul Shin. "Charge-sharing read port with bitline pre-charging and sensing scheme for low-power SRAMs", International Journal of Circuit Theory and Applications, 2017 Publication	2%
2	Hooman Farkhani, Ali Peiravi, Farshad Moradi. "A new write assist technique for SRAM design in 65nm CMOS technology", Integration, the VLSI Journal, 2015 Publication	1%
3	Jitendra Kumar Mishra, Harshit Srivastava, Prasanna Kumar Misra, Manish Goswami. "A 40nm Low Power High Stable SRAM Cell Using Separate Read Port and Sleep Transistor Methodology", 2018 IEEE International Symposium on Smart Electronic Systems (iSES) (Formerly iNiS), 2018 Publication	1%
4	Vernor, Dusten. "SNM analysis of 11NM shorted-gate and low-power 6T FinFET SRAM	1%

topologies.", Proquest, 2015.
Publication

5	Neha Gupta, Ambika Prasad Shah, Rana Sagar Kumar, Tanisha Gupta, Sajid Khan, Santosh Kumar Vishvakarma. "On-Chip Adaptive VDD Scaled Architecture of Reliable SRAM Cell with Improved Soft Error Tolerance", IEEE Transactions on Device and Materials Reliability, 2020 Publication	1 %
6	Vojin G. Oklobdzija. "Digital Design and Fabrication", CRC Press, 2017 Publication	1 %
7	M. Elangovan, G. Saravanan, S. Jayanthi, P. Raja, Kulbhushan Sharma, S. Nireshkumar. "High stability and high speed 11T cntfet sram cell for mimo applications", Journal of Circuits, Systems and Computers, 2023 Publication	1 %
8	Brajesh Kumar Kaushik, Brijesh Kumar, Sanjay Prajapati, Poornima Mittal. "Organic Thin-Film Transistor Applications - Materials to Circuits", CRC Press, 2019 Publication	<1 %
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11	Sd Nageena Parveen, V Charishma, P Summit, A Sandeep, R Sai Rahul. "Design and Performance Analysis of 6T SRAM Cell on Different CMOS Technologies", 2023 World Conference on Communication & Computing (WCONF), 2023 Publication	<1 %
12	Rahebeh Niaraki Asli, Shiva Taghipour. "Reliable and high performance asymmetric FinFET SRAM cell using back-gate control", Microelectronics Reliability, 2020 Publication	<1 %
13	Rajendran, Aravind, Yuriy Shiyanovskii, Frank Wolff, and Chris Papachristou. "Noise margin, critical charge and power-delay tradeoffs for SRAM design", 2011 IEEE 17th International On-Line Testing Symposium, 2011. Publication	<1 %
14	"VLSI Design and Test", Springer Science and Business Media LLC, 2019 Publication	<1 %

15	Zhiting Lin, Panpan Chen, Le Ye, Xu Yan, Lanzhi Dong, Shuguang Zhang, Zhou Yang, Chunyu Peng, Xiulong Wu, Junning Chen. "Challenges and Solutions of the TFET Circuit Design", IEEE Transactions on Circuits and Systems I: Regular Papers, 2020 Publication	<1 %
16	Alorda, Bartomeu, Gabriel Torrens, Sebastia Bota, and Jaume Segura. "Adaptive static and dynamic noise margin improvement in minimum-sized 6T-SRAM cells", Microelectronics Reliability, 2014. Publication	<1 %
17	C.M.R. Prabhu, Ajay Kumar Singh. "A proposed SRAM cell for low power consumption during write operation", Microelectronics International, 2009 Publication	<1 %
18	Harry Veendrick. "Chapter 4 CMOS Circuit, Layout and Library Design", Springer Science and Business Media LLC, 2025 Publication	<1 %
19	Manoj Kumar R, P.V. Sridevi. "Design of an enhanced write stability, high-performance, low power 11T SRAM cell", International Journal of Electronics, 2021 Publication	<1 %

20	Upadhyay, P., R. Kar, D. Mandal, and S.P. Ghoshal. "A design of low swing and multi threshold voltage based low power 12T SRAM cell", Computers & Electrical Engineering, 2015. Publication	<1 %
21	E. McCluskey, S. Bozorgui-Nesbat. "Design for autonomous test", IEEE Transactions on Circuits and Systems, 1981 Publication	<1 %
22	M. Madhusudhan Reddy, M. Sailaja, K. Babulu. "Energy optimization of 6T SRAM cell using low-voltage and high-performance inverter structures", International Journal of Electrical and Computer Engineering (IJECE), 2019 Publication	<1 %
23	Himanshu Banga, Dheeraj Agarwal. "Single bit-line 10T SRAM cell for low power and high SNM", 2017 International Conference on Recent Innovations in Signal processing and Embedded Systems (RISE), 2017 Publication	<1 %

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