MANIPAL INSTITUTE OF TECHNOLOGY
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Manipal Institute of Technology

Department of Electronics and Communication Engineering

Course: ECE 5112 DIGITAL VLSI DESIGN

Assignment 2(Part B)

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Submitted to,

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i. Do the literature survey of some schemes of parallel prefix adders (PPA) existing in literature, such as,

a. Brent-Kung

b. Kogge-Stone

c. Han-Carlson

and find their limitations in terms of power, performance, area, power delay product (PDP), and energy-delay product (EDP) during data path design for the next-generation technology.

ii. Further, design the 4-bit adder using the following architecture for your data path design using sparse tree architecture (STA) with single rail and semi-dynamic circuit using reference.

iii. Calculate its average power and performance by circuit simulation using the following technologies available in the laboratory (45 nm, 90nm, 180 nm technologies) and compare them with the existing literature.

iv. Draw the stick diagram and layout of the STA-based optimized cell. Perform the post-layout simulation and check whether both the results are relatively equal or not. If so, highlight the cause and possible remedies.

v. Perform the process corner analysis and discuss the effects of transistor sizing in the cell qualitatively.

vi. Finally, Generate a GDS II file for your design.

After all the analysis, can you develop the design specification for your proposed adder using STA architecture?

…….

i. Parallel Prefix Adders (PPAs) play a crucial role in high-speed digital systems and are typically assessed on metrics such as power, performance, area, power-delay product (PDP), and energy-delay product (EDP). This survey examines prominent PPA designs frequently employed in high-performance applications, with a focus on the Brent-Kung, Kogge-Stone, and Han-Carlson adders, highlighting their respective limitations.

1. Brent-Kung Adder

Overview: Brent-Kung adders are well-regarded for their compact design, offering an efficient balance of speed and resource use. Due to their tree-like structure, they're often chosen for systems with limited hardware resources, where area efficiency is prioritized.

Limitations:

Power: Generally low power consumption, but longer delays in signal propagation can increase energy use in high-bit scenarios.

Performance: Provides moderate speed, though the critical path length makes it slower than faster designs like Kogge-Stone, impacting its suitability for high-frequency operations.

Area: Known for area efficiency, making it a good fit for resource-constrained systems.

Power-Delay Product (PDP): Offers moderate power-delay product, but higher delays reduce its efficiency in applications demanding quick responses.

Energy-Delay Product (EDP): The slower speed impacts its energy-delay product, making it less ideal for performance-intensive and energy-efficient applications.

2. Kogge-Stone Adder

Overview: The Kogge-Stone adder is structured for high-speed performance with minimal logic depth, making it a go-to option in applications where speed is a top priority. However, this design requires a large number of interconnections, increasing its power and area requirements.

Limitations:

Power: High power consumption due to extensive wiring and buffer requirements, especially in high-bit configurations.

Performance: One of the fastest PPAs, optimized for high-speed applications, although the interconnection complexity adds capacitance that may impact efficiency in finer technology nodes.

Area: Requires significant area, which can be a drawback in space-constrained designs.

Power-Delay Product (PDP): High speed comes at the cost of a higher power-delay product, limiting its suitability for low-power applications.

Energy-Delay Product (EDP): High energy consumption per operation results in a less favorable energy-delay product, especially in energy-sensitive environments.

3. Han-Carlson Adder

Overview: The Han-Carlson adder combines features of both Brent-Kung and Kogge-Stone designs, aiming to provide a compromise between speed and resource efficiency. Its structure offers a balanced option that is useful in applications needing a moderate balance between area and performance.

Limitations:

- **Power:** Has a moderate power requirement, generally more than Brent-Kung but less than Kogge-Stone, providing a good middle ground.
- **Performance:** Offers a balanced speed, providing adequate performance without the delays of Brent-Kung or the power demands of Kogge-Stone.

- **Area:** Occupies more area than Brent-Kung but less than Kogge-Stone, making it a good option for systems needing a balance of area and speed.
- **Power-Delay Product (PDP):** Presents a moderate power-delay product, which makes it suitable for designs requiring both decent speed and energy efficiency.
- **Energy-Delay Product (EDP):** With a balanced energy-delay product, the Han-Carlson adder is effective for applications needing moderate performance and energy efficiency without extreme power costs.

Summary of Limitations for Each Adder

- **Brent-Kung**: Limited by slower carry propagation and moderate delay, which affects its suitability for high-frequency applications.
- **Kogge-Stone**: High power and area costs make it challenging to implement in power-constrained or compact systems.
- **Han-Carlson**: While balanced, it does not excel in any single metric, meaning it may not be ideal for applications that demand either extreme power efficiency or ultra-high speed.

Attribute	Brent-Kung Adder	Kogge-Stone Adder	Han-Carlson Adder
Power	Low power consumption due to fewer nodes and minimal wiring complexity.	High power consumption from dense wiring and high fan-out.	Moderate power consumption; fewer interconnections than Kogge-Stone.
Performance	Moderate; slower carry propagation due to increased logic depth.	High performance; minimal carry propagation delay, ideal for high-speed applications.	Moderate-to-high performance; faster than Brent-Kung but slower than Kogge-Stone.
Area	Small area footprint	Large area	Moderate area
Power-Delay Product (PDP)	Low PDP	Moderate PDP	Balanced PDP
Energy-Delay Product (EDP)	High EDP.	Competitive EDP	Favourable EDP;

ii. The circuit is designed for 45nm technology node in Cadence Virtuoso.

CMOS inverter

A simple inverter circuit, or NOT gate, reverses the input signal:

- PMOS Transistor: Connected to the power supply (VDD). It turns on when the input is low, pulling the output high.
- NMOS Transistor: Connected to ground(VSS). It turns on when the input is high, pulling the output low.

When the input is high, the NMOS conducts, grounding the output to produce a low output. When the input is low, the PMOS conducts, pulling the output up to VDD , producing a high output. This makes the output the logical opposite of the input.

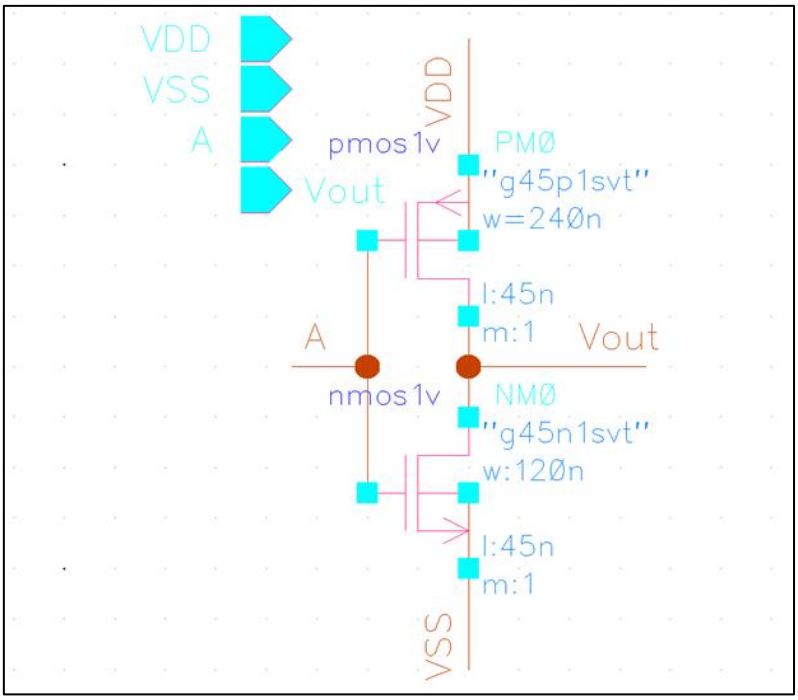

Fig. 1 : Schematic of CMOS inverter

Generate block

The Generate block in the PPA is a dynamic AND gate that outputs G=A·B.

- Pre-charge Phase: When the clock is low, a PMOS transistor charges the output node to high.
- Evaluation Phase: When the clock goes high, if both A and B are high, the NMOS network discharges the output to low. If either A or B is low, the output remains high.

This dynamic design improves speed and reduces static power, essential for efficient high-speed addition.

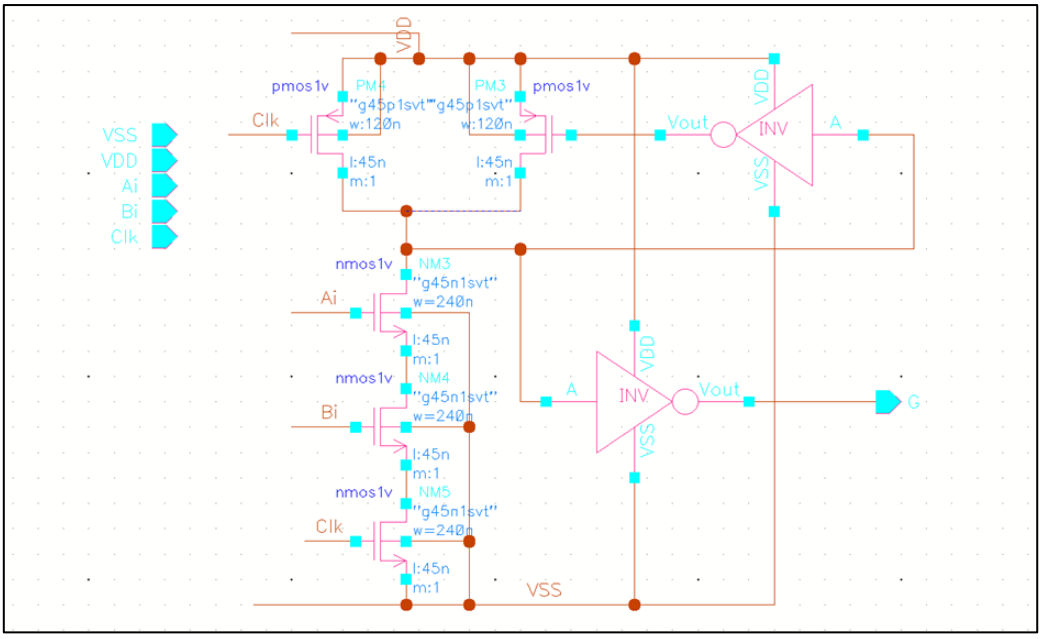

Fig. 2 : Schematic of Generate block (A.B)

Propagate block

The Propagate block in the PPA is a dynamic XOR gate that outputs P=A⊕B.

- Precharge Phase: When the clock is low, a PMOS transistor charges the output node to high.
- Evaluation Phase: When the clock goes high, the NMOS network discharges the output to low only if A and B are in opposite states (one high, one low), creating the XOR effect. If A and B are both high or both low, the output remains high.

This dynamic XOR design provides fast switching and lower power consumption, ideal for rapid signal propagation in the adder.

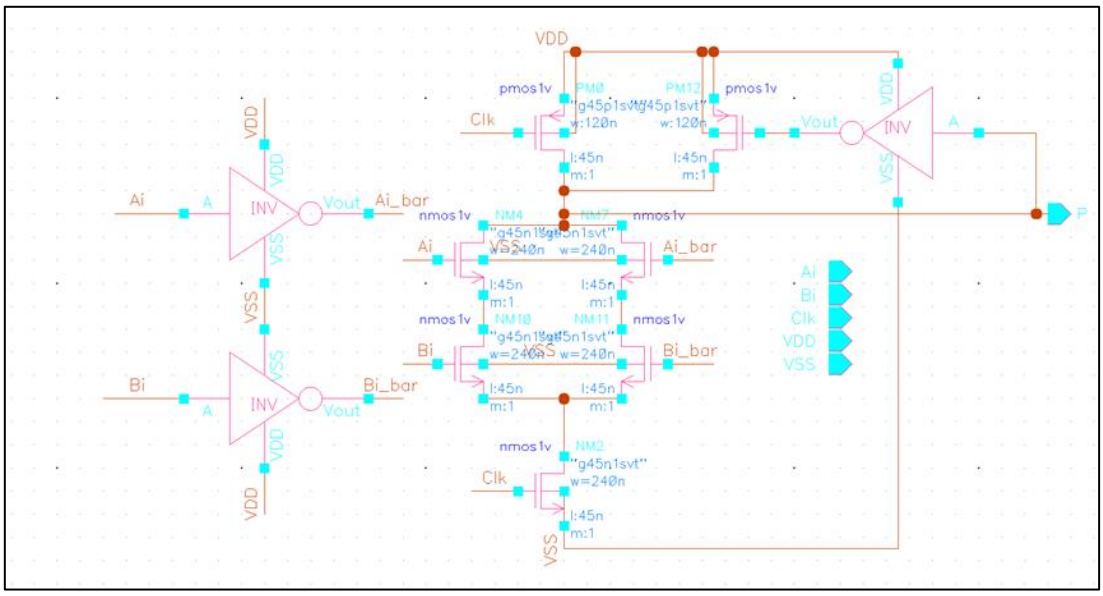

Fig. 3 : Schematic of Propagate block (A XOR B)

Dynamic MUX

The Dynamic MUX selects between two inputs, Sum_1 and Sum_0, based on a control signal Carry.

- Precharge Phase: When the clock is low, a PMOS transistor precharges the output node to high.
- Evaluation Phase: When the clock goes high:
  - If Carry is high, the NMOS network connects Sum_1 to the output.
  - If Carry is low, the NMOS network connects Sum_0 to the output.

Only the selected input discharges the output if it's low, implementing a dynamic multiplexing effect with reduced static power and faster operation.

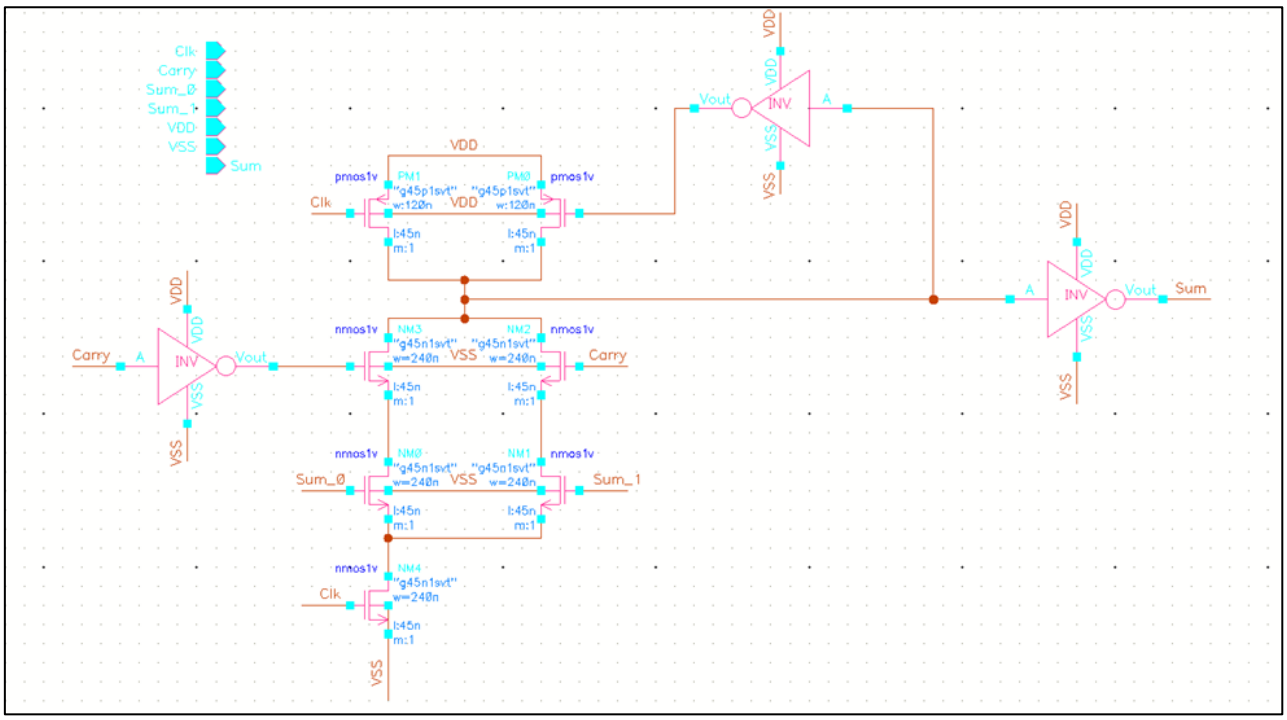

Fig. 4 : Schematic of Dynamic MUX

Schematic of Parallel Prefix Adder implemented using Carry Look Ahead Logic

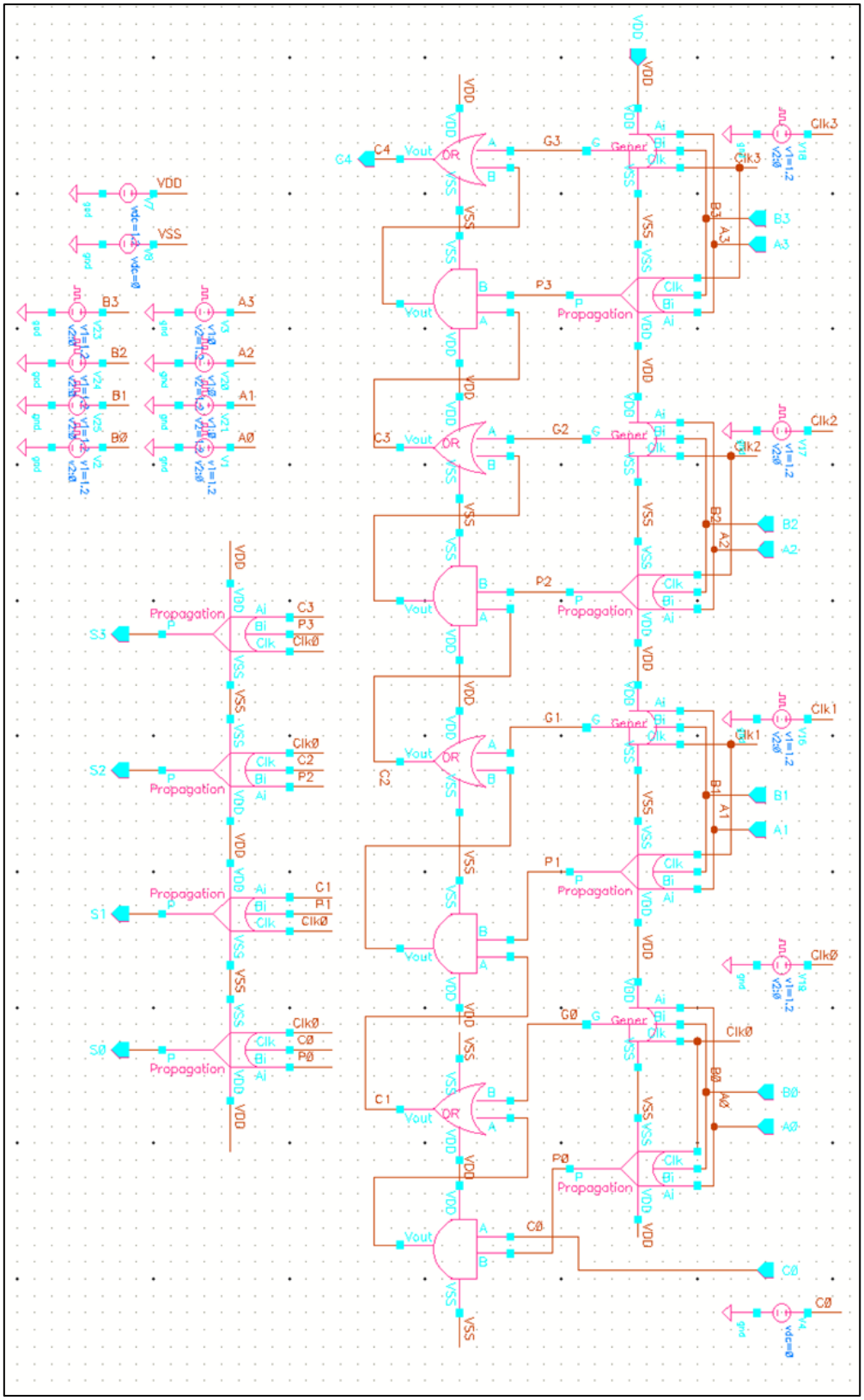

Fig. 5 : Schematic of Parallel Prefix Adder implemented using Carry Look Ahead Logic

A **Parallel Prefix Adder** (PPA) using **Carry Look-Ahead (CLA) Logic** quickly computes carries for each bit position, making addition faster by avoiding the linear carry propagation delay of ripple adders. Here's a breakdown of its structure:

1. Generate and Propagate Signals

- Each bit pair (Ai,Bi) produces **Generate** ($G_i = A_i \cdot B_i$) and **Propagate** ($P_i = A_i \oplus$) signals.
- These initial signals are the foundation for the carry calculation and are fed into the carry computation logic.

2. Carry Look-Ahead Logic

- CLA logic uses the generate and propagate signals to compute carry signals in parallel:
  - $C1 = G0 + (P0 \cdot C0)$
  - $C2 = G1 + (P1 \cdot C1)$
  - $C3 = G2 + (P2 \cdot C2)$
  - $C4 = G3 + (P3 \cdot C3)$
- Instead of waiting for each carry to propagate sequentially, the CLA logic computes each carry directly from the generate and propagate signals, significantly reducing delay.

3. Parallel Prefix Network

- The PPA uses a **prefix network** of **black cells** and **gray cells** to efficiently compute intermediate carries across stages.
  - **Black Cells**: Combine propagate and generate signals to pass them along the prefix tree.
  - **Gray Cells**: Generate only the final carry output without further propagation, reducing the logic required in the last stage.
- The prefix network creates a balanced tree structure, enabling carry computation in logarithmic time relative to the number of bits.

4. Sum Calculation

- Each sum bit Si is calculated with the final propagate and carry outputs:
  - $S_i = P_i \oplus C_i$

- This completes the addition operation, with all carries already precompute

Output waveform for C_{in} = 0 using above designed adder

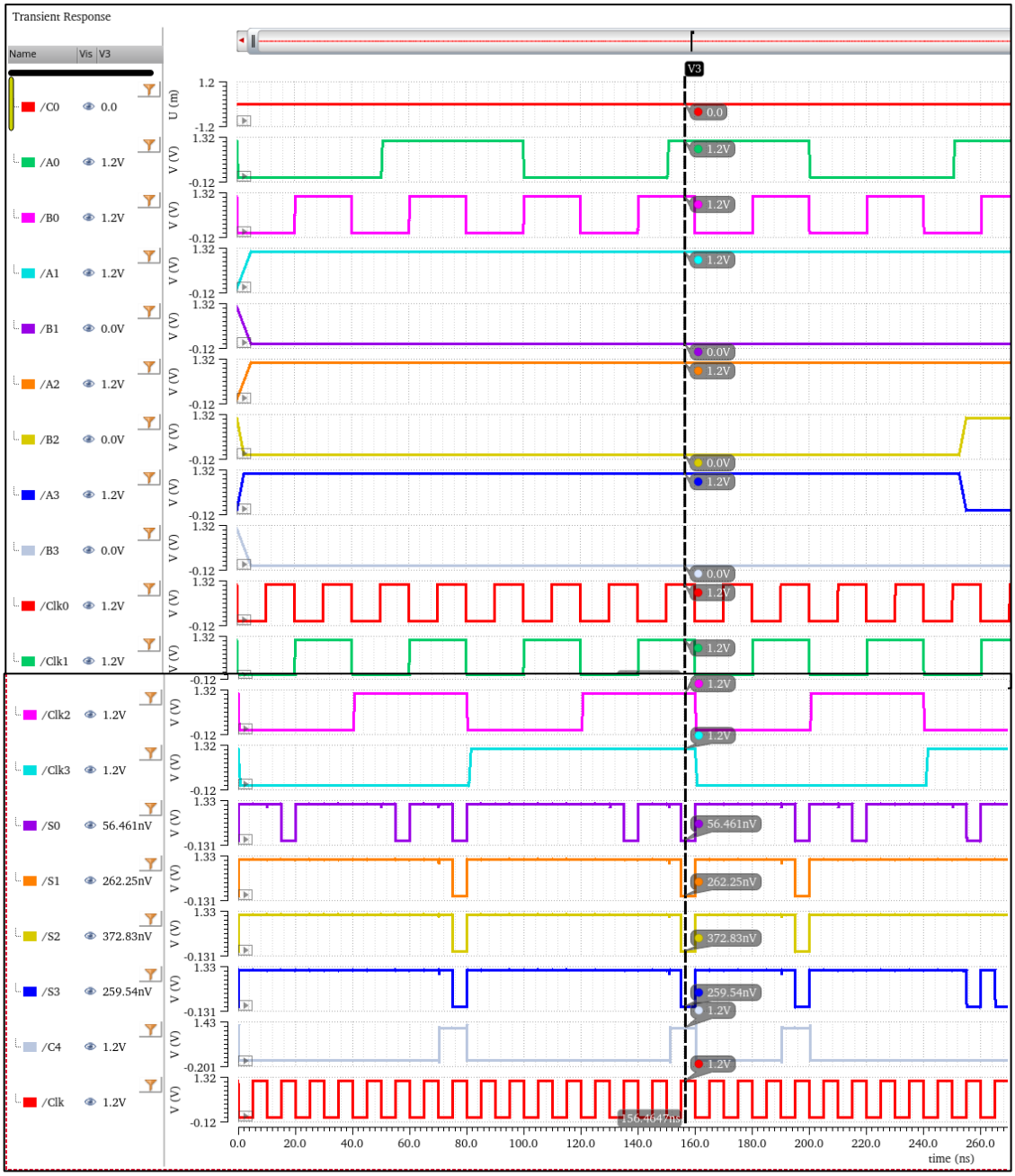

Fig. 6 : Output waveform for C_{in} = 0 using above designed adder

Input Combination:

A3 A2 A1 A0	1111
B3 B2 B1 B0	0001
Cin	0

For Cin=0,

Sum :

Calculated(S3 S2 S1 S0)	0000
From Waveform(S3 S2 S1 S0)	0000

Carry out :

Calculated(C4)	1
From Waveform(C4)	1

Output waveform for C_{in} = 1 using above designed adder

Input Combination:

A3 A2 A1 A0	1111
B3 B2 B1 B0	0001
Cin	0

For Cin=1,

Sum :

Calculated(S3 S2 S1 S0)	0001
From Waveform(S3 S2 S1 S0)	0001

Calculated(C4)	1

Carry out :

From Waveform(C4)	1

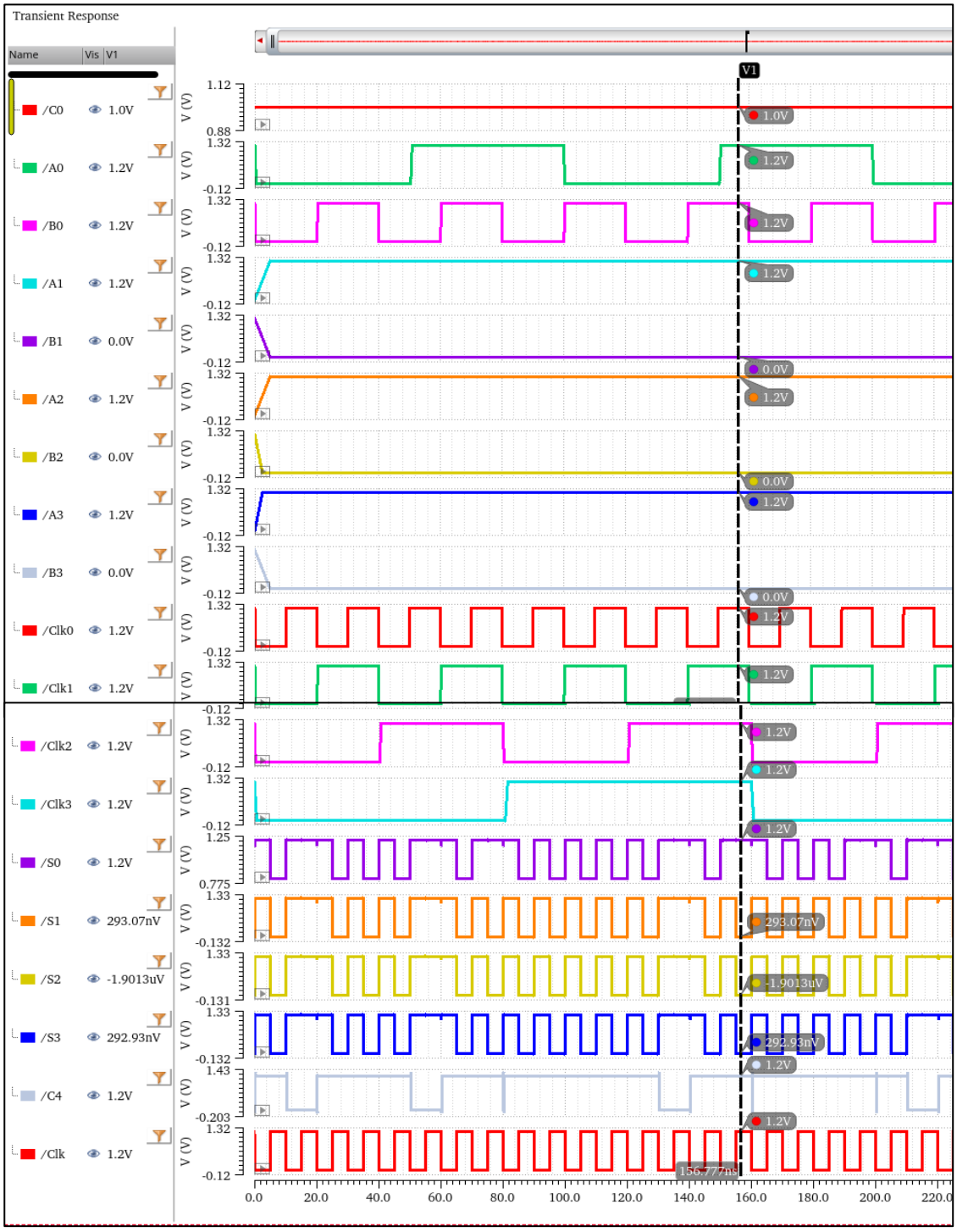

Fig. 7 : Output waveform for C_{in} = 1 using designed adder

Schematic of Parallel Prefix Adder implemented using Carry Select Logic

In this implementation of a **Carry Select Adder (CSA)** using **Parallel Prefix Adder (PPA) logic**, we combine high-speed addition with efficient carry selection. Each block of the adder precomputes sum and carry-out values for both possible carry-in values (0 and 1), using PPA to generate carries in parallel.

For each block:

- **Precomputed Sum and Carry**: The block computes two sets of outputs assuming both Cin=0 and Cin=1.
- **Multiplexer Selection**: A 2:1 multiplexer selects the correct output based on the actual carry-in from the previous block.

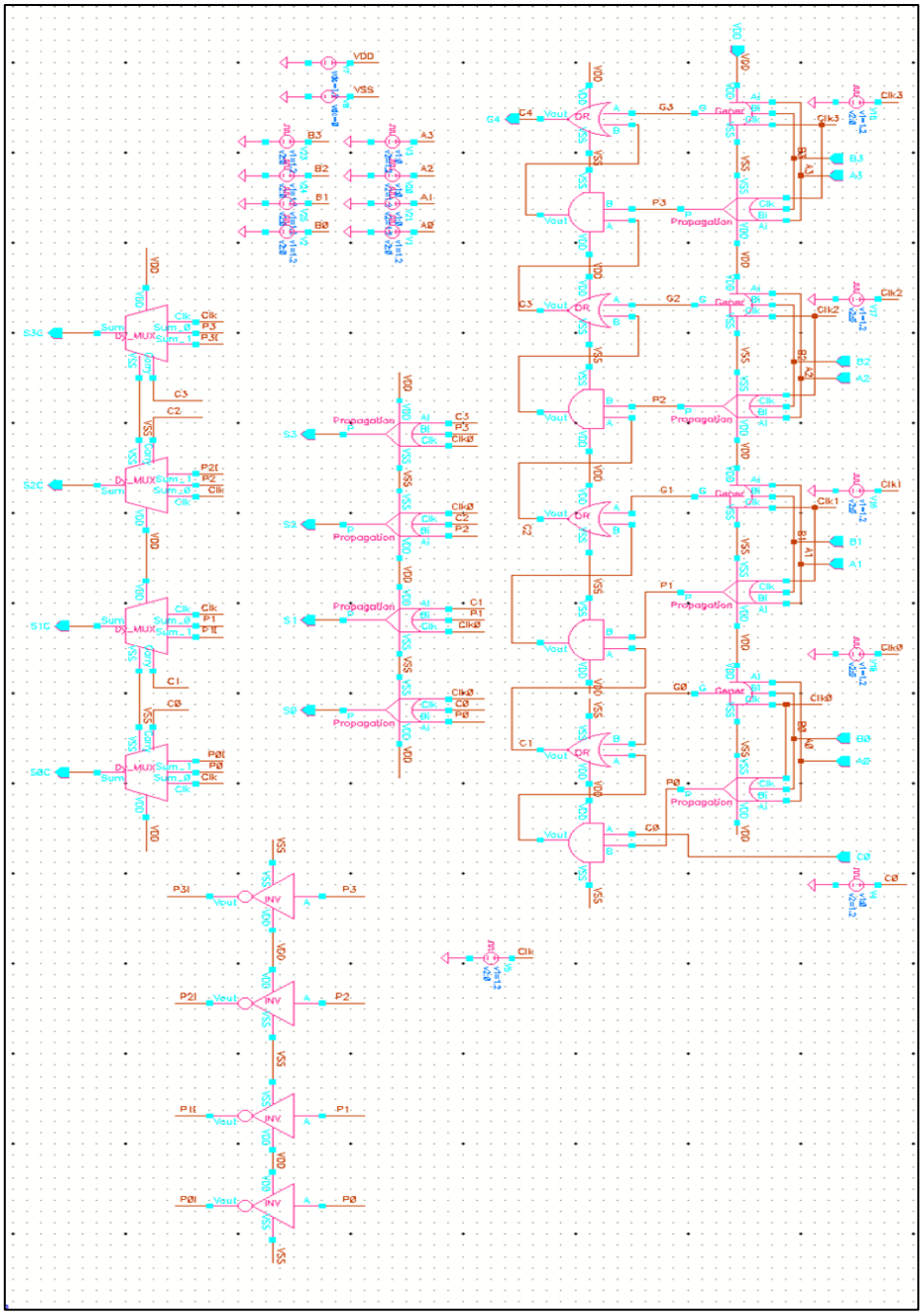

Fig. 8 : Schematic of Parallel Prefix Adder implemented using Carry Select Logic

This design minimizes delay by parallelizing the carry computation with the PPA structure and using multiplexers for rapid carry selection, allowing the CSA to achieve high-speed addition across all bits

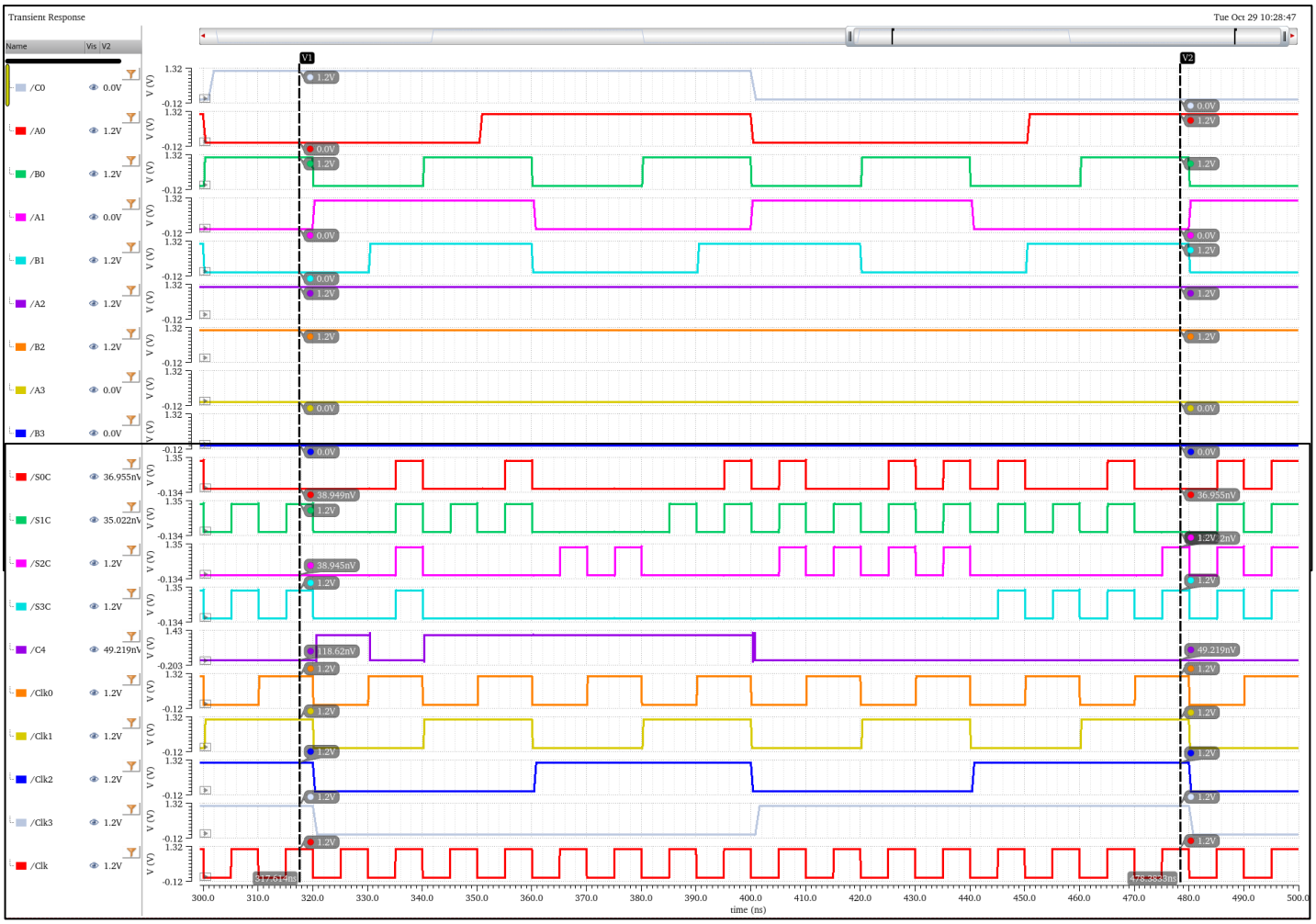

Fig. 9 : Waveforms for C_{in} = 0 and C_{in} = 1 (Sum selected according to input carry)

Case 1: Mux input (Cin)=1

Input Combination:

A3 A2 A1 A0	0100
B3 B2 B1 B0	0101
Cin	1

For Cin=1,

Sum :

Calculated(S3 S2 S1 S0)	1010
From Waveform(S3 S2 S1 S0)	1010

Carry out :

Calculated(C4)	0
From Waveform(C4)	0

Case 2: Mux input (Cin)=0

Input Combination:

A3 A2 A1 A0	0101
B3 B2 B1 B0	0111
Cin	1

For Cin=0,

Sum :

Calculated(S3 S2 S1 S0)	1100
From Waveform(S3 S2 S1 S0)	1100

Carry out :

Calculated(C4)	0
From Waveform(C4)	0

iii. Calculate its average power and performance by circuit simulation using the following technologies available in the laboratory (45 nm, 90nm, 180 nm technologies) and compare them with the existing literature.

Power Dissipation at 45nm:

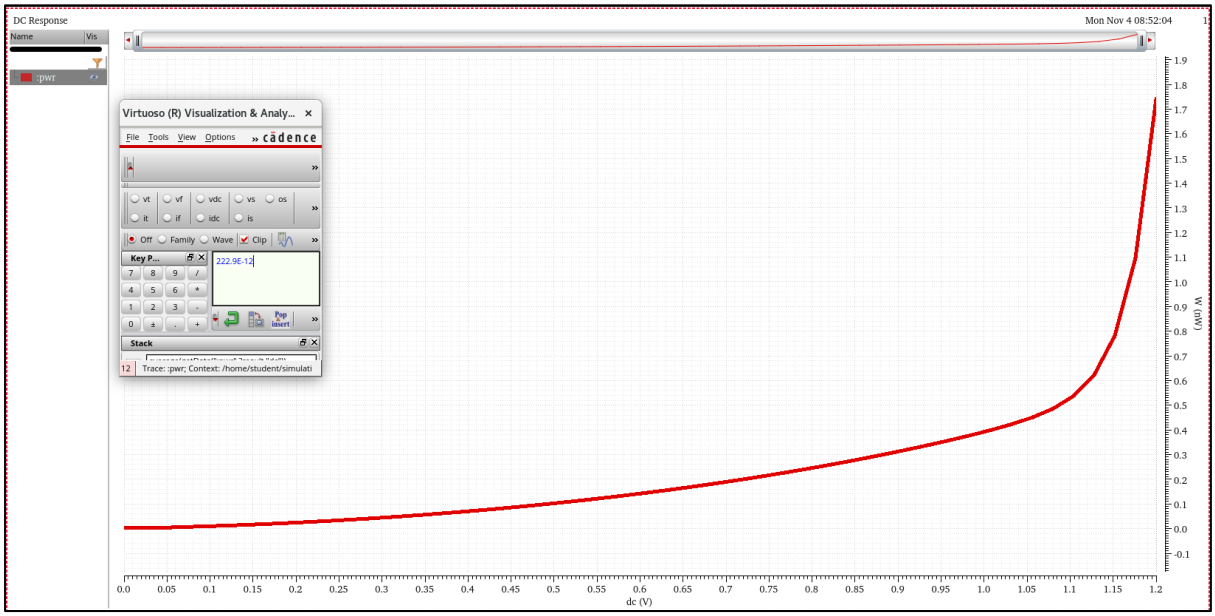

Fig. 10: Static Power Dissipation

The average static power dissipation during the Write operation is 222.9pW.

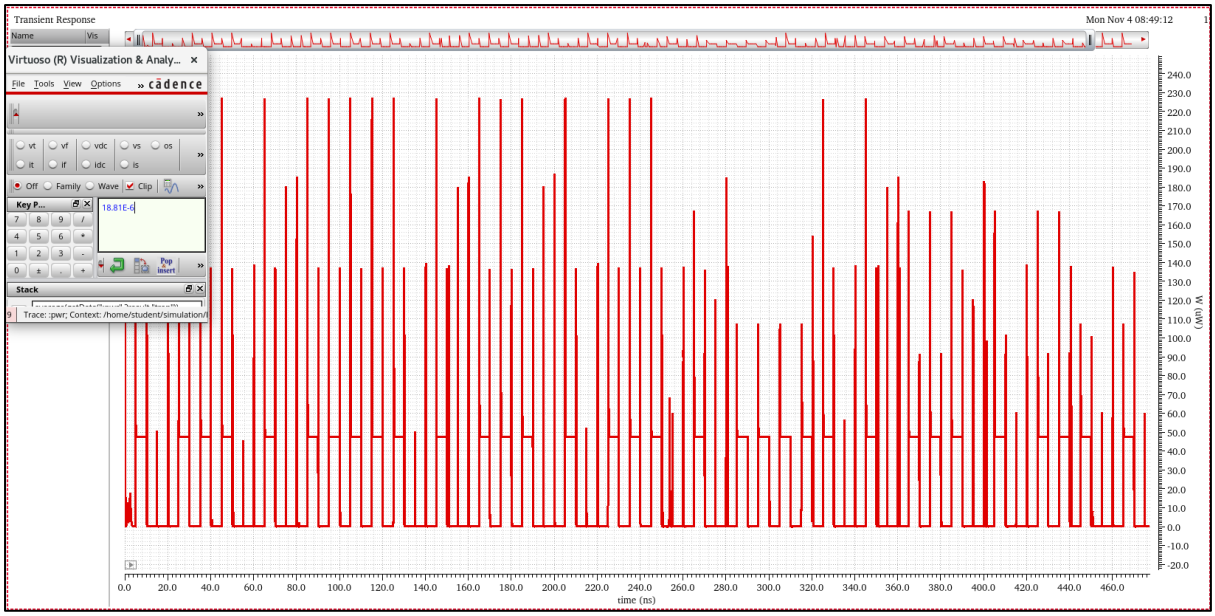

Fig. 11: Dynamic Power Dissipation

The average dynamic power dissipation during the Write operation is 18.81µW.

Thus, **Total Power Dissipation** = P_{Static} + $P_{Dynamic}$ = 222.9pW + 18.81µW = **18.81µW**

References:

1. Jan M, Rabaey, et al, Digital Integrated Circuits: A Design Perspective, Prentice Hall, 2003. (Chapter 11)
2. Neil Weste and K. Eshragian, Principles of CMOS VLSI Design: A System Perspective, Pearson Education, 2000.
3. Zheng, DY., Sun, Y., Li, SQ. et al. A 485ps 64-Bit Parallel Adder in 0.18μm CMOS. J Comput Sci Technol 22, 25–27 (2007). https://doi.org/10.1007/s11390-007-9002-1

Team Member	Contribution
Abhiram K M	**Literature Survey on Parallel Prefix Adders (PPA):** Researched Brent-Kung, Kogge-Stone, and Han-Carlson adders, highlighting their limitations in power, performance, area, power-delay product (PDP), and energy-delay product (EDP).
	Circuit Simulation: Designed a 4-bit adder using CLA and Carry Select Logic. Simulated and analysed the circuit, documenting its impact on power and performance.
	Power Dissipation Analysis: Calculated static and dynamic power dissipation at 45 nm, recording the effect on power efficiency.
	Documentation and Reporting: Compiled the final report, including the literature review, simulation data, and analysis of power dissipation.
Harshith Gowda B V	**Literature Survey on Parallel Prefix Adders (PPA):** Researched Brent-Kung, Kogge-Stone, and Han-Carlson adders, highlighting their limitations in power, performance, area, power-delay product (PDP), and energy-delay product (EDP).
	Circuit Simulation: Simulated and analysed the circuit, and verified the output for all input and carry combinations.
	Power Dissipation Analysis: Summarized power dissipation findings, recommending adjustments for reduced power consumption.
	Documentation and Reporting: Finalized the document format to meet project requirements.

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