MANIPAL INSTITUTE OF TECHNOLOGY
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Project Synopsis On

Partition-Level Timing Analysis and Closure Methodology for Advanced SoC Designs

MASTER OF TECHNOLOGY

IN

MICROELECTRONICS

Submitted by,

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ABSTRACT

With continuous scaling of semiconductor technology, modern System-on-Chip (SoC) designs have reached high levels of complexity, integrating millions of transistors on a single die. Achieving timing closure for such designs requires a proper understanding of the entire digital design flow — from Register Transfer Level (RTL) synthesis to place-and-route, parasitic extraction, and finally static timing analysis (STA). The proposed work focuses on partition-level timing analysis and closure within a full-chip environment of an advanced SoC design. The selected partition comprises several hundred thousand combinational and sequential cells, including flip-flops, latches, and Hard IP (HIPs), thus representing a live industrial block.

The project involves studying, understanding and implementing the complete flow of timing convergence across multiple design stages. Beginning from RTL synthesis, the design undergoes optimization and physical implementation using standard EDA tools. Post-layout parasitic extraction and STA are then performed to identify and resolve setup, hold, and design rule violations under multiple process, voltage, and temperature corners. The methodology includes iterative timing closure using Engineering Change Orders (ECOs) while minimizing area and power overhead. By exploring the interdependencies between synthesis constraints, placement strategies, and timing optimization techniques, the work aims to achieve a stable and signoff-quality timing closure for the partition at full chip level. The outcome of this project contributes toward building an optimized and predictable timing closure methodology for large-scale SoCs.

In addition to timing analysis, the project emphasizes on managing inter-partition SoC level timing dependencies, which are critical in achieving convergence for hierarchical SoC designs at Full Chip level. Techniques such as path-based analysis, clock domain isolation, and constraint refinement are explored to improve both accuracy and efficiency of the timing closure process.

The insights gained from this work are expected to strengthen the understanding of end-to-end digital implementation flow from RTL to signoff. The project not only enhances technical expertise in physical design and timing optimization but also provides practical exposure to the challenges faced in industrial environments where large designs operate under tight power-performance-area trade-offs.

INTRODUCTION

Background:

The evolution of semiconductor technology has followed Moore's Law, which predicts that the number of transistors on a chip doubles approximately every two years. This exponential growth has enabled modern System-on-Chip (SoC) designs to integrate millions of transistors, including digital and analog subsystems, memory blocks, and interface modules, all on a single chip. Ensuring correct and predictable operation across all timing paths becomes a critical challenge as SoCs become more complex.

Timing analysis is a fundamental aspect of SoC design, especially in fully synchronous designs, where the clock regulates the sequential behavior of circuits. Static Timing Analysis (STA) has emerged as the standard methodology for verifying timing correctness without requiring dynamic simulation. STA examines all possible timing paths under multiple operating conditions and parasitic scenarios, identifying setup and hold violations, maximum and minimum delays, and clock uncertainty.

Motivation:

With increasing transistor counts and lowering technology nodes, achieving timing closure has become one of the most difficult aspects in advanced SoC design. STA provides a systematic approach to identify critical paths, setup/hold violations, and inter-partition timing dependencies. However, as designs scale, manual closure becomes inefficient and error prone. The project is motivated by the need for robust, repeatable, and automated STA-based timing closure methodologies that can handle the complexity of industrial-scale SoC partitions.

Relevance:

STA is highly relevant to both academic research and industries. Academically, it applies theoretical digital timing concepts — such as setup, hold, clock skew, and derating — with real-world implementation challenges. Industrially, accurate STA and timing closure are crucial for ensuring that large-scale SoCs meet performance, power, and reliability targets. Mismanaged timing can lead to failures, increased ECO iterations, and delayed design signoff.

Problem Definition:

In modern SoC design flows, achieving full-chip timing closure across multiple partitions poses a significant challenge due to increasing design complexity, shrinking technology nodes, and tighter power, performance and area (PPA) trade-offs. Each partition within a full-chip design must independently achieve timing convergence before final integration, demanding high precision in constraint definition, delay modelling, and path optimization. The primary goal of this work is to explore and implement partition-level timing analysis and closure techniques followed by full chip SoC timing convergence.

The objective is to analyze and close timing for a representative partition of an industrial SoC using industry-standard Synopsys EDA tools. The selected partition consists of *320,813 combinational cells and 51,972 sequential elements, which include 51,921 flip-flops and registers, 543 latches, and 82 HIPs* The complexity and scale of this partition provide a practical platform to study real-world timing challenges such as clock skew, on-chip variation, and constraint correlation across multiple hierarchical levels. Fig. 1 shows the rough floorplan of the Full Chip SoC, which also indicates the Partition to be analyzed.

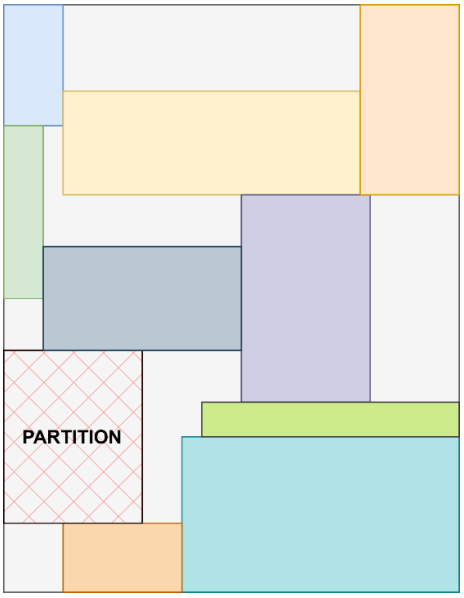

Fig.1: Rough Floorplan of the SoC

The work focuses on understanding the complete RTL-to-GDSII flow, with emphasis on the timing signoff stage, involving constraint validation, timing path analysis, and engineering change order (ECO) closure. The process includes identifying setup and hold violations, validating multi-mode multi-corner (MMMC) scenarios, and applying effective optimization strategies for timing convergence.

The initial objective is to achieve timing convergence at the partition level. Once this is accomplished, both internal and external paths to the partition are analyzed using an FCT (Full Chip Timing) model. These paths are then modelled for timing convergence at the full-chip level. It is important to note that a path may appear to meet timing at the partition level but still violate timing at the SoC level. Ultimately, timing closure must be achieved at the full-chip level, as sign-off occurs at the SoC level. Therefore, ensuring that each partition is cleanly integrated and stitched at the full-chip level is critical to achieving overall timing convergence at the top level.

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Deliverables

At the end of the project, the following outcomes are expected:

1. **Partition-Level Timing Closure:**
   Achievement of signoff-quality timing closure for the selected SoC partition at the Full Chip level, ensuring that all setup, hold, and clock uncertainty violations are resolved across multiple process, voltage, and temperature corners.
2. **Detailed Timing Reports and Analysis:**
   Generation of comprehensive timing reports, including critical path identification, slack analysis, and timing exception handling, providing a clear understanding of partition-level timing behavior.
3. **Optimization of Critical Paths:**
   Implementation of targeted Engineering Change Orders (ECOs) and constraint refinements to optimize timing on critical paths, reduce slack violations, and improve overall design predictability.
4. **Timing Closure Methodology Documentation:**
   Preparation of a structured methodology document detailing the techniques, best practices, and flow followed for timing analysis, closure, and optimization.
5. **Insights on Timing Optimization:**
   Quantitative evaluation of timing improvements, including reduced ECO iterations, improved critical path slack, and enhanced confidence in partition-level and full-chip timing convergence.

Key tools to be used: *Synopsys PrimeTime*

Timeline

June-July 2025	To understand STA run structure and overview of basic STA concepts and commands
August 2025	To get familiar with Unix Environment and understanding Timing constraints and Timing exceptions
September 2025	To perform basic STA checks and analysis at different stages To understand and perform ECO generation Flow and Overview of PVT & OCV derates
October -November 2025	To start working on the assigned partition CFO (Compile Final Opt) Stage Checking for no clocks, unclocked registers, linking issues and timing loops
December 2025-January 2026	Checking for unconstrained endpoints Providing I/O budgeting and Checking I/O Constraints Quality Modelling of Critical paths with high Negative slack
February 2026	CTS Stage Checking in skew, Latencies Checking whether logics are placed properly and floorplan is proper or not
March-April 2026	Route opt Stage (Datapath Routing) Checking for Setup, Hold, Annotated nets, Transition time, Capacitance Analyzing the possible fixes and giving feedback
May 2026	ECO generation and sign off

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[5] https://www.cadence.com/en_US/home/explore/timing-closure.html

Place of Execution of work: *Intel Technology India Pvt. Ltd. Bangalore – 560103, India*

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Letter of permission

Internship letter

KL

Krishnan, Lisha
To K M, Abhiram

Reply | Reply All | Forward

Fri 31-10-2025 05:22 PM

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Start your reply all with: Thank you! | Got it, thanks! | Thank you for your confirmation.

Hi,

This is to confirm that "Abhiram K M" is working as an intern in Intel India Pvt Ltd from June 02 ,2025 on a project titled "Partition-Level Timing Analysis and Closure Methodology for Advanced SoC Designs "

Thanks
Lisha