Advanced Placement Interview Questions & Solutions (3 Years Experience - Physical Design: Placement)

Prepared by VLSI FOR ALL / Rajat Kumar Singh

1. Explain the overall placement flow in PnR. How do global placement and detailed placement differ?

Placement flow begins after floorplanning and legalization of macros. Global placement optimizes cell locations to minimize wirelength and timing cost without detailed routing awareness; it focuses on partitioning, analytic spreading, and congestion estimation. Detailed placement resolves standard-cell legalization, cell alignment to rows, local swaps, and timing-driven optimizations ensuring DRC-compliant cell locations ready for routing.

2. How does legalization work after placement?

Legalization converts float positions from global placement to legal cell locations aligned to rows and site pitches. It addresses overlaps by shifting/swapping cells, using local reordering and legalization engines to meet placement rules while preserving timing and wirelength as much as possible.

3. How does placement affect setup and hold violations?

Placement determines net lengths and buffer insertion points — longer net/higher delay can harm setup (late arrival). Hold violations occur when paths become too fast (short parasitic delays) or due to buffer insertion. Placement impacts buffer insertion candidates and skew; timing-driven placement seeks to minimize WNS (setup) while avoiding creating new hold paths by considering net delays and adding minimal buffering or path-specific fixes.

4. What optimization techniques/tools are used for timing-driven placement?

Techniques include timing-cost-based analytic placement, critical-path clustering, slack-aware cell spreading, and incremental placement. Tools (Cadence Innovus, Synopsys ICC2, Mentor Olympus-SoC) provide timing-driven placer modes, scripting to constrain critical regions, and iterative optimization with STA feedback.

5. What factors contribute to routing congestion during placement?

High cell density, poor macro placement, long skinny channels, unrestricted standard-cell orientation, uneven pin distribution, and insufficient routing resources (vias/metal layers) lead to congestion. Lack of power/clock planning and misaligned placement of high-fanout nets exacerbate it.

6. How do you analyze and fix congestion at the placement stage?

Use congestion maps from the placer, identify hot regions, and apply tactics: spread cells, reserve routing channels, relocate macros, create blockages for routing or reserve higher metal layers for global nets, and perform net clustering/unclustering. Adjust target utilization or introduce routing-aware placement constraints and rip-up non-critical nets.

7. Why do clock buffers and CTS cells need special consideration during placement?

Clock buffers are large and consume routing and power resources; their placement affects clock tree balance and skew. Poor placement can increase buffer count, routing congestion, and SSN. Place clock sinks with awareness of CTS regions, reserve space for clock routes, and prevent clock buffer clustering that hampers routing.

8. How do you ensure clock tree doesn’t worsen congestion?

Reserve routing channels for clock nets, use higher metal layers for clock distribution, avoid placing high-fanout sinks in dense data regions, and collaborate with CTS engineers to select buffer sites. Floorplan clock regions and iterate placement with CTS feedback to minimize routing overlap.

9. How do you handle placement of multi-voltage domain cells?

Group cells by voltage domains, place level shifters at domain boundaries, and ensure sufficient space for isolation and power-gating cells. Maintain rails continuity and reserve power routing channels. Follow UPF/CPF intent and enforce placement constraints to avoid cross-domain net issues.

10. What's the impact of power gating switches on placement?

Power gating cells are large and require placement near domain boundaries; they influence routing and timing. They also introduce wake-up current demands and may necessitate local decaps. Plan their placement to minimize IR/EM impact and avoid creating congestion or timing cliffs.

11. What is placement blockage and how is it used?

Placement blockage are areas where standard cells cannot be placed—used to protect routing channels, macros, keep-out zones, and analog regions. Use blockages to guide the placer away from sensitive areas, reserve space for routing or power, and enforce floorplan constraints.

12. How do you handle placement near macros/SRAMs/IOs?

Maintain proper placement density around macros, respect macro keep-outs, align cell rows to macro boundaries, and ensure sufficient pin access and taping for power/vias. Place timing-critical cells close to macro pins and reserve routing for macro interface nets.

13. Explain min-cut vs analytical placement methods.

Min-cut placement partitions the netlist recursively to minimize cut size and later refines; it's simple and fast for block-level partitioning. Analytical placement (quadratic or nonlinear) formulates wirelength and congestion as continuous optimization and solves using numerical methods—better for global optimization and handling large designs with smooth spreading.

14. Why is wirelength optimization critical in placement?

Shorter wirelength reduces delay, power, and routing resources, improving timing and manufacturability. It reduces congestion, via counts, and improves signal integrity. Wirelength is a primary objective combined with timing cost in modern placers.

15. Where do you place tie-high, tie-low, isolation, and level shifter cells?

Place tie-high/low cells near scan/unused inputs or where power-down states require static logic levels. Isolation and level shifters should be near domain boundaries—typically on the source-side domain—to minimize long cross-domain routing. Follow UPF mapping to ensure their netlists and placement match power intent.

16. How do filler cells affect placement density and DRC closure?

Filler cells maintain rail continuity and pitch; they fill gaps to meet manufacturing density and DRC requirements. Incorrect filler usage can leave open rails or break power continuity; proper filler placement ensures LVS/DRC compliance and supports predictable routing.

17. How do you handle last-minute ECO placement changes?

Perform incremental placement—lock non-affected regions, place ECO cells close to related nets, run localized legalization and incremental STA. Use placement scripts to minimize global disturbance, re-evaluate congestion, and run focused timing fixes to preserve WNS/TNS.

18. How is MCMM considered during placement optimization?

In MCMM, create composite timing costs that account for multiple corners/modes, prioritize nets that are critical across corners, and use multi-corner aware placement heuristics. Balance trade-offs by focusing on worst-case corners while ensuring no other mode regresses beyond acceptable margins.

19. What is target utilization and how do you decide it?

Target utilization is the fraction of core area allocated to standard cells. Decide based on design complexity, routing resources, and timing: lower utilization eases routing and reduces congestion but increases die size; higher utilization saves area but risks congestion. Typical targets vary by node and IP mix (e.g., 60–75%).

20. How does placement affect IR drop and routing resources?

Placement dictates current paths; clustering high-power cells without adequate via/strap access increases local IR drop. Dense regions impede power strap insertion and via stitching. Ensure power-aware placement by distributing power-hungry cells, aligning them to power straps, and coordinating with PDN planning.

21. Why is scan chain reordering done after placement and how does it affect routing?

Reordering minimizes interconnect length between scan registers, reducing routing and improving test time. After placement, physical proximity information allows building efficient chains that lower routing congestion and shift test resources to less critical routing layers.

22. What metrics do you check after placement to ensure quality?

Check HPWL (half-perimeter wirelength), WNS/TNS (worst/total negative slack), congestion maps, utilization, timing path counts, and preliminary power/IR estimates. Also review DRC/post-placement LVS and cell alignment statistics.

23. If WNS worsens after placement, what steps do you take to debug?

Identify critical paths and their net delays, check buffer/inverter insertion, examine parasitic extraction differences, and review congestion-induced detours. Actions: move critical cells closer, legalize or swap cells, insert buffers, adjust placement directives, or relax non-critical area constraints.

24. How do you plan placement for high-speed I/O and SERDES regions?

Place SERDES and high-speed IO close to the package pins and allocate dedicated routing channels and
shielding. Keep analog/bias supplies and termination networks nearby, ensure low-latency paths to PHY macros, and reserve high-quality metal layers for IO routing and high-speed traces.

25. How do you coordinate with backend teams (CTS, Routing, Signoff) during placement?

Maintain iterative communication—share placement checkpoints, congestion forecasts, and critical-path maps. Run collaborative iterations: give CTS reserved sites, get CTS buffer placements back, adapt placement based on signoff IR/EM feedback, and converge through incremental optimizations.

Notes:

- This document provides concise solutions and practical notes for advanced placement interview preparation (3 years experience).
- Customize strategies based on process node, IP mix, and tool flows (e.g., Cadence Innovus, Synopsys ICC2, Mentor tools).
- Practice with real design checkpoints and placement tool reports for hands-on readiness.