

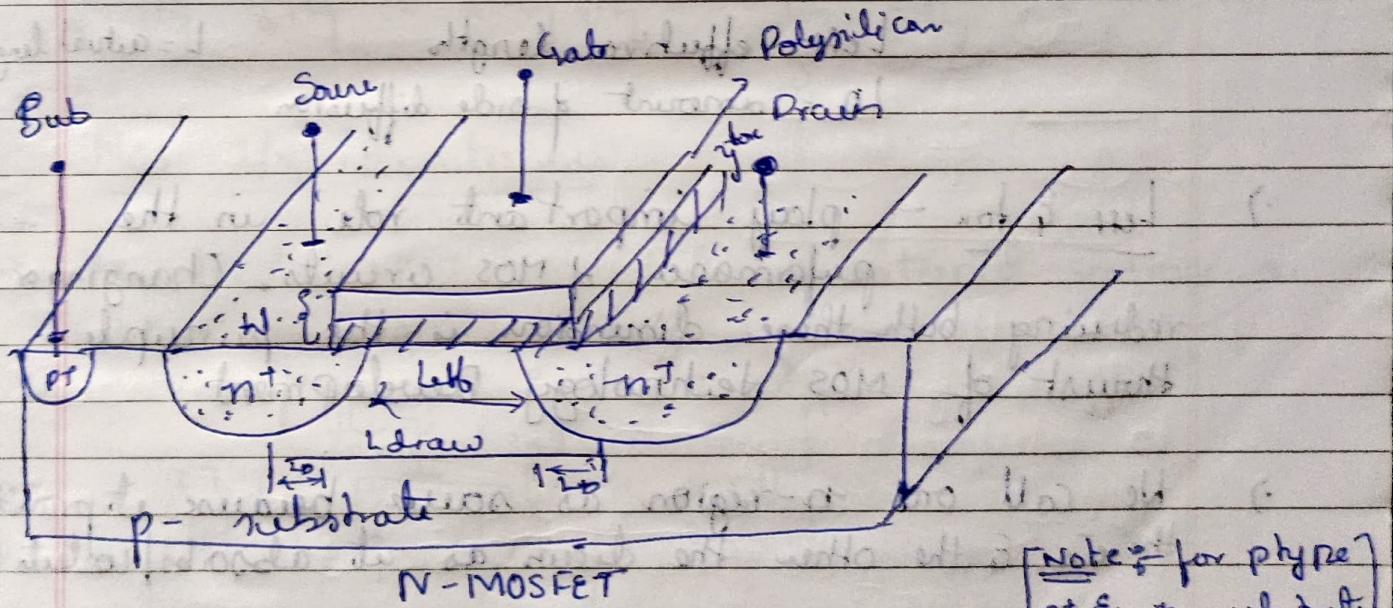
Analog

:) Gordon Moore:- Every one and half years transistors per chip is doubled and dimensions will decrease.

Observation

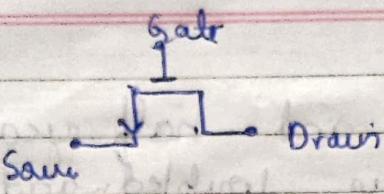
- $\propto C \propto V$ (i.e., V & C are inversely proportional)
- If voltage V , Q_T & electron density P are constant
- If thickness of the dielectric t , capacitance C , Q_T & density P are constant

MOS (Metal Oxide Semiconductor Structure)



- MOSFET \rightarrow 4 terminal device
- Mos structure is symmetric
-)

MOSFET as a switch:- It turns on when gate is high (i.e. transistor connects the source & drain) and turns off when gate is low (i.e. isolates source and drain) for nmos



MOSFET Structure

- Lateral dimension of the gate along source-drain path is called length, L , & that perpendicular to length is called the width, W .
- Since the S/D junction "side-diffuse" during fabrication, the actual distance between the source and drain is slightly less than L .
- Therefore, $L_{eff} = L_{drawn} - 2D$. (where D is side diffusion)

L_{eff} = effective length

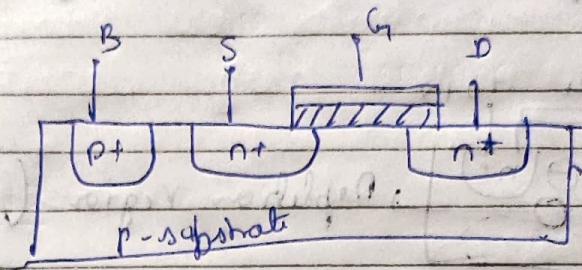
L = actual length

$2D$ = amount of side diffusion

- L & W → play important role in the performance of MOS circuits. Changing or reducing both these dimensions is the principle thrust of MOS technology development.
- We call one n-region as source because it provides the carriers & the other the drain as it absorbs/collects the carriers.
- MOS is symmetric → Source & Drain can be exchanged based on voltage provided.

MOS Symbols

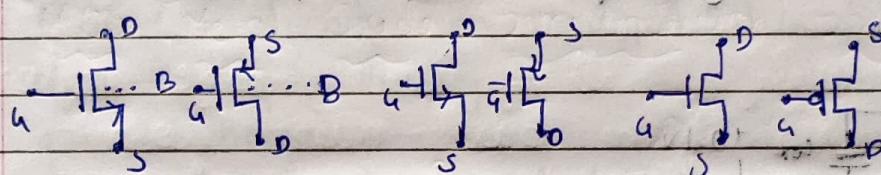
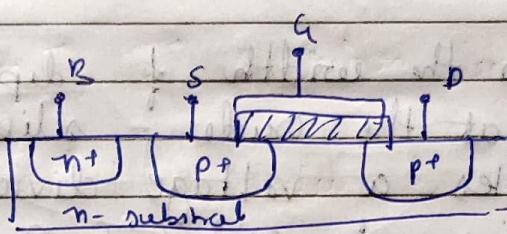
NMOS :-



n^+ highly doped

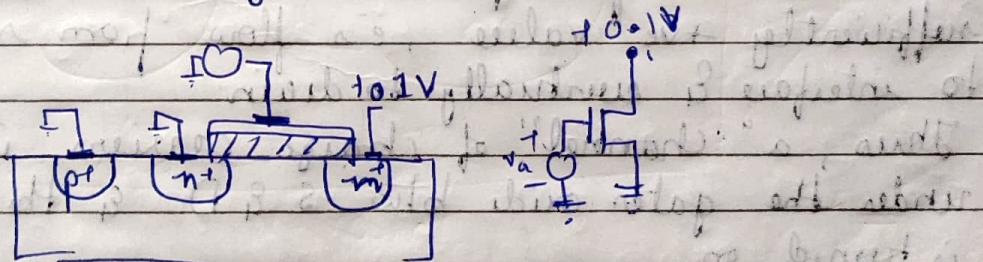
$(10^{19} \text{ to } 10^{20} \text{ atoms/cm}^3)$

PMOS :-



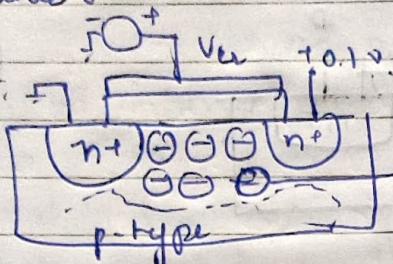
Mos I/V Characteristics

- Consider an NFET connected to external voltages as shown in figure below.



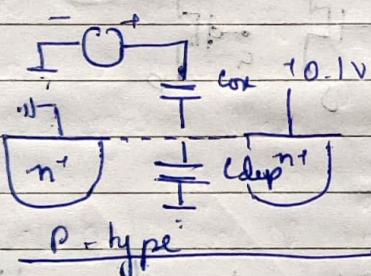
- The polysilicon gate, the dielectric & the substrate form a capacitor, as V_G increase from zero.
- As we increase V_G even more, the holes in the p-substrate are repelled from gate area, leaving negative ions behind so as to mirror the charge on the gate.

- Depletion region is created & in this condition no current flows as no charge carriers available.



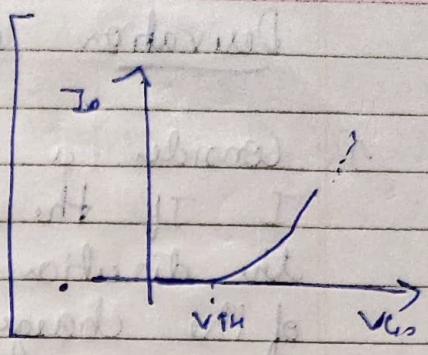
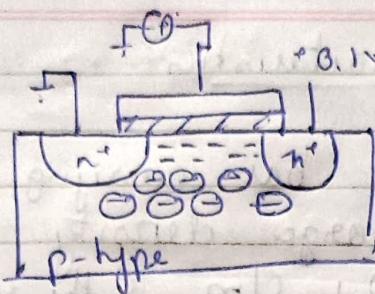
Depletion region (having only cations)

- As $V_G \uparrow$, so do the width of depletion region & the potential at the oxide - silicon interface.
- It resembles a voltage divider consisting of 2 capacitors (i.e. gate-oxide & Depletion region) in series.



(not inverted) v/t 30M

- When the interface potential reaches a sufficiently +ve value, e⁺ flow from source to interface & eventually to drain.
- Thus, a "channel" of charge carriers is formed under the gate oxide btw S & D & the transistor is turned on.
- The channel is also called inversion layer as the interface is inverted.
- The voltage at which the inversion of the channel occurs is called threshold voltage (V_{TH}).
- If V_G rises further, the charge in the depletion region remains constant while charge density ρ , current from D to S ↑



$$V_{TH} = \phi_{MS} + 2\phi_F + \frac{Q_{dep}}{C_{ox}}$$

$$\phi_F = (kT/q) \ln \left(\frac{N_{sub}}{n_i} \right), \quad k = \text{Boltzmann's Constant} = 1.38 \times 10^{-23} \text{ J/K}$$

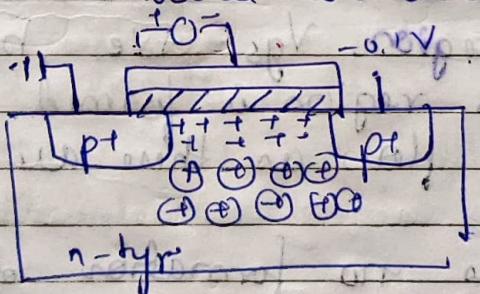
\downarrow Work fun. of silicon substrate $= 1.38 \times 10^{-23} \text{ J/K}$

- .) n_i \rightarrow e⁻ density in undoped Silicon
- .) N_{sub} \rightarrow doping density
- .) q \rightarrow e⁻ charge
- .) Q_{dep} \rightarrow charge in the depletion region
- .) ϕ_{MS} \rightarrow Work function of poly-silicon gate

[Workfun]: - The minimum quantity of energy required to remove an e⁻ to infinity from surface of given solid

Notes: In PMOS, all the polarities are reversed.

V_{DS} becomes sufficiently -ve, an inversion layer consist of holes, providing a conduction path between source and drain.

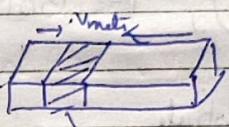
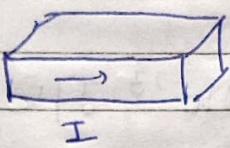


Derivation of I/V characteristics

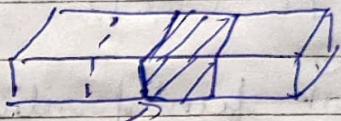
- Consider a semiconductor bar carrying a current I . If the mobile charge density along the direction of current Q_d C/m & the velocity of the charge is v meters per second, then

$$I = Q_d \cdot v$$

drift velocity



later



- With velocity v , all of the charge enclosed in v meters of the bar must flow through the cross section in one second.
- Since, the charge density is Q_d , the total charge in v meters is $Q_d \cdot v$.

Let us derive I_{ds} for 3 regions, namely cut-off, linear region & saturation region

a) Cut-off region of bar

In cut-off region, $V_{gs} = +ve$, but $V_{go} < V_t$ i.e. the depletion region is formed but there is no current flow as there are no charge carriers.

Hence, there is no formation of channel btw drain and source

∴ $I_{ds} = 0 A$

(b) Linear Region:

- 1) In linear Region, $V_{GS} > V_t$, E channel is formed btwn D & S
- 2) In linear region
 $V_{GS} > V_t$ & $V_{DS} < V_{GS} - V_t$
As soon as voltage is applied btwn drain and source, the e^- 's start to flow & sets up current I_{DS} .
- Note:- Without V_{DS} , I won't flow even though gate voltage is greater V_t because there is no potential difference between source to drain which can make the e^- 's flow, as soon as it is provided e^- 's gets attracted towards the drain & $I \uparrow$ from $0 \rightarrow S$

$$\text{WKT. } I = \frac{Q}{t} \quad \text{i.e. } I_{DS} = \frac{Q_n}{t}$$

where $Q = \text{charge}$

$t_f = \text{transit time}$ which is the time taken by the e^- to reach drain from source

$$\text{WKT. } T_z \text{ distance} \rightarrow \frac{L}{\text{velocity}}$$

$v = uE$; $u = \text{mobility of } e^-$ & $E = \text{Electric field}$
↳ drift velocity

$$\text{Hence } E = \frac{\text{Voltage}}{\text{distance}}$$

$$E = \frac{V_{DS}}{L}$$

$$\therefore V = \mu \left[\frac{V_{ds}}{L} \right]$$

$$t_f = \frac{L}{\mu \left[\frac{V_{ds}}{L} \right]}$$

$$t_f = \frac{L^2}{\mu V_{ds}}$$

∴ The charge density is $V_{ds} - V_{TH}$

∴ For $V_{ds} \geq V_{TH}$,

$$Q_d = W C_o x (V_{ds} - V_{TH})$$

WKT. $C_o = \text{Capacitance}$

$$C_o = \frac{\epsilon A}{d}$$

$A \rightarrow \text{area}$

$\epsilon = \text{permittivity}$

$d = \text{distance}$

$$C_o = \frac{\epsilon o x (L \cdot W)}{d}$$

$$\left[\frac{\epsilon o x}{d} = C_o \right]$$

$$C_o = C_o x L \cdot W$$

$$C_o = C_o x W \text{ (per unit length)}$$

∴ Suppose the drain voltage is greater than channel zero.

∴ potential varies from zero to V_d at drain.

∴ Mobility potential varies from gate to drain.

i.e. $V_G - V_d$.

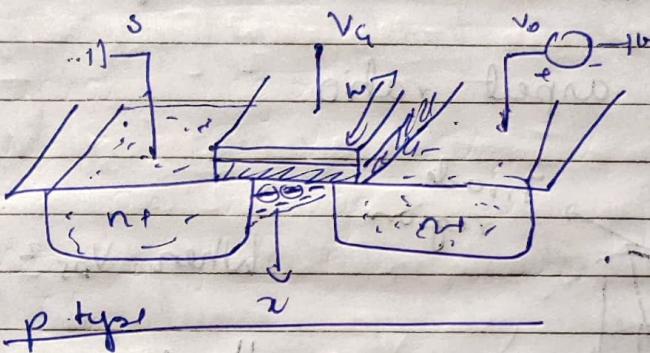
∴ Thus charge density at point x is given by

$$Q_d(x) \rightarrow W C_o [V_{ds} - V(x) - V_{TH}]$$

Current I_{DS} can be given by

$$Q_D V_s - W C_{ox} [V_{GS} - V_{th} - V_{DS}] \sim I$$

$$I_D = -W C_{ox} [V_{GS} - V_{th} - V_{DS}] \sim I$$



-ve sign
indicates
charge carrier
are -ve

$$V = \mu_n E$$

$$E = -\frac{dV}{dx}$$

[given in previous page]

$$I_D = W C_{ox} [V_{GS} - V_{th} - V_{DS}] \mu_n \frac{dV}{dx}$$

This is subjected to the boundary conditions
 $V(0) = 0$ & $V(L) = V_{DS}$

$$I_D dx = W C_{ox} [V_{GS} - V_x - V_{DS}] \mu_n dV$$

Integrating

$$\int_{x=0}^L I_D dx = \int_{V=0}^{V_{DS}} W C_{ox} [V_{GS} - V_x - V_{DS}] \mu_n dV$$

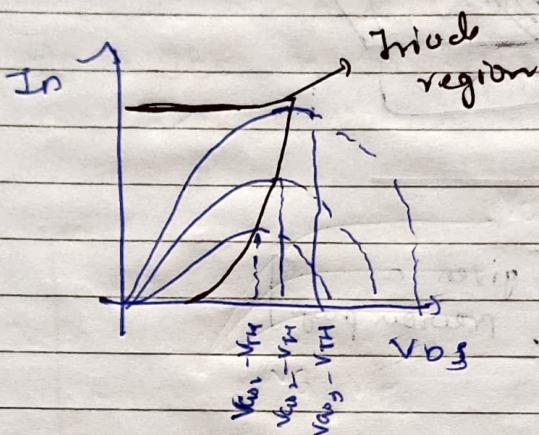
$$I_D [L] = W C_{ox} [V_{GS} - V_{DS}] \left[\frac{V_{DS}^2}{2} \right]$$

$$I_D [L] = W C_{ox} \mu_n \left[V_{GS} \cdot V_{DS} - V_{th} V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$I_D = \frac{W}{L} C_{ox} n \mu \int (V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2}$$

$V_{GS} - V_{TH}$ = Overdrive voltage

$\frac{W}{L}$ = aspect ratio



When $V_{DS} \geq V_{GS} - V_{TH}$,

the device is

?

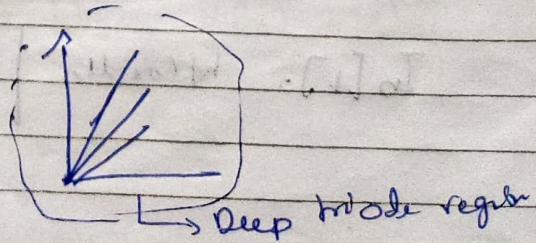
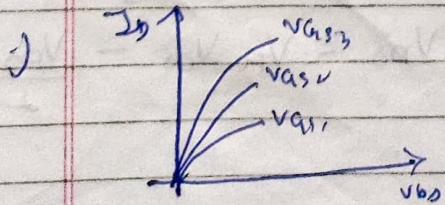
If $V_{DS} \leq 2(V_{GS} - V_{TH})$,
I_D will be linear fun' of V_DS

$$I_D \approx I_{DSS} \text{Cox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS} \left[\frac{V_{DS}}{I_{DSS}} + \frac{R_{on}}{L} \right]$$

2. If V_DS is too small, path b/w S & D can be represented as a linear resistor whose value is

$$R_{on} = \frac{1}{\text{Cox} \text{C}_{ox} \frac{W}{L} (V_{GS} - V_{TH})}, \text{ This value is controlled by } V_{DS}$$

This condition or region is called deep triode region



Note:-) I_S & I_b are the other currents apart from I_D , but we don't use it because $I_S = I_D$ as path is there & same current flows.

) I_{D20} because its connected to a capacitor & capacitors don't conduct for DC currents.

i) Saturation region,

- When $V_{DS} \geq V_{GS} - V_{TH}$, I_D becomes relatively constant & device operates in saturation region thus
- As $V_{DS} \uparrow$, I_D drops to zero

$$\text{at } V_{DS} = V_{GS} - V_{TH}$$

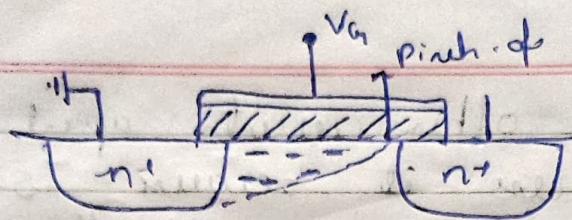
$$I_D = \frac{W \text{Conduct}}{L} \left((V_{GS} - V_{TH})^2 - \frac{(V_{GS} - V_{TH})^2}{2} \right)$$

$$I_D = \frac{W \text{Conduct}}{2L} (V_{GS} - V_{TH})^2$$

- This indicates I_D is independent of V_{DS}
- If I_D is known

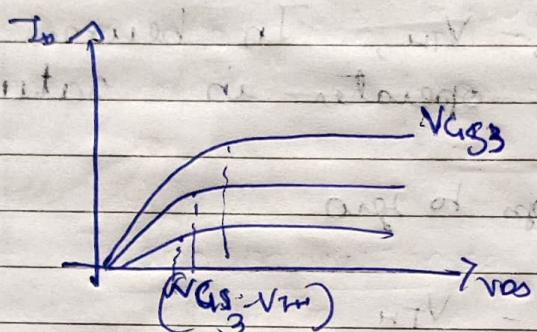
$$V_{GS} = \sqrt{\frac{2I_D}{W \text{Conduct}}} + V_{TH}$$

- When $Q_d \rightarrow 0$, at point $x=L$, i.e. $x \leq L$, no channel is pinched off
- As the e⁻ approach the pinch-off point, their velocity ↑.
- Upon passing the pinch-off point, the e⁻ simply shoot through the depletion region near the drain junction & arrive at the drain terminal



Note: For PMOS $I_D = k_d \cdot \text{dep}(\cos \frac{W}{L}) \cdot [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]$

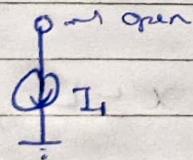
$$@ \text{Saturation: } I_D = \frac{1}{2} \text{ dep}(\cos \frac{W}{L}) (V_{GS} - V_{TH})^2$$



[Ideally here ID/V_{DS}
slope is zero]

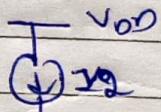
Note: With L assumed constant, a saturated MOSFET can be used as a current source connected b/w the drain & the source.

NMOS



current source injects
current into ground

PMOS



current source
draws current from VDS

'One terminal is open'

17) $E_{GSS} = 100 \mu A/V^2$, $V_{TH} = 0.5V$, $\frac{W}{L} = \frac{5 \mu m}{0.5 \mu m}$
 Design a 1mA current source.

$$I_{MA} = \frac{1}{2} (100 \mu A/V^2) \times 10 \times (V_{GS} - 0.5)^2$$

$$V_{GS} = 1.9V, V_{GS} - V_{TH} = (1.9 - 0.5) = 1.4V$$

If $V_{GS} + V_{DS} > V_{GS} - V_{TH}$, i.e., $V_{DS} > 1.4V$,
 Then only Transistor acts as current source

Ch. Secondary / Second-Order Effects

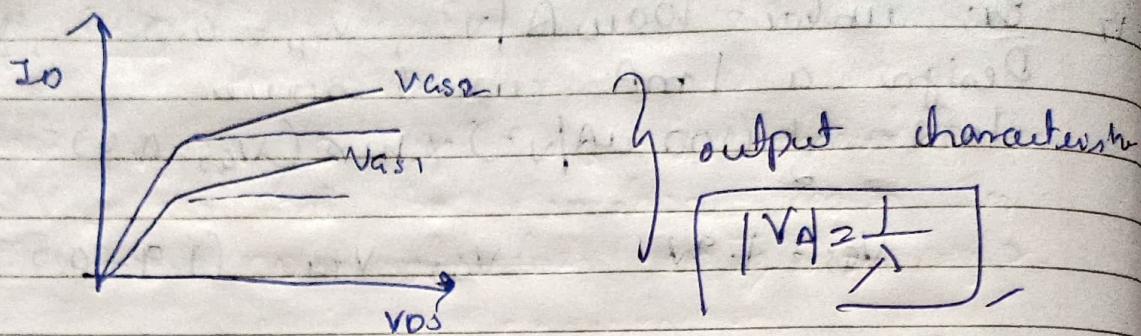
Channel-length modulation

- .) When pinch-off occurs in the channel, the length of the channel gradually decreases as the $V_{GS} \downarrow$ or $V_{DS} \downarrow$.
- .) The reduced length is denoted by L' , this is a function of V_{GS} .
- .) This effect is called channel length modulation.
- .) $L' = L - \Delta L$

$$I_D = \frac{1}{2} \text{ Unitor } \frac{W}{L} \left(V_{GS} - V_{TH} \right)^2 \left(1 + \lambda V_{DS} \right)$$

• λ = channel length modulation coefficient

- .) This phenomena introduces a non-zero slope in the I_D/V_{GS} curve & hence non-ideal current source b/w I_{DS} & V_{GS} in saturation.
- .) λ = relative variation in length for a given increment in V_{GS} .
- .) Thus, λ is smaller for longer channels.



Note: This is seen only in saturation & not in other regions because there is no pinch off & in triode region channel continuously stretches from source to drain.

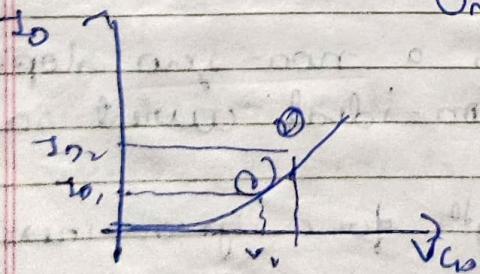
Note: Transconductance.

- A mos device "converts" a voltage to a current
- The change in the drain current divided by the change in gate-source voltage is called transconductance

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \quad |_{V_{DS} \text{ const}} \quad \therefore g_m = \frac{I_D}{V_{GS}/2}$$

gm = $\frac{W}{L} C_{GS} (V_{GS} - V_T)$

Unit $\frac{1}{A}$ → Siemens



- In saturation region, $g_m = \frac{1}{R_{DS}}$ in dep triode region

$$I_D = \frac{1}{2} I_{DSS} \cos \frac{w}{L} (V_{GS} - V_{TM})^2 \quad \text{when}$$

$$g_m = \text{current } \frac{W}{L} (V_{GS} - V_{TM})$$

$$\text{given } V_{th} \text{ and } V_{GS}$$

 $\frac{w}{L}$

constant

then $V_{GS} - V_{TM}$ constantso I_D constantso g_m constantso $\frac{w}{L}$ constant

$$g_m = \frac{1}{2} I_{DSS} \cos \frac{w}{L}$$

①

$$g_m = \frac{W}{L} (V_{GS} - V_{TM})$$

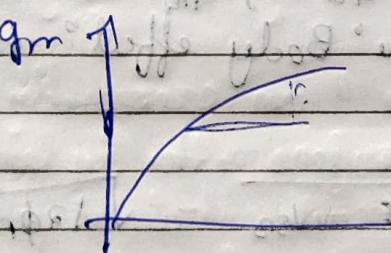
$$g_m = \frac{1}{2} I_{DSS} \cos \frac{w}{L}$$

②

$$g_m = \frac{W}{L} (V_{GS} - V_{TM}) \quad (\frac{w}{L} \text{ constant})$$

$$g_m = \frac{1}{2} I_{DSS} \quad (I_D \text{ constant})$$

$$g_m = I_D / (V_{GS} - V_{TM}) \quad (V_{GS} - V_{TM} \text{ constant})$$



ID

 $(\frac{w}{L} \text{ constant})$

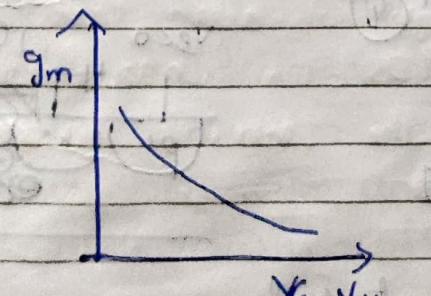
$$g_m = \frac{2 I_D}{V_{GS} - V_{TM}}$$

$$g_m = \frac{I_D}{V_{GS} - V_{TM}}$$

 $\frac{w}{L}$

constant

so

 $(I_D \text{ is constant})$ $V_N = 0 - 50 \text{ mV}$

(2)

Body Effect:-

- Suppose $V_S = V_D > 0$ and V_G is somewhat less than V_{TH} , so that the depletion region is formed but no-saturation inversion region exist
(i.e. $V_{SB} < 0$)
- As V_B becomes more -ve, more holes are attracted to the substrate connection, leaving a larger negative charge behind the depletion region becomes wider.
- WKT

$$V_{TH} = \Phi_{BS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}} \quad \text{--- (1)}$$

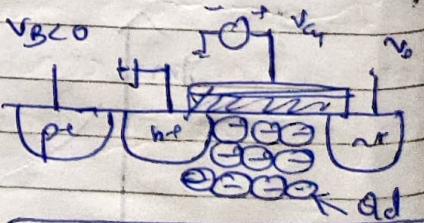
By above equation WKT $V_{TH} \propto Q_{dep}$; i.e. total charge in the depletion region because the gate charge must mirror Q_S before an inversion layer is formed.

- Thus as V_B drops $\propto Q_{dep}$, V_{TH} also \propto . This phenomenon is called the "Body effect" or the "Back-gate effect".

$$V_{TH} = V_{TH0} + \gamma (\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F})$$

V_{TH0} is given by eqn (1)

- $\gamma = \sqrt{2qE_s N_{Si}} / C_{ox}$
L. body effect co-efficient

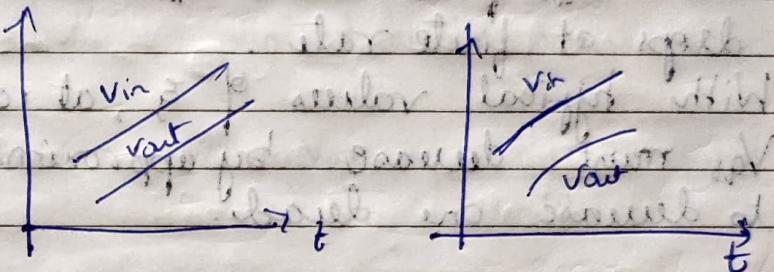


- V_{SB} is the source - bulk potential

- γ typically lies in the range $0.3 - 0.4 \text{ V}^{-1/2}$

- Body effect can be achieved with V_B is some voltage & not changing bulk potential because V_{TH} is dependent on V_{SB} not only on V_B .
- If V_{IN} & V_{OUT} is considered w/o body effect, V_{OUT} follows V_{IN} being drain current I_D remains constant

$$I_D = \frac{1}{2} \mu n C_o \frac{W}{L} (V_{IN} - V_{DSS} - V_{TH})^2$$



- If body effect is considered, V_{OUT} becomes more +ve, $V_{SB} \uparrow$, raising V_{IN} . So, in order to maintain constant I_D , $(V_{IN} - V_{OUT})$ must \uparrow

Note:- When V_{SB} becomes more negative i.e. when bulk voltage becomes more than V_S , V_{IN} falls below V_{TH0} . This can be used in low power voltage designs.

Sub-threshold conduction

- In our previous analysis, we have assumed that the device turns off abruptly as V_G drops below V_{TH} .
- In reality, for $V_G \approx V_{TH}$, a 'weak' inversion layer still exists & some current flows from D to S.
- Even for $V_G < V_{TH}$, I_D is finite, but it exhibits an

exponential dependence on V_{GS} . This is called "Subthreshold conduction", this effect can be formulated for V_{GS} greater than roughly W/V_t as $I_D = I_0 e^{\frac{V_{GS}}{W} - \frac{V_t}{kT/q}}$, where $I_0 \propto \frac{W}{L}$, $\frac{kT}{q} \approx 25mV$ is an nonideality factor & $V_t = kT/q$.

- .) We also say the device operates in "weak inversion".
- .) When V_{GS} falls below V_{TH} , the drain current drops at finite rate.
- .) With typical values of ξ , at room temperature V_{GS} must decrease by approximately $80mV$ to decrease one decade.

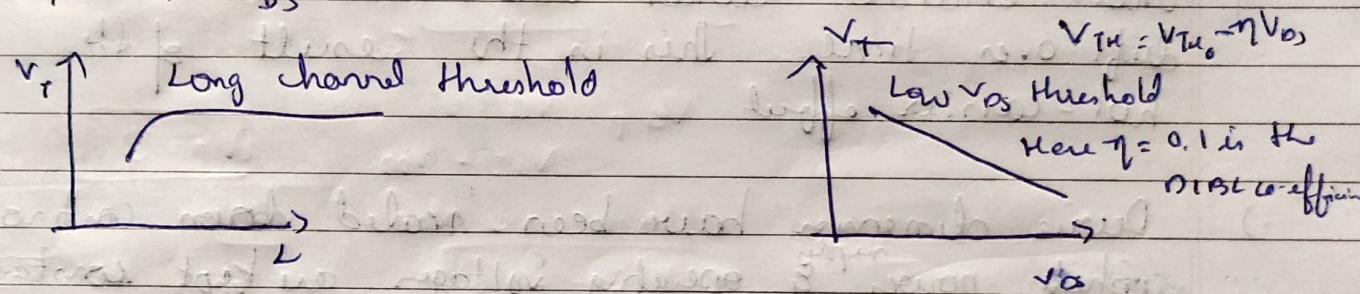
4) Voltage limitations:-

- .) In a MOSFET, at high gate-source voltage, the gate oxide breaks down irreversibly damaging the transistor.
- .) In short-channel device, an excessively large drain-source voltage widens the depletion region around the drain so much that it touches that around the source, creating a very large drain current. This effect is called Punchthrough.
- .) Even w/o breakdown, MOSFET's characteristics can change permanently if the terminal voltage difference exceeds a specified value.

Threshold Variations and DIBL

$$V_T = V_{T0} + \gamma (\sqrt{2\phi_F + V_{SB}}) - \sqrt{2\phi_F}$$

Threshold is a function of the manufacturing technology & the applied body bias. As the device dimensions are reduced this model becomes inaccurate, & the threshold potential becomes a func' of L, W & V_{DS}.



- a) Threshold as a func' of the length (for low V_{DS})
- b) Drain-induced barrier lowering

- .) Threshold decrease with $\uparrow V_{DS}$. This is called drain-induced barrier lowering, causes the threshold potential to be a func' of the operating voltages.
- .) For high enough values of the drain voltage, the source-drain voltage, the source & drain region can even be shorted together & normal transistor operation ceases to exist. The sharp T is current due to this effect
- .) Based is called Punch through.

Narrow channel Effect:

-) This effect is a phenomenon observed in MOSFET when the channel width becomes very small. This affects the V_{th} .

Hot - carrier effect

-) Short channel devices also have the tendency to drift over time. This is the result of the hot-carrier effect.
-) Device dimension have been scaled down continuously while power & operating voltages are kept constant.
-) The resulting increase in the electrical field strength causes an increasing velocity of the electron, which can leave the device.
-) As gate voltage \uparrow , the electrons of the inversion region goes into the dielectric of the p-silicon, this inturn increases the V_{th} . This effect is called Hot - carrier effect.
-) $V_{th} \uparrow \rightarrow$ for nmos
 $V_{th} \downarrow \rightarrow$ for pmos { why }

.) NMOS Inverter

.) Resistive Load Inverter

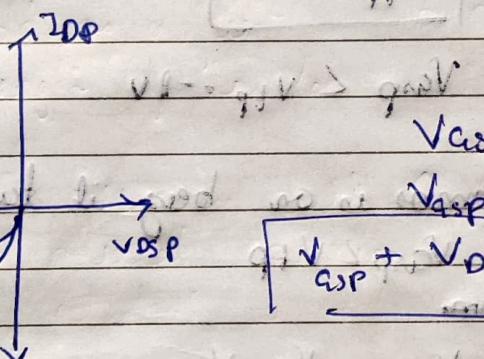
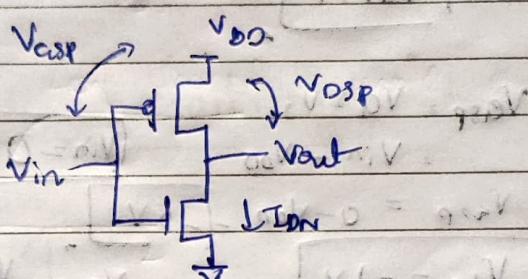
CMOS Inverters

Goal: Combine I_{on} and I_{off} in one graph

$$\text{Kirchhoff's } V_{in} = V_{DD} + V_{GSP}$$

$$I_{on} = -I_{off}$$

$$V_{out} = V_{DD} + V_{DP}$$



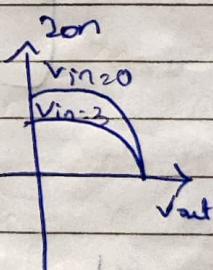
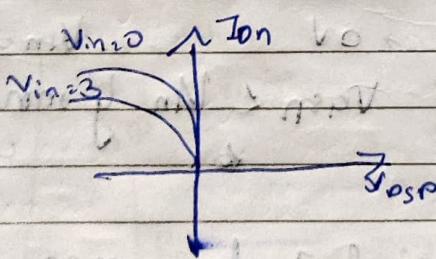
$$V_{GSP} = V_G - V_S$$

$$V_{GSP} = V_{in} - V_{DD}$$

$$V_{GSP} + V_{DD} = V_{in}$$

$$\text{Assume } V_{DD} = 5V$$

negative of
both others



complement of C logical = not

$$I_{on} = -I_{off}$$

$$V_{in} = V_{DD} + V_{GSP}$$

$$V_{in} = 5 - 2 \times 3$$

$$= +5 - 5 = 0$$

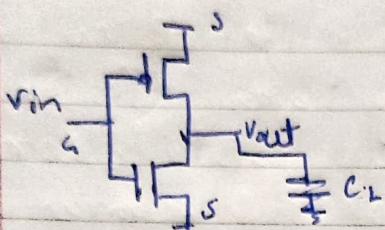
$$V_{GSP} = V_G - V_S$$

$$V_{out} = V_{GSP} + V_{DD}$$

$$V_{out} = V_{GSP} + V_{DD}$$

Castree
more addition
VDD to VGS
no graph is
shifted to
right

For nmos, the graph remains same because
 $V_{OS} = V_{out}$ b/c as $V_s = 0$, source is grounded
 V_{DS}, V_{IN} are not enough to turn on the mosfet



$$V_{DS(on)} = V_G - V_S, \text{ at } V = V_{IN} = 0 \text{ V}$$

$$V_{DS} = V_D - V_S = 0 - 0 = 0 \text{ V}$$

$$V_{DS} = V_D$$

$$V_{DS} = 0 \rightarrow V_{DS} = 0$$

$$V_{GSP} = V_G - V_S$$

$$= V_{IN} - V_{DD}$$

$$V_{IN} = 0 \text{ V}$$

$$V_{GSP} = 0 - V_{DD} = -5 \text{ V}$$

$$V_{TP} = -1 \text{ V}$$

$$V_{GSP} = V_D - V_S = V_{out} - 0$$

$$V_{IN} = 0 \text{ V}$$

$$V_{GSP} < V_{TP} = -1 \text{ V}$$

$$V_{out} = 5 \text{ V} \rightarrow \text{Pins out of capacity}$$

pmos is on bcz it turns on when $V_{GSP} > V_{TP}$

$$V_{GSP} > V_{TP}$$

$$V_{DS(on)} = V_G - V_S$$

$$= V_{IN} - 0$$

$$= 0 - 0$$

$$= 0 \text{ V}$$

$$V_{IN} = 1 \text{ V}$$

$V_{DS(on)} < V_{IN}$ b/c pmos is in cutoff

Here, V_{out} is logical 1 for pmos

Beta Ratio Effects

$$r = \frac{\beta_r}{\beta_n}$$

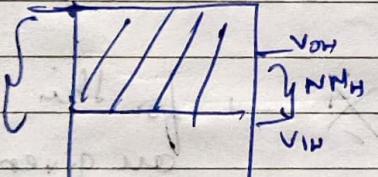
If $r > 1 \rightarrow$ Hi-skewed, $r < 1 \rightarrow$ low, lo-skewed,
 $r = 1 \rightarrow$ normal skewed

Note: $V_{in} = V_{ob} + V_{tp} + V_{tn} \sqrt{1 - \frac{1}{r}}$

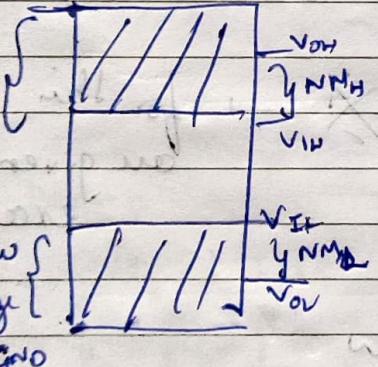
\rightarrow V_{tp} should be taken -ve while calculation

Noise Margin

logical
High
I/p
range

V_{OH}

logical low
I/p range

V_{OL}V_{OH} maxV_{OL} minV_{OH} minV_{OL} maxV_{OL} minV_{OL} max

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{NH}$$

V_{IH} : minimum high i/p voltage

V_{IL} : max low i/p voltage

V_{OL} : min high o/p voltage

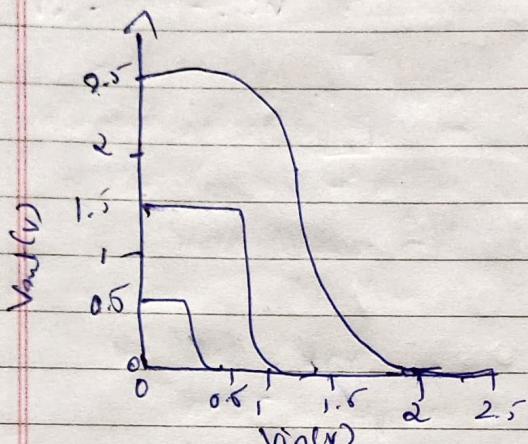
V_{OL} : max low o/p voltage

H.W

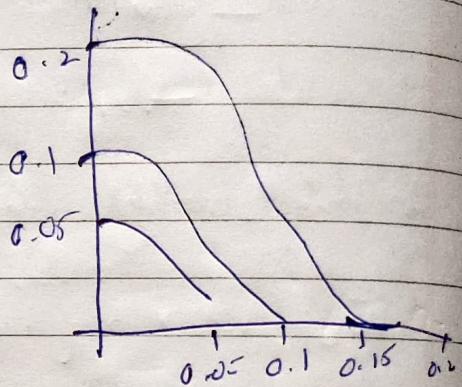
MOS capacitance (soft study) \rightarrow Capacitance with MOS device

Note Eq: 5.11 in Rabe - Scaling

Scaling the Supply Voltage



a) Reducing



- a) Reducing the VDD voltage \rightarrow gain is improved
(For ideal \rightarrow gain will be ∞)
- b) VDD voltage is reduced to 200mV, 100mV & 50mV, keeping \sqrt{I} constant.
- c) At VDD voltage which is not even large enough to turn on the transistors. Due to subthreshold conduction, switching current requires a very slow operation.
Application: In watches
- d) For other digital circuits, to \uparrow the supply voltage scaling should be applied
- e) The supply voltage should be minimum at least a couple time of $QF = kT/q$, thermal voltage