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INPUT FILES FOR PHYSICAL DESIGN

1. Netlist (Verilog/VHDL .v)

1. **Hierarchy**: Module definitions and instantiations, representing the circuit structure.
2. **Logic Gates/Cells**: List of standard cells, macros, and flip-flops used.
3. **Connectivity**: Net connections between pins/ports of cells.
4. **Ports**: Input/output ports for top-level module.
5. **Parameters**: Optional configuration parameters.
6. **Comments**: Functional description.

2. Standard Cell Library (.lib, Liberty Format)

7. **Cell List**: Names and types of all cells (AND, OR, DFF, etc.).
8. **Pin Information:** Pin names, direction (input/output), capacitance.
9. **Timing Information:**
   1. Delay tables: NLDM or CCS tables indexed by input slew and output load.
10. **Setup/Hold times:** For flip-flops/latches.
11. **Transition time:** Output transition for given input conditions.
12. **Power Data**: Dynamic and leakage power, per transition or condition.
13. **Functionality:** Boolean logic expression for each cell.
14. **Cell Area:** Physical area used by each cell.
15. **Related pins:** Pin-to-pin relationships for timing.
16. **Operating conditions:** PVT (Process, Voltage, Temperature) corners.
17. **Current source data**: (For CCS/ECSM) Current waveform data for timing.

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3. LEF (Library Exchange Format)

Cell Abstracts:

Macro definitions: Cell size, height, width, orientation.

Pin locations: X/Y coordinates for each pin.

Obstructions/Blockages: Metal blockages, keep-out regions.

Tech Layer Info:

Metal layers: Layer names, width, spacing, pitch.

Via definitions: Via types, size, and location.

Routing Rules: Preferred directions, minimum spacing.

Site definitions: Default cell site and row information.

Non-timing information: LEF does not include timing, only geometry and rules.

4. DEF (Design Exchange Format)

Component Placement:

Cell/macro instance names: and their locations, orientations.

Net Routing: Routing paths for each net (metal layers, segment coordinates).

Pin Placement: Locations of IO pins on the die.

Special Nets: Power/ground net routing (VDD, VSS).

Floorplan Information:

Core/Die area: Size, origin, boundaries.

Rows/Tracks: Placement rows for standard cells.

Blockages: Locations of placement/routing blockages.

Groups/Regions: Logical regions for constraints (e.g., voltage domains).

Design version/history: Metadata for version tracking.

5. SDC (Synopsys Design Constraints)

Clocks: Name, period, waveform, source.

Input/Output Delay: Timing requirements on primary inputs/outputs.

Timing Exceptions:

False paths: Paths to be ignored in timing analysis.

Multi-cycle paths: Paths taking more than one clock cycle.

Case Analysis: Constant values for specific signals during timing.

Generated Clocks: Derived clocks from primary clocks.

Max/Min Delay: Specific timing constraints for paths.

Load/Drive Constraints: Load capacitance and drive strength for pins.

6. Floorplan and Physical Constraints

Macro Placement: X/Y locations, orientation, rotation for hard macros.

Keep-out Regions: Forbidden zones for placement or routing.

IO Placement: Location of IO cells/pads on chip edges.

Power Domains: Definition and Location of Voltage Islands.

Partitioning: Region definitions for hierarchical blocks.

Pin Constraints: Fixed/flexible pin locations and order.

7. Technology Files (Tech LEF, Rule Files)

Layers: Metal, polysilicon, diffusion layer definitions.

Design Rules:

DRC: Minimum width, spacing, area, enclosure, and overlap rules.

LVS: Rules for layout vs schematic checking.

Via Definitions: Allowed via types and locations.

Process Corners: Variations for PVT analysis.

Antenna/EM Rules: Rules for antenna effect, electromigration.

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8. Power Intent Files (UPF/CPF)

Power Domains: Definition of multiple voltage regions.

Power Switches: Switches for disconnecting domains.

Level Shifters: Placement and connection info for voltage boundary crossing.

Isolation Cells: Placement for data retention/isolation.

Retention Logic: Data retention cells for low-power modes.

Power States: Allowed power modes for different regions.

9. Others (ECO files, Antenna files, etc.)

ECO Files: Changes to netlist or placement after initial implementation.

Antenna Files: Data for antenna rule violations and fixes.

Test Constraints: Scan chain info, test point placement.

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