VLSI

Digital Electronics Interview Questions and Answers

• MALAVIYA NATIONAL INSTITUTE OF TECHNOLOGY JAIPUR •

मालवीय राष्ट्रीय प्रौद्योगिकी संस्थान जयपुर

योगः कर्मसु कौशलम्

By

Nagaraju Ramavath

Design Verification Engineer

Q1: What is a Digital System?

A1: A digital system is a system that processes discrete or binary signals (0s and 1s) rather than continuous analog signals.

Q2: What is meant by a Bit?

A2: A bit is the smallest unit of data in a digital system and represents a binary digit, either 0 or 1.

Q3: Define Radix.

A3: Radix, also known as the base of a number system, refers to the total number of unique symbols (including zero) used to represent numbers in that system.

For example, the radix of the binary system is 2, as it uses symbols 0 and 1.

Q4: Give an example of a digital system.

A4: A digital computer is a classic and widely used example of a digital system.

Q5: Define Nibble and Byte.

A5:

- A Nibble is a group of 4 bits.
- A Byte is a group of 8 bits**.**

Q6: What are the different number systems?

A6: The commonly used number systems in digital electronics are:

1. Decimal Number System (Base 10)
2. Binary Number System (Base 2)
3. Octal Number System (Base 8)
4. Hexadecimal Number System (Base 16)

Q7: What is Binary Logic?

A7: Binary logic uses binary variables that take only two values: 0 and 1. It involves three fundamental logical operations:

- AND

- OR
- NOT

  Variables are typically represented by symbols like A, B, C, x, y, z, etc**.**

Q8: What are the basic digital logic gates?

A8: The three fundamental digital logic gates are:

1. AND Gate
2. OR Gate
3. NOT Gate

Let me know if you want diagram support or want to extend this with universal gates

(NAND, NOR) or truth tables

Ques 9: How to represent a positive and negative sign in computers? Ans

9: Positive and negative sign in computers is represented as follows.

1. Positive (+) sign by 0
2. Negative (-) sign by 1

Ques 10: Define Boolean algebra & Boolean Expression.

Ans10: System of algebra that operates on Boolean variables. The binary nature of Boolean algebra makes it useful for analysis, simplification and design of logic circuits

Ques 11: What are basic properties of Boolean algebra?

Ans 11: A system of algebra that operates on Boolean variables. The binary nature of Boolean algebra makes it useful for analysis, simplification and design of logic circuits.

Ques 12: State the commutative property of Boolean algebra?

Ans 12: The commutative property states that the order in which the variables are OR & makes no difference. The commutative property is

1. A+B=B+A
2. AB = BA

Ques 13: Define Cell.

Ans: 13: The smallest unit of a karnaugh map, corresponding to one rows of a truth table. The input variables are the cells coordinates and the output variable is the cells contents.

Ques 14: What are the applications of octal number system?

Ans 14: The applications of octal number system are

1. It is used for entering the binary data and displaying certain information’s.
2. It is very important for the efficient use of microprocessors and other digitalcircuits

Ques 15: What is an essential prime implicant?

Ans 15 : The Essential Prime Implicant is a prime implicant in which one or more mintermsare unique, it contains at least one minterm which is not contained in any other primeimplicant.

1. **Question 1. What Is Difference Between Latch And Flip-flop?**

   Answer :

   The main difference between latch and FF is that latches are level sensitive while FF is edge sensitive. They both require the use of clock signal and are used in sequential logic. For a latch, the output tracks the input when the clock signal is high, so as long as the clock is logic 1, the output can change if the input also changes.

   FF on the other hand, will store the input only when there is a rising/falling edge of the clock. Latch is sensitive to glitches on enable pin, whereas flip-flop is immune to glitches. Latches take fewer gates (also less power) to implement than flip-flops. Latches are faster than flip-flops

2. **Question 2. Given Only Two Xor Gates One Must Function As Buffer And Another As Inverter?**

   Answer :

   Tie one of xor gates input to 1 it will act as inverter.
   Tie one of xor gates input to 0 it will act as buffer.

3. **Question 3. Difference Between Mealy And Moore State Machine?**

   Answer :

   A) Mealy and Moore models are the basic models of state machines. A state machine which uses only Entry Actions, so that its output depends on the state, is called a Moore model. A state machine which uses only Input Actions, so that the output depends on the state and also on inputs, is called a Mealy model. The models selected will influence a design but there are no general indications as to which model is better. Choice of a model depends on the application, execution means (for instance, hardware systems are usually best realized as Moore models) and personal preferences of a designer or programmer
   B) Mealy machine has outputs that depend on the state and input (thus, the FSM has the output written on edges) Moore machine has outputs that depend on state only (thus, the FSM has the output written in the state itself.

   Advantage and Disadvantage

   •In Mealy as the output variable is a function both input and state, changes of state of the state variables will be delayed with respect to changes of signal level in the input variables, there are possibilities of glitches appearing in the output variables.

   •Moore overcomes glitches as output dependent on only states and not the input signal level.
   •All of the concepts can be applied to Moore-model state machines because any Moore state machine can be implemented as a Mealy state machine, although the converse is not true.
   •Moore machine: the outputs are properties of states themselves... which means that you get the output after the machine reaches a particular state, or to get some output your machine has to be taken to a state which provides you the output. The outputs are held until you go to some other state Mealy machine:
   •Mealy machines give you outputs instantly, that is immediately upon receiving input, but the output is not held after that clock cycle.

4. **Question 4. Difference Between One Hot And Binary Encoding?**

   Answer :

   Common classifications used to describe the state encoding of an FSM are Binary (or highly encoded) and One hot.

A binary-encoded FSM design only requires as many flip-flops as are needed to uniquely encode the number of states in the state machine. The actual number of flip-flops required is equal to the ceiling of the log-base-2 of the number of states in the FSM.A one hot FSM design requires a flip-flop for each state in the design and only one flip-flop (the flip-flop representing the current or "hot" state) is set at a time in a one hot FSM design.

For a state machine with 9- 16 states, a binary FSM only requires 4 flip-flops while a one hot FSM requires a flip-flop for each state in the design FPGA vendors frequently recommend using a one hot state encoding style because flip-flops are plentiful in an FPGA and the combinational logic required to implement a one hot FSM design is typically smaller than most binary encoding styles.

Since FPGA performance is typically related to the combinational logic size of the FPGA design, one hot FSMs typically run faster than a binary encoded FSM with larger combinational logic blocks

5. **Question 5. How To Achieve 180 Degree Exact Phase Shift?**
Answer :
Never tell using inverter
a) DCM an inbuilt resource in most of FPGA can be configured to get 180 degree phase shift.
b) BUFGDS that is differential signaling buffers which are also inbuilt resource of most of FPGA can be used.
6. **Question 6. What Is Significance Of Ras And Cas In Sdram?**
Answer :
SDRAM receives its address command in two address words. It uses a multiplex scheme to save input pins. The first address word is latched into the DRAM chip with the row address strobe (RAS).

Following the RAS command is the column address strobe (CAS) for latching the second address word. Shortly after the RAS and CAS strobes, the stored data is valid for reading.
7. **Question 7. Tell Some Of Applications Of Buffer?**
Answer :
a) They are used to introduce small delays.
b) They are used to eliminate cross talk caused due to inter electrode capacitance due to close routing.
c) They are used to support high fan-out, e.g.: bufg
8. **Question 8. Give Two Ways Of Converting A Two Input Nand Gate To An Inverter?**
Answer :
a) Short the 2 inputs of the nand gate and apply the single input to it.
b) Connect the output to one of the input and the other to the input signal.
9. **Question 9. Why Is Most Interrupts Active Low?**
Answer :
This answers why most signals are active low if you consider the transistor level of a module, active low means the capacitor in the output terminal gets charged or discharged based on low to high and high to low transition respectively. When it goes from high to low it depends on the pull down resistor that pulls it down and it is relatively easy for the output capacitance to discharge rather than charging. Hence people prefer using active low signals.
10. **Question 10. Design A Four-input Nand Gate Using Only Two-input Nand Gates.**
Answer :

Basically, you can tie the inputs of a NAND gate together to get an inverter.

11. **Question 11. What Will Happen If Contents Of Register Are Shifter Left, Right?**
    Answer :
    It is well known that in left shift all bits will be shifted left and LSB will be appended with 0 and in right shift all bits will be shifted right and MSB will be appended with 0 this is a straightforward answer What is expected is in a left shift value gets Multiplied by 2
    e.g.: consider 0000_1110=14 a left shift will make it 0001_110=28, it the same fashion right shift will Divide the value by 2.
12. **Question 12. Given The Following Fifo And Rules, How Deep Does The Fifo Need To Be To Prevent Underflow Or Overflow?**
    Answer :
    RULES:

    1) frequency(clk_A) = frequency(clk_B) / 4
    2) period(en_B) = period(clk_A) * 100
    3) duty cycle(en_B) = 25%
    Assume clk_B = 100MHz (10ns)
    From (1), clk_A = 25MHz (40ns)
    From (2), period(en_B) = 40ns * 400 = 4000ns, but we only output for 1000ns,due to (3), so 3000ns of the enable we are doing no output work. Therefore, FIFO size = 3000ns/40ns = 75 entries
13. **Question 13. Differences Between D-latch And D Flip-flop?**
    Answer :
    D-latch is level sensitive where as flip-flop is edge sensitive. Flip-flops are made up of latches.
14. **Question 14. What Is A Multiplexer?**
    Answer :
    Is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line.

    (2n =>n). Where n is selection line.
15. **Question 15. What Are Set Up Time & Hold Time Constraints? What Do They Signify? Which One Is Critical For Estimating Maximum Clock Frequency Of A Circuit?**
    Answer :
    Set up time is the amount of time the data should be stable before the application of the clock signal, where as the hold time is the amount of time the data should be stable after the application of the clock. Setup time signifies maximum delay constraints; hold time is for minimum delay constraints. Setup time is critical for establishing the maximum clock frequency.
16. **Question 16. How Can You Convert An Sr Flip-flop To A Jk Flip-flop?**
    Answer :
    By giving the feedback we can convert, i.e. !Q=>S and Q=>R.Hence the S and R inputs will act as J and K respectively.
17. **Question 17. How Can You Convert The Jk Flip-flop To A D Flip-flop?**
    Answer :
    By connecting the J input to the K through the inverter.

18. **Question 18. How Do You Detect If Two 8-bit Signals Are Same?**
    Answer :
    XOR each bits of A with B (for e.g. A [0] xor B [0]) and so on. The o/p of 8 xor gates is then given as i/p to an 8-i/p nor gate.

    if o/p is 1 then A=B.
19. **Question 19. Convert D-ff Into Divide By 2. (not Latch) What Is The Max Clock Frequency The Circuit Can Handle, Given The Following Information?**
    Answer :
    T_setup= 6nsT_hold = 2nS T_propagation = 10nS

    Circuit: Connect Qbar to D and apply the clk at clk of DFF and take the O/P at Q. It gives freq/2. Max. Freq of operation: 1/ (propagation delay+setup time) = 1/16ns = 62.5 MHz
20. **Question 20. 7 Bit Ring Counter's Initial State Is 0100010. After How Many Clock Cycles Will It Return To The Initial State?**
    Answer :
    6 cycles
21. **Question 21. Design All The Gates (not, And, Or, Nand, Nor, Xor, Xnor) Using 2:1 Multiplexer?**
    Answer :
    Using 2:1 Mux, (2 inputs, 1 output and a select line)
    a) NOT :Give the input at the select line and connect I0 to 1 & I1 to 0. So if A is 1, we will get I1 that is 0 at the O/P.
    b) AND: Give input A at the select line and 0 to I0 and B to I1. O/p is A & B
    c) OR: Give input A at the select line and 1 to I1 and B to I0. O/p will be A | B
    d) NAND: AND + NOT implementations together
    e) NOR: OR + NOT implementations together
    f) XOR: A at the select line B at I0 and ~B at I1. ~B can be obtained from (a)
    g) XNOR: A at the select line B at I1 and ~B at I0
22. **Question 22. Design A Circuit That Calculates The Square Of A Number?**
    Answer :
    It should not use any multiplier circuits. It should use Multiplexers and other logic?

    1^2=0+1=1
    2^2=1+3=4
    3^2=4+5=9
    4^2=9+7=16
    5^2=16+9=25
    See a pattern yet? To get the next square, all you have to do is add the next odd number to the previous square that you found. See how 1,3,5,7 and finally 9 are added. Wouldn’t this be a possible solution to your question since it only will use a counter, multiplexer and a couple of adders? It seems it would take n clock cycles to calculate square of n.
23. **Question 23. N Number Of Xnor Gates Is Connected In Series Such That The N Inputs (a0, A1, A2.....) Are Given In The Following Way: A0 & A1 To First Xnor Gate And A2 & O/p Of First Xnor To Second Xnor Gate And So On..... Nth Xnor Gates Output Is Final Output. How Does This Circuit Work? Explain In Detail?**
    Answer :

If N=Odd, the circuit acts as even parity detector, i.e. the output will 1 if there are even number of 1's in the N input...This could also be called as odd parity generator since with this additional 1 as output the total number of 1's will be ODD. If N=Even, just the opposite, it will be Odd parity detector or Even Parity Generator.

24. **Question 24. What Is Race-around Problem? How Can You Rectify It?**
    Answer :
    The clock pulse that remains in the 1 state while both J and K are equal to 1 will cause the output to complement again and repeat complementing until the pulse goes back to 0, this is called the race around problem. To avoid this undesirable operation, the clock pulse must have a time duration that is shorter than the propagation delay time of the F-F, this is restrictive so the alternative is master-slave or edge-triggered construction.
25. **Question 25. An Assembly Line Has 3 Fail Safe Sensors And One Emergency Shutdown Switch. The Line Should Keep Moving Unless Any Of The Following Conditions Arise:**
    Answer :
    (i) If the emergency switch is pressed
    (ii) If the senor1 and sensor2 are activated at the same time.
    (iii) If sensor 2 and sensor3 are activated at the same time.
    (iv) If all the sensors are activated at the same time
    suppose a combinational circuit for above case is to be implemented only with NAND Gates. How many minimum number of 2 input NAND gates are required?

    No of 2-input NAND Gates required = 6 you can try the whole implementation.
26. **Question 26. How Will You Implement A Full Subtractor From A Full Adder?**
    Answer :
    All the bits of subtrahend should be connected to the xor gate. Other input to the xor being one. The input carry bit to the full adder should be made 1. Then the full adder works like a full subtract.
27. **Question 27. What Is Difference Between Setup And Hold Time. The Interviewer Was Looking For One Specific Reason, And Its Really A Good Answer Too..the Hint Is Hold Time Doesn't Depend On Clock, Why Is It So...?**
    Answer :
    Setup violations are related to two edges of clock, i mean you can vary the clock frequency to correct setup violation. But for hold time, you are only concerned with one edge and do not basically depend on clock frequency.
28. **Question 28. In A 3-bit Johnson's Counter What Are The Unused States?**
    Answer :
    2(power n)-2n is the one used to find the unused states in Johnson counter.

    So for a 3-bit counter it is 8-6=2.Unused states=2. the two unused states are 010 and 101.
29. **Question 29. What Is Difference Between Ram And Fifo?**
    Answer :
    FIFO does not have address lines

    Ram is used for storage purpose where as FIFO is used for synchronization purpose i.e. when two peripherals are working in different clock domains then we will go for FIFO.
30. **Question 30. Consider Two Similar Processors, One With A Clock Skew Of 100ps And Other With A Clock Skew Of 50ps. Which One Is Likely To Have More Power? Why?**

Answer :

Clock skew of 50ps is more likely to have clock power. This is because it is likely that low-skew processor has better designed clock tree with more powerful and number of buffers and overheads to make skew better.

31. **Question 31. Is It Possible To Reduce Clock Skew To Zero? Explain Your Answer?**

    Answer :

    Even though there are clock layout strategies (H-tree) that can in theory reduce clock skew to zero by having the same path length from each flip-flop from the pll, process variations in R and C across the chip will cause clock skew as well as a pure H-Tree scheme is not practical (consumes too much area).

32. **Question 32. The Circle Can Rotate Clockwise And Back. Use Minimum Hardware To Build A Circuit To Indicate The Direction Of Rotating?**

    Answer :

    2 sensors are required to find out the direction of rotating. They are placed like at the drawing. One of the m is connected to the data input of D flip-flop, and a second one - to the clock input. If the circle rotates the way clock sensor sees the light first while D input (second sensor) is zero - the output of the flip-flop equals zero, and if D input sensor "fires" first - the output of the flip-flop becomes high.

33. **Question 33. You Have Two Counters Counting Upto 16, Built From Negedge Dff , First Circuit Is Synchronous And Second Is "ripple" (cascading), Which Circuit Has A Less Propagation Delay? Why?**

    Answer :

    The synchronous counter will have lesser delay as the input to each flop is readily available before the clock edge. Whereas the cascade counter will take long time as the output of one flop is used as clock to the other. So the delay will be propagating. For E.g.: 16 state counter = 4 bit counter = 4 Flip flops Let 10ns be the delay of each flop The worst case delay of ripple counter = 10 * 4 = 40ns The delay of synchronous counter = 10ns only.(Delay of 1 flop)

34. **Question 34. Difference Between Synchronous And Asynchronous Reset?**

    Answer :

    Synchronous reset logic will synthesize to smaller flip-flops, particularly if the reset is gated with the logic generating the dinput. But in such a case, the combinational logic gate count grows, so the overall gate count savings may not be that significant. The clock works as a filter for small reset glitches; however, if these glitches occur near the active clock edge, the Flip-flop could go metastable. In some designs, the reset must be generated by a set of internal conditions. A synchronous reset is recommended for these types of designs because it will filter the logic equation glitches between clocks.

    Disadvantages of synchronous reset:

    Problem with synchronous resets is that the synthesis tool cannot easily distinguish the reset signal from any other data signal. Synchronous resets may need a pulse stretcher to guarantee a reset pulse width wide enough to ensure reset is present during an active edge of the clock. if you have a gated clock to save power, the clock may be disabled coincident with the assertion of reset. Only an asynchronous reset will work in this situation, as the reset might be removed prior to the resumption of the clock. Designs that are pushing the limit for data path timing, cannot afford to have added gates and additional net delays in the data path due to logic inserted to handle synchronous resets.

Asynchronous reset:
The biggest problem with asynchronous resets is the reset release, also called reset removal. Using an asynchronous reset, the designer is guaranteed not to have the reset added to the data path. Another advantage favoring asynchronous resets is that the circuit can be reset with or without a clock present.

Disadvantages of asynchronous reset: ensure that the release of the reset can occur within one clock period. if the release of the reset occurred on or near a clock edge such that the flip-flops went metastable.

35. **Question 35. Implement The Following Circuits:**
Answer :
(a) 3 input NAND gate using min no of 2 input NAND Gates
(b) 3 input NOR gate using min no of 2 input NOR Gates
(c) 3 input XNOR gate using min no of 2 input XNOR Gates
Assuming 3 inputs A,B,C?
3 input NAND Connect:
a) A and B to the first NAND gate
b) Output of first Nand gate is given to the two inputs of the second NAND gate (this basically realizes the inverter functionality)4
c) Output of second NAND gate is given to the input of the third NAND gate, whose other input is C ((A NAND B) NAND (A NAND B)) NAND C Thus, can be implemented using '3' 2-input NAND gates. I guess this is the minimum number of gates that need to be used.

1. **Question 1. Explain About Setup Time And Hold Time, What Will Happen If There Is Setup Time And Hold Tine Violation, How To Overcome This?**
   Answer :
   Set up time is the amount of time before the clock edge that the input signal needs to be stable to guarantee it is accepted properly on the clock edge.

   Hold time is the amount of time after the clock edge that same input signal has to be held before changing it to make sure it is sensed properly at the clock edge.

   Whenever there are setup and hold time violations in any flipflop, it enters a state where its output is unpredictable: this state is known as metastable state (quasi stable state)Í¾ at the end of metastable state, the flipflop settles down to either '1' or '0'. This whole process is known as metastability.
2. **Question 2. What Is Skew, What Are Problems Associated With It And How To Minimize It?**
   Answer :
   In circuit design, clock skew is a phenomenon in synchronous circuits in which the clock signal (sent from the clock circuit) arrives at different components at different times.

   This is typically due to two causes. The first is a material flaw, which causes a signal to travel faster or slower than expected. The second is distance: if the signal has to travel the entire length of a circuit, it will likely (depending on the circuit's size) arrive at different parts of the circuit at different times. Clock skew can cause harm in two ways. Suppose that a logic path travels through combinational logic from a source flipflop to a destination flipflop. If the destination flipflop receives the clock tick later than the source flipflop, and if the logic path delay is short enough, then the data signal might arrive at the destination flipflop before the clock tick, destroying there the previous data that should have been clocked through. This is called a hold violation because the previous data is not held long enough at the destination flipflop to be properly clocked through. If the destination flipflop receives the clock tick earlier than the source flipflop, then the data signal has that much less time to reach the destination flipflop before the next clock tick. If it fails to do so, a setup violation occurs, socalled because the new data was not set up and stable before the next clock tick arrived. A hold violation is more serious than a setup violation because it cannot be fixed by increasing the clock period.

   Clock skew, if done right, can also benefit a circuit. It can be intentionally introduced to decrease the clock period at which the circuit will operate correctly, and/or to increase the setup or hold safety margins. The optimal set of clock delays is determined by a linear program, in which a setup and a hold constraint appears for each logic path. In this linear program, zero clock skew is merely a feasible point.

   Clock skew can be minimized by proper routing of clock signal (clock distribution tree) or putting variable delay buffer so that all clock inputs arrive at the same time.
3. **Question 3. What Is Slack?**
   Answer :
   'Slack' is the amount of time you have that is measured from when an event 'actually happens' and when it 'must happen'.. The term 'actually happens' can also be taken as being a predicted time for when the event will 'actually happen'.

When something ‘must happen’ can also be called a ‘deadline’ so another definition of slack would be the time from when something ‘actually happens’ (call this Tact) until the deadline (call this Tdead).

Slack = Tdead – Tact.

Negative slack implies that the ‘actually happen’ time is later than the ‘deadline’ time…in other words it’s too late and a timing violation….you have a timing problem that needs some attention.

4. **Question 4. What Is Glitch? What Causes It (explain With Waveform)? How To Overcome It?**
   Answer :
   The following figure shows a synchronous alternative to the gated clock using a data path. The flipflop is clocked at every clock cycle and the data path is controlled by an enable. When the enable is Low, the multiplexer feeds the output of the register back on itself. When the enable is High, new data is fed to the flipflop and the register changes its state.
5. **Question 5. Given Only Two Xor Gates One Must Function As Buffer And Another As Inverter?**
   Answer :
   - Tie one of xor gates input to 1 it will act as inverter.
   - Tie one of xor gates input to 0 it will act as buffer.
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7. **Question 7. Difference Between Heap And Stack?**
   Answer :
   The Stack is more or less responsible for keeping track of what’s executing in our code (or what’s been “called”). The Heap is more or less responsible for keeping track of our objects (our data, well… most of it – we’ll get to that later.).

   Think of the Stack as a series of boxes stacked one on top of the next. We keep track of what’s going on in our application by stacking another box on top every time we call a method (called a Frame). We can only use what’s in the top box on the stack. When we’re done with the top box (the method is done executing) we throw it away and proceed to use the stuff in the previous box on the top of the stack. The Heap is similar except that its purpose is to hold information (not keep track of execution most of the time) so anything in our Heap can be accessed at any time. With the Heap, there are no constraints as to what can be accessed like in the stack. The Heap is like the heap of clean laundry on our bed that we have not taken the time to put away yet – we can grab what we need quickly. The Stack is like the stack of shoe boxes in the closet where we have to take off the top one to get to the one underneath it.
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   Answer :

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A onehot FSM design requires a flipflop for each state in the design and only one flipflop (the flipflop representing the current or “hot” state) is set at a time in a one hot FSM design. For a state machine with 916 states, a binary FSM only requires 4 flipflops while a onehot FSM requires a flipflop for each state in the design FPGA vendors frequently recommend using a onehot state encoding style because flipflops are plentiful in an FPGA and the combinational logic required to implement a onehot FSM design is typically smaller than most binary encoding styles. Since FPGA performance is typically related to the combinational logic size of the FPGA design, onehot FSMs typically run faster than a binary encoded FSM with larger combinational logic blocks

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    Answer :
    - They are used to introduce small delays
    - They are used to eliminate cross talk caused due to inter electrode capacitance due to close routing.
    - They are used to support high fanout,eg:bufg
13. **Question 13. Implement An And Gate Using Mux?**
    Answer :
    This is the basic question that many interviewers ask. for and gate, give one input as select line,incase if u r giving b as select line, connect one input to logic '0' and other input to a.
14. **Question 14. What Will Happen If Contents Of Register Are Shifter Left, Right?**
    Answer :
    It is well known that in left shift all bits will be shifted left and LSB will be appended with 0 and in right shift all bits will be shifted right and MSB will be appended with 0 this is a straightforward answer What is expected is in a left shift value gets Multiplied by 2 eg:consider 0000_1110=14 a left shift will make it 0001_110=28, it the same fashion right shift will Divide the value by 2.
15. **Question 15. What Is A Multiplexer?**
    Answer :
    A multiplexer is a combinational circuit which selects one of many input signals and directs to the only output.
16. **Question 16. What Is A Ring Counter?**
    Answer :
    A ring counter is a type of counter composed of a circular shift register. The output of the last shift register is fed to the input of the first register. For example, in a 4-register counter, with initial register values of 1100, the repeating pattern is: 1100, 0110, 0011, 1001, 1100, so on.
17. **Question 17. Compare And Contrast Synchronous And Asynchronous Reset?**
    Answer :
    Synchronous reset logic will synthesize to smaller flip-flops, particularly if the reset is gated with the logic generating the d-input. But in such a case, the combinational logic gate count grows, so the overall gate count savings may not be that significant. The clock works as a filter for small reset glitches; however, if these glitches occur near the active clock edge, the Flip-flop could go metastable. In some designs, the reset must be generated by a set of

internal conditions. A synchronous reset is recommended for these types of designs because it will filter the logic equation glitches between clock.

Problem with synchronous resets is that the synthesis tool cannot easily distinguish the reset signal from any other data signal. Synchronous resets may need a pulse stretcher to guarantee a reset pulse width wide enough to ensure reset is present during an active edge of the clock, if you have a gated clock to save power, the clock may be disabled coincident with the assertion of reset. Only an asynchronous reset will work in this situation, as the reset might be removed prior to the resumption of the clock. Designs that are pushing the limit for data path timing, can not afford to have added gates and additional net delays in the data path due to logic inserted to handle synchronous resets.

Asynchronous reset: The major problem with asynchronous resets is the reset release, also called reset removal. Using an asynchronous reset, the designer is guaranteed not to have the reset added to the data path. Another advantage favoring asynchronous resets is that the circuit can be reset with or without a clock present. Ensure that the release of the reset can occur within one clock period else if the release of the reset occurred on or near a clock edge then flip-flops may go into metastable state.

18. **Question 18. What Is A Johnson Counter?**
Answer :
Johnson counter connects the complement of the output of the last shift register to its input and circulates a stream of ones followed by zeros around the ring. For example, in a 4-register counter, the repeating pattern is: 0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001, so on.

19. **Question 19. What Are The Differences Between A Flip-flop And A Latch?**
Answer :
    - Flip-flops are edge-sensitive devices where as latches are level sensitive devices.
    - Flip-flops are immune to glitches where are latches are sensitive to glitches.
    - Latches require less number of gates (and hence less power) than flip-flops.
    - Latches are faster than flip-flops.

20. **Question 20. What Is The Difference Between Mealy And Moore Fsm?**
Answer :
Mealy FSM uses only input actions, i.e. output depends on input and state. The use of a Mealy FSM leads often to a reduction of the number of states.

    Moore FSM uses only entry actions, i.e. output depends only on the state. The advantage of the Moore model is a simplification of the behavior.

21. **Question 21. What Are Various Types Of State Encoding Techniques? Explain Them?**
Answer :
One-Hot encoding: Each state is represented by a bit flip-flop). If there are four states then it requires four bits (four flip-flops) to represent the current state. The valid state values are 1000, 0100, 0010, and 0001. If the value is 0100, then it means second state is the current state.
One-Cold encoding: Same as one-hot encoding except that '0' is the valid value. If there are four states then it requires four bits (four flip-flops) to represent the current state. The valid state values are 0111, 1011, 1101, and 1110.
Binary encoding: Each state is represented by a binary code. A FSM having '2 power N' states requires only N flip-flops.

Gray encoding: Each state is represented by a Gray code. A FSM having '2 power N' states requires only N flip-flops.

22. **Question 22. Define Clock Skew , Negative Clock Skew, Positive Clock Skew?**

    Answer :

    Clock skew is a phenomenon in synchronous circuits in which the clock signal (sent from the clock circuit) arrives at different components at different times. This can be caused by many different things, such as wire-interconnect length, temperature variations, variation in intermediate devices, capacitive coupling, material imperfections, and differences in input capacitance on the clock inputs of devices using the clock.

    There are two types of clock skew: negative skew and positive skew. Positive skew occurs when the clock reaches the receiving register later than it reaches the register sending data to the receiving register. Negative skew is the opposite: the receiving register gets the clock earlier than the sending register.

23. **Question 23. Define Metastability?**

    Answer :

    If there are setup and hold time violations in any sequential circuit, it enters a state where its output is unpredictable, this state is known as metastable state or quasi stable state, at the end of metastable state, the flip-flop settles down to either logic high or logic low. This whole process is known as metastability.

24. **Question 24. What Are Set Up Time And Hold Time Constraints?**

    Answer :

    Set up time is the amount of time before the clock edge that the input signal needs to be stable to guarantee it is accepted properly on the clock edge.

    Hold time is the amount of time after the clock edge that same input signal has to be held before changing it to make sure it is sensed properly at the clock edge.

    Whenever there are setup and hold time violations in any flip-flop, it enters a state where its output is unpredictable, which is known as as metastable state or quasi stable state. At the end of metastable state, the flip-flop settles down to either logic high or logic low. This whole process is known as metastability.

25. **Question 25. Expand The Following: Pla, Pal, Cpld, Fpga?**

    Answer :

    PLA - Programmable Logic Array
    PAL - Programmable Array Logic
    CPLD - Complex Programmable Logic Device
    FPGA - Field-Programmable Gate Array

26. **Question 26. What Are Pla And Pal? Give The Differences Between Them?**

    Answer :

    Programmable Logic Array is a programmable device used to implement combinational logic circuits. The PLA has a set of programmable AND planes, which link to a set of programmable OR planes, which can then be conditionally complemented to produce an output.

    PAL is programmable array logic, like PLA, it also has a wide, programmable AND plane. Unlike a PLA, the OR plane is fixed, limiting the number of terms that can be ORed together.

Due to fixed OR plane PAL allows extra space, which is used for other basic logic devices, such as multiplexers, exclusive-ORs, and latches. Most importantly, clocked elements, typically flip-flops, could be included in PALs. PALs are also extremely fast.

27. **Question 27. What Is Lut?**
    Answer :
    LUT - Look-Up Table. An n-bit look-up table can be implemented with a multiplexer whose select lines are the inputs of the LUT and whose inputs are constants. An n-bit LUT can encode any n-input Boolean function by modeling such functions as truth tables. This is an efficient way of encoding Boolean logic functions, and LUTs with 4-6 bits of input are in fact the key component of modern FPGAs.
28. **Question 28. What Is The Significance Of Fpgas In Modern Day Electronics? (applications Of Fpga.)**
    Answer :
    - ASIC prototyping: Due to high cost of ASIC chips, the logic of the application is first verified by dumping HDL code in a FPGA. This helps for faster and cheaper testing. Once the logic is verified then they are made into ASICs.
    - Very useful in applications that can make use of the massive parallelism offered by their architecture. Example: code breaking, in particular brute-force attack, of cryptographic algorithms.
    - FPGAs are sued for computational kernels such as FFT or Convolution instead of a microprocessor.
    - Applications include digital signal processing, software-defined radio, aerospace and defense systems, medical imaging, computer vision, speech recognition, cryptography, bio-informatics, computer hardware emulation and a growing range of other areas.
29. **Question 29. Arrange The Following In The Increasing Order Of Their Complexity: Fpga,pla,cpld,pal?**
    Answer :
    Increasing order of complexity: PLA, PAL, CPLD, FPGA.

1. What is meant by D-FF?
2. What is the basic difference between Latches and Flip flops?
3. What is a multiplexer?
4. How can you convert an SR Flip-flop to a JK Flip-flop?
5. How can you convert a JK Flip-flop to a D Flip-flop?
6. What is Race-around problem? How can you rectify it?
7. Which semiconductor device is used as a voltage regulator and why?
8. What do you mean by an ideal voltage source?
9. What do you mean by zener breakdown and avalanche breakdown?
10. What are the different types of filters?

Question1. What is difference between latch and flip-flop?
Answer: The main difference between latch and FF is that latches are level sensitive while FF is edge sensitive. They both require the use of clock signal and are used in sequential logic. For a latch, the output tracks the input when the clock signal is high, so as long as the clock is logic 1, the output can change if the input also changes.

FF on the other hand, will store the input only when there is a rising/falling edge of the clock. Latch is sensitive to glitches on enable pin, whereas flip-flop is immune to glitches. Latches take fewer gates (also less power) to implement than flip-flops. Latches are faster than flip-flops.

Question2. Given only two xor gates one must function as buffer and another as inverter?
Answer: Tie one of xor gates input to 1 it will act as inverter. Tie one of xor gates input to 0 it will act as buffer.

Question3. How to achieve 180 degree exact phase shift?
Answer:

1. a) DCM an inbuilt resource in most of FPGA can be configured to get 180 degree phase shift.
2. b) BUFGDS that is differential signaling buffers which are also inbuilt resource of most of FPGA can be used. Digital Electronics Solved Questions

Question4. What is Electronic?
Answer: The study and use of electrical devices that operate by controlling the flow of electrons or other electrically charged particles.

Question5. What is communication?
Answer: Communication means transferring a signal from the transmitter which passes through a medium then the output is obtained at the receiver. (or)communication says as transferring of message from one place to another place called communication.

Question6. What is sampling?
Answer: The process of obtaining a set of samples from a continuous function of time x(t) is referred to as sampling.

Question7. State sampling theorem.
Answer: It states that, while taking the samples of a continuous signal, it has to be taken care that the sampling rate is equal to or greater than twice the cut off frequency and the minimum sampling rate is known as the Nyquist rate.

Question8. What is cut-off frequency?
Answer: The frequency at which the response is -3dB with respect to the maximum response.

Question9. What is pass band?

Answer: Passband is the range of frequencies or wavelengths that can pass through a filter without being attenuated.

Question10. What is stop band?
Answer: A stopband is a band of frequencies, between specified limits, in which a circuit, such as a filter or telephone circuit, does not let signals through, or the attenuation is above the required stopband attenuation level.