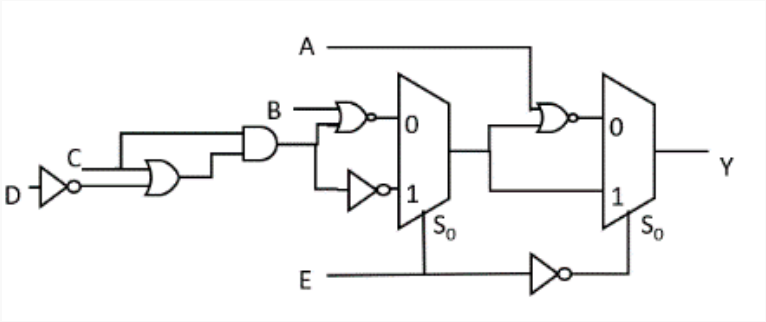
Question Bank in **Static Timing Analysis (STA)**

1. Consider the following logic circuit. Delays of logic gates are t_{nor} = 1.5ns, t_{inv} = 1ns, t_{or} = 2ns, t_{and} = 1.5ns and t_{mux} = 2.5ns

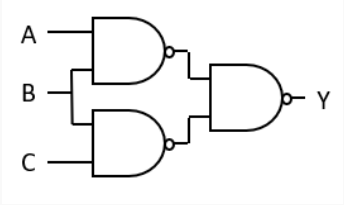


The critical path delay in the logic circuit given above is ___(in ns)

2. Find the delay of the false path in the logic circuit given in Question 1.

11ns 10ns 11.5ns 12.5ns

3. Consider the following logic circuit.



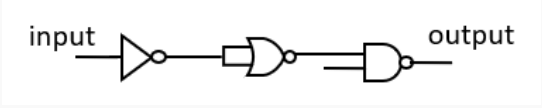
What is the Unateness of output pin Y with respect to the input pin B?

Negative unate Positive unate Non unate Cannot be determined

4. The number of timing arcs in a three input AND gate are

3 4 6 7

5. Consider the given logic circuit. Find the rise and fall delays of the timing path from input to output.

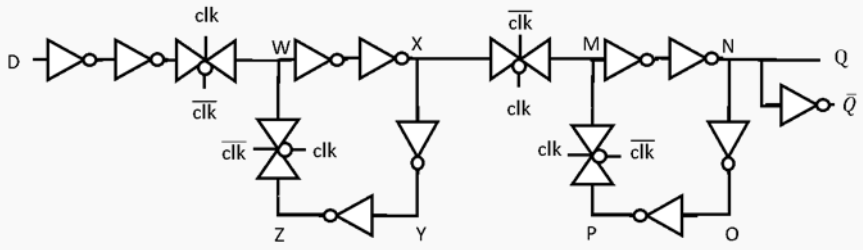


The rise and fall delays of the gates are as follows

Gate	NOT(ns)	NOR(ns)	NAND(ns)
Rise delay	2	2	5
Fall delay	2	3	4

t_{rise} = 10ns, t_{fall} = 8ns t_{rise} = 8ns, t_{fall} = 9ns t_{rise} = 7ns, t_{fall} = 10ns t_{rise} = 9ns, t_{fall} = 8ns

6. Consider the master-slave flipflop circuit given below.



Delays of gates are t_{inv} = 0.5ns, t_{tx} = 1ns.

Given master-slave flipflop is _____ triggered.

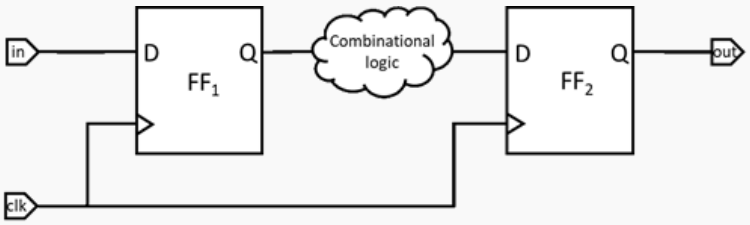
Positive edge Negative edge Level None of the above

7. The setup time of the master-slave flipflop given in question 6 is _____(in ns)

8. The hold time of the master-slave flipflop given in question 6 is

Negative Positive Zero Cannot be determined

9. Consider the following diagram.



Delay values of Flipflop and Combinational circuit are: t_{setup} = 5ns and t_{hold} = 4ns.

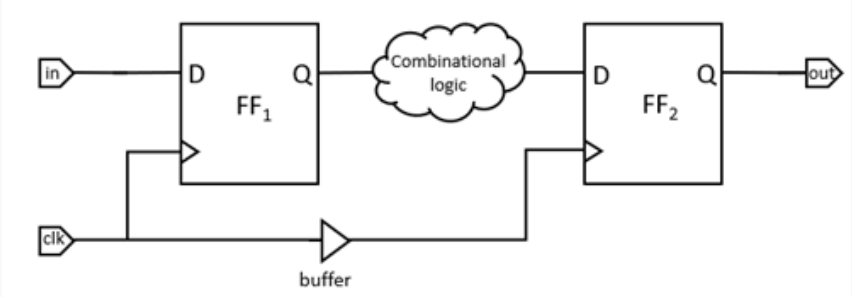
Delay	t_{clk-q}	t_{comb}
Max	4 ns	7 ns
Min	3 ns	2 ns

The maximum frequency at which the given circuit can operate without failure is ___(in MHz)

10. Choose the correct hold constraint equation for the circuit given in question 9.

4ns ≤ 3ns + 7ns 4ns ≤ 3ns + 2ns 4ns ≤ 4ns + 7ns 4ns ≤ 4ns + 2ns

11. Consider the following circuit.



Delay values of Flipflop and Combinational circuit are: t_{setup} = 5ns and t_{hold} = 4ns. The delay of the buffer is t_{buf} = 2ns.

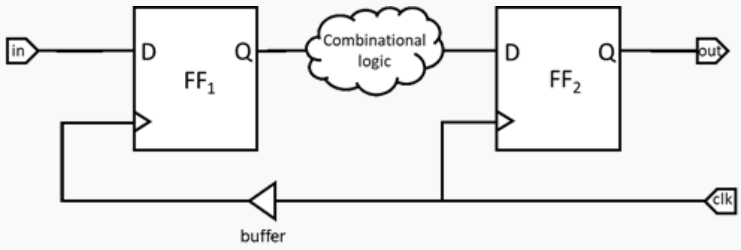
Delay	t_{clk-q}	t_{comb}
Max	4 ns	7 ns
Min	3 ns	2 ns

The maximum frequency at which the given circuit can operate without failure is _____(MHz)

12. Choose the correct hold constraint equation for the circuit given in question 1.

4ns ≤ 4ns + 7ns 4ns - 2ns ≤ 3ns + 2ns 4ns + 2ns ≤ 3ns + 2ns 4ns ≤ 3ns + 2ns + 2ns

13. Consider the following circuit.

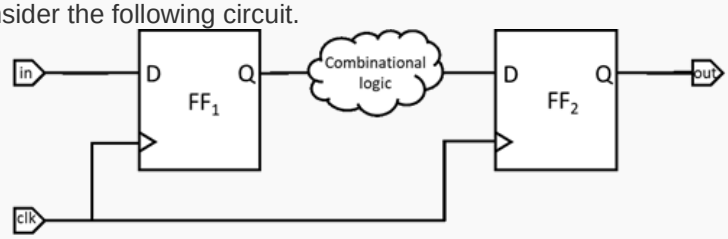


Delay values of Flipflop and Combinational circuit are: t_{setup} = 5ns and t_{hold} = 4ns. The delay of the buffer is t_{buf} = 2ns.

Delay	t_{clk-q}	t_{comb}
Max	4 ns	7 ns
Min	3 ns	2 ns

The maximum frequency at which the given circuit can operate without failure is _____(MHz)

14. Consider the following circuit.



Delay values of Flipflop and Combinational circuit are: t_{setup} = 5ns and t_{hold} = 4ns. The clock period is T_{clk} = 20ns.

Delay	t_{clk-q}	t_{comb}
Max	4 ns	7 ns
Min	3 ns	2 ns

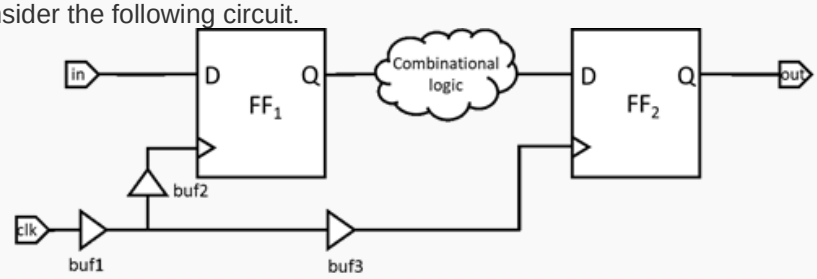
15. What is the maximum allowable jitter (t_{jitter}) in the clock signal so that the given circuit works at the given frequency without failure?

0.5 ns 1 ns 2 ns 4 ns

Choose the correct option(s) about clock skew and clock jitter.

Clock jitter deteriorates the performance of the system
Clock jitter is a spatial variation
Clock period varies due to clock skew
Coupling between two adjacent lines is one of the sources of clock jitter

16. Consider the following circuit.



Delay	$t_{clk\text{-}q}(FF_1)$	$t_{clk\text{-}q}(FF_2)$	t_{comb}
Max	3.8 ns	5 ns	6 ns
Min	2 ns	2.8 ns	2.5 ns

The delays of buffers t_{buf1} = 1.2ns, t_{buf2} = 0.9ns, and t_{buf3} = 0.7ns. The setup and hold time of both flipflops is t_{setup} = 2ns and t_{hold} = 1ns respectively.

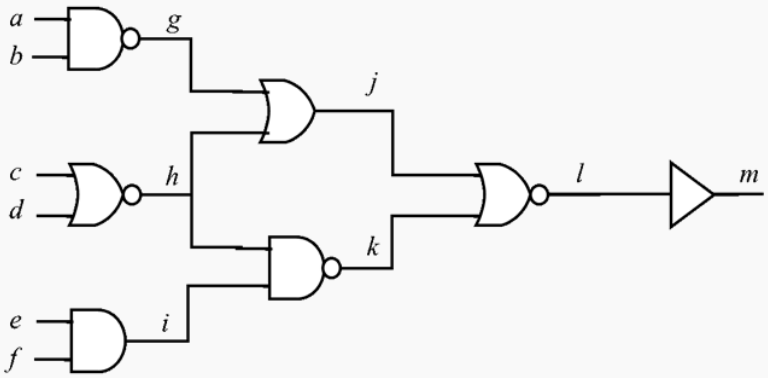
The On-chip variation is modeled as

set_timing_derate -early 0.9 set_timing_derate -late 1.12 set_timing_derate -early 1.08 -cell_check

With On-chip variation, the maximum frequency at which the given circuit can operate without failure is _____(MHz)

17. The value of common path pessimism(CPP) in the circuit given in question 6 is ____ps

18. Consider the following logic circuit.



Logic gate	Rise delay(ns)	Fall delay(ns)
NAND	4	3
NOR	3	5
AND	2	3
OR	5	4
Buffer	1	2

Arrival Time at all primary inputs a, b, c, d, e, and f is 0/0.

Required Time at node 'm' is 16/13. The fall output arrival time at node *'l'* is ____(ns)

19. The rise input required time at node 'c' in the circuit given in question 8 is ____ (ns)

20. The slack(rise/fall) at node 'i' in the circuit given in question 8 is ____(ns/ns)

0/6
6/0
1/4
4/1