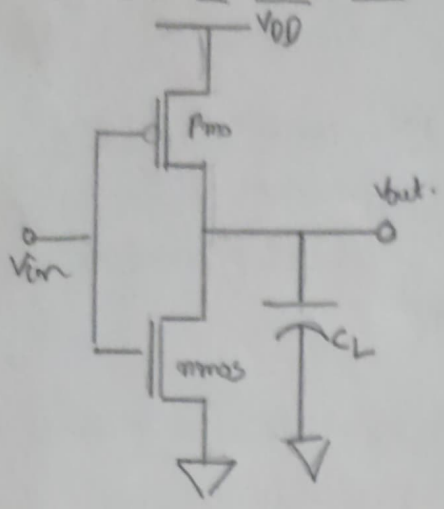
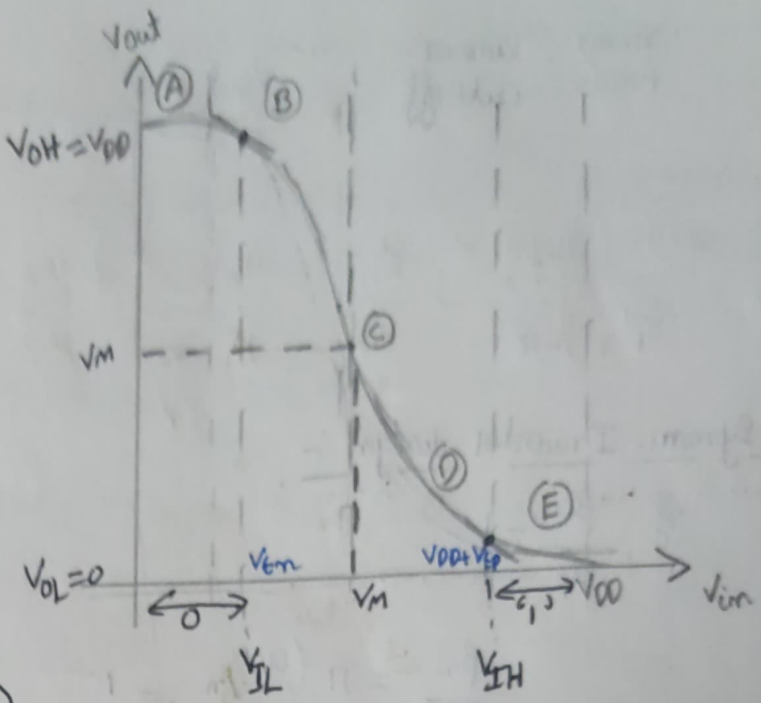
① Inverter :-

⊙ DC characteristics :-





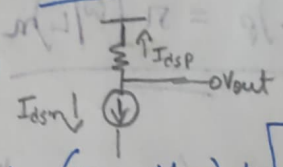
⊙ Region A :- $(0 \le V_{in} \le V_{tn})$

nmos : cut off
Pmos : linear region

$V_{out} = V_{DD}$

⊙ Region B :- $(V_{tn} \le V_{in} \le V_{DD}/2)$

nmos : Saturation
Pmos : linear region

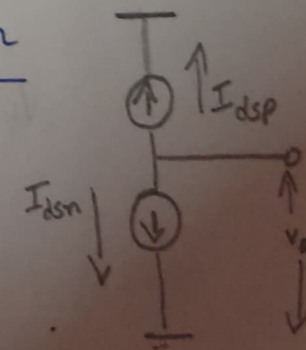


$$V_{out} = (V_{in} - V_{tp}) + \sqrt{(V_{in} - V_{tp})^2 - 2\left(V_{in} - \frac{V_{DD}}{2} - V_{tp}\right) - \beta_n/\beta_p (V_{in} - V_{tn})^2}$$

⊙ Region C :- $\left(V_{in} = \frac{V_{DD}}{2}\right)$

nmos : Saturation
Pmos : Saturation

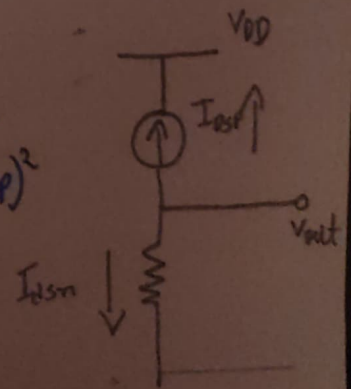
$$V_m = \frac{V_{DD} - |V_{tp}| + \sqrt{\frac{\beta_n}{\beta_p}}\, V_{tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$



Region D :- $(V_{DD}/2 \le V_{in} \le V_{DD} - V_{tp})$

nmos : Saturation
Pmos : non-saturation

$$V_{out} = (V_{in} - V_{tn}) - \sqrt{(V_{in} - V_{tn})^2 - \beta_p/\beta_n (V_{in} - V_{DD} - V_{tp})^2}$$



Region E :- $(V_{in} \geq V_{DD} - V_{tp})$

nmos : linear
Pmos : cutt off

$V_{out} = 0$

$$\frac{\beta_n}{\beta_p} = \frac{K_n'(W/L)_n}{K_p'(W/L)_p}, \quad \frac{K_n'}{K_p'} = \frac{\mu_n C_{ox}}{\mu_p C_{ox}} = \frac{\mu_n}{\mu_p} = r$$

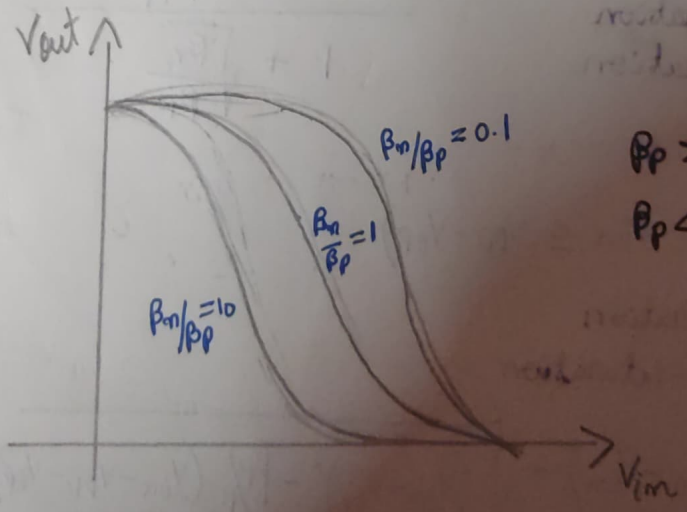
For Symm. Inverter design :-

If $\frac{\beta_n}{\beta_p} = 1$

$$\frac{\beta_n}{\beta_p} = r \frac{(W/L)_n}{(W/L)_p} = 1$$

$$(W/L)_p = r\,(W/L)_n$$ → aspect ratio

$$\frac{\beta_n}{\beta_p} = \left(\frac{V_{DD}/2 - |V_{tp}|}{V_{DD}/2 - V_{tn}}\right)^2$$



$\beta_p > \beta_n$; High skewed Inv

$\beta_p < \beta_n$; low skewed Inv.

Noise Margin :-

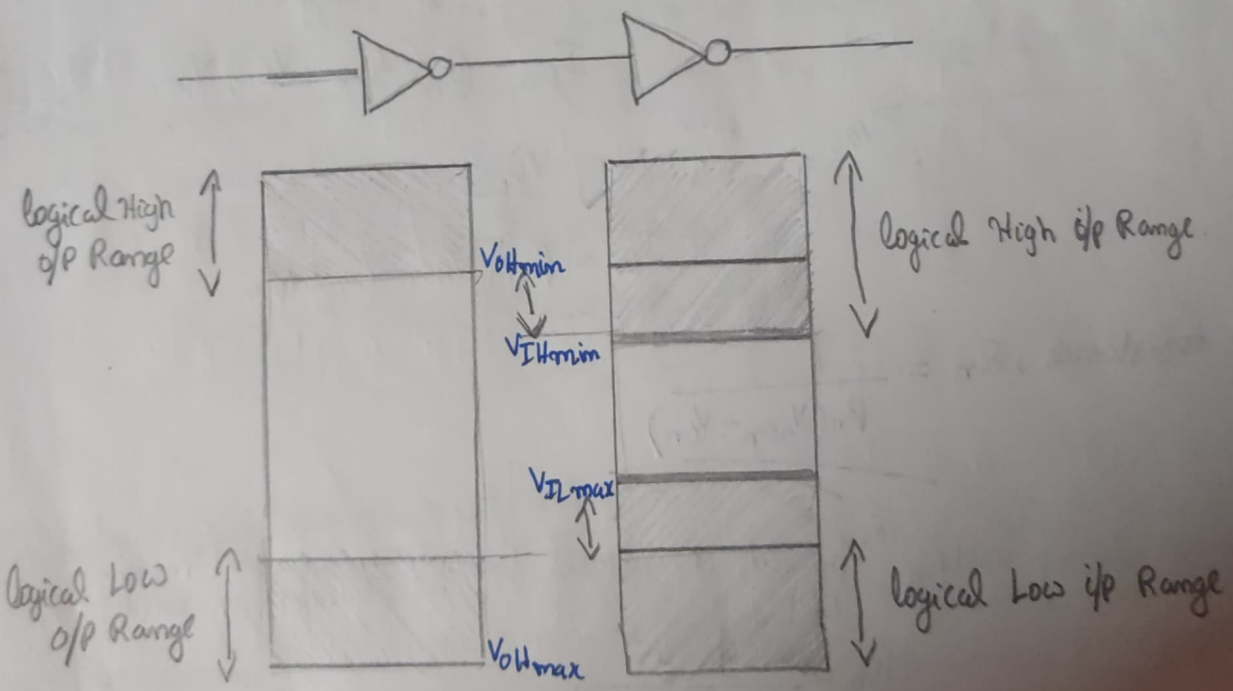
- This parameter allows us to determine the allowable noise voltage on the input of a gate so that the o/p will not be affected.

- **Low noise Margin, NM_L** :- difference in magnitude b/w the maximum Low o/p voltage of the driving gate & the max i/p Low voltage recognized by the driven gate

$$NM_L = |V_{ILmax} - V_{OLmax}|$$

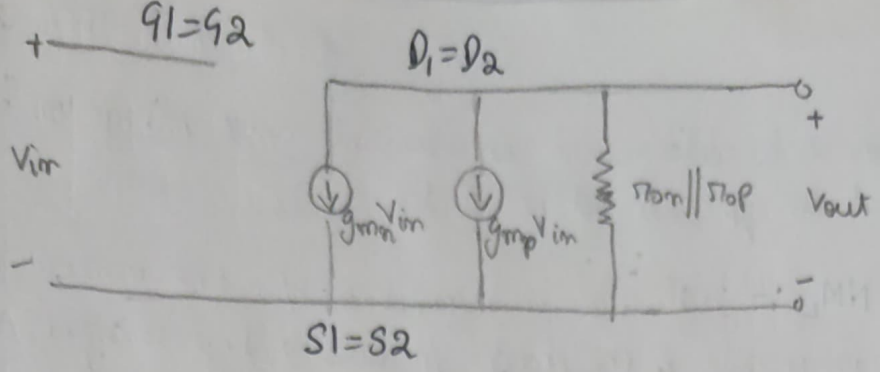
- **High noise Margin, NM_H** :- difference in magnitude b/w the min. HIGH o/p voltage of the driving gate & the min. i/p HIGH voltage recognized by the receiving gate.

$$NM_H = |V_{OHmin} - V_{IHmin}|$$



$$NM_L = V_{inv} - \frac{V_{DD} - V_{IN}}{A_V}$$

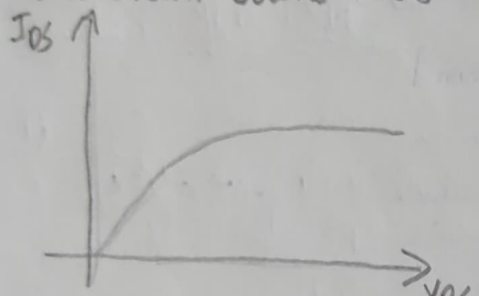
$$NM_H = V_{DD} - V_{inv}\left(1 + \frac{1}{|A_V|}\right)$$



$$A_v = -(g_{mn} + g_{mp})(r_{on} // r_{op})$$

⊙ Drain-Source FET Resistance :-

The drain-Source resistance at any point on curve $R_n = \frac{V_{DSn}}{I_{Dn}}$



Current in non-saturated region

$$I_{Dn} = \beta_n \left[(V_{GSn} - V_{tn}) V_{DSn} - \frac{V_{DSn}^2}{2} \right]$$

*** ignoring $\frac{V_{DSn}^2}{2}$

$$I_{Dn} = \beta_n \left[V_{GSn} - V_{tn} \right] V_{DSn}$$

The resistance, $R_n = \frac{1}{\beta_n (V_{GSn} - V_{tn})}$

• The power supply voltage 'V_{DD}' as the largest possible value for 'V_{GSn}'

$$R_n = \frac{1}{\beta_n (V_{DD} - V_{tn})}$$

$$R_n \propto \frac{1}{\beta_n}$$

large β_n conducts more current than small β_n

Capacitances :-

i) **gate capacitance C_g** :- ie due to the MOS structure. Since this is the region that has a gate oxide thickness of t_{ox}.

$$C_g = C_{ox} A_g$$

$C_g = C_{ox} \omega L$, gate capacitance $\propto$ width of the channel

ii) **Gate source capacitance & gate drain capacitance** :-

Their value change with the voltage due to the changing shape of the channel region, the capacitance is said to be non-linear.

$$C_{gs} = \frac{1}{2} C_g \simeq C_{gD}$$

iii) **Junction Capacitance** :-

- Pn junction automatically exhibits capacitance due to the opposite polarity charge involed. This is called **junction or depletion** capacitance and is found at every drain or source region of a FET. C_{SB} (source-bulk) & C_{DB} (drain-bulk)

$$C_n = C_{bot} + C_{sw}$$

$$= C_j A_{bot} + C_{jsw} P_{sw}$$

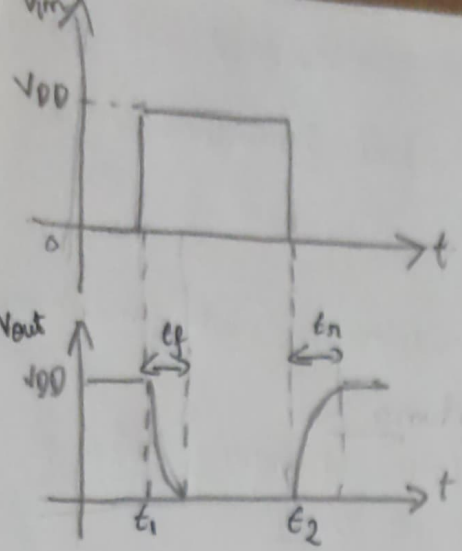
Inverter Switching Characteristics :-

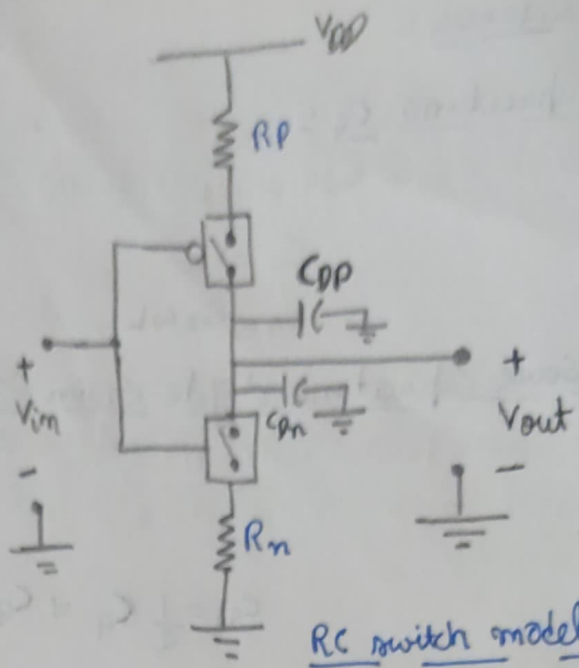
The o/p waveform reacts to the i/p, but o/p voltage cannot change instantaneously. The o/p 1-to-0 transistion introduces fall time delay t_f; while the 0 to 1 change at the o/p is described by rise time t_r

- The rise & fall time delays are due to parasitic resistance and capacitances of the transistors.

resistance, $R_n = \dfrac{1}{\beta_n (V_{DD} - V_{tn})}$ $\qquad R_n = \dfrac{1}{\partial I_{ds} / \partial V_{ds}}$

$$R_p = \frac{1}{\beta_p (V_{DD} - |V_{TP}|)}$$





RC switch model Equivalent

① Capacitance C_{on} & C_{DP} :-

$\rightarrow C_{gs} \simeq C_{DS} = 1/2 C_g$ → gate capacitance

i) $C_{Dn} = C_{gsn} + C_{DBn}$

$C_{on} = \underbrace{\frac{1}{2} C_{ox} L' W_n}_{\text{gate-source/drain cap.}} + \underbrace{C_{jn} A_n}_{\text{Bottom}} + \underbrace{C_{jswn} P_n}_{\text{sidewall}}$

(Area → A_n; Perimeter → P_n)

Drain-Bulk cap/Junction capacitance.

ii) $C_{DP} = C_{gsp} + C_{DBp} = \frac{1}{2} C_{ox} L' W_n + C_{jp} A_p + C_{jswp} P_p$

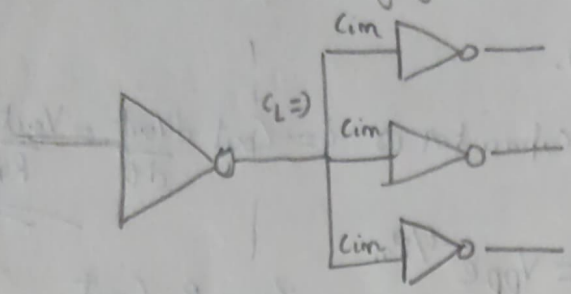
② In a logic chain, every logic gate must drive another gate or set of gates to be use full. The no. of gates is specified by the fan-out (Fo) of CK

. The fan-out gates acts a load to the driving ckt because of their input capacitance Cin.

** Input capacitance is the sum of the Fet capacitance i.e Gate capacitance of nmos & Pmos

$$C_{in} = C_{gp} + C_{gn} \quad \text{——(*)(*)}$$

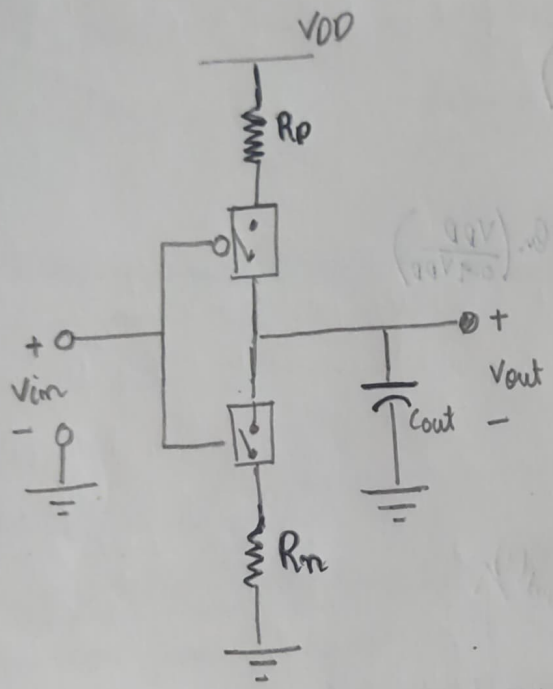
The i/p capacitance of each gate acts as an external load capacitance 'C_L' to the driving gate



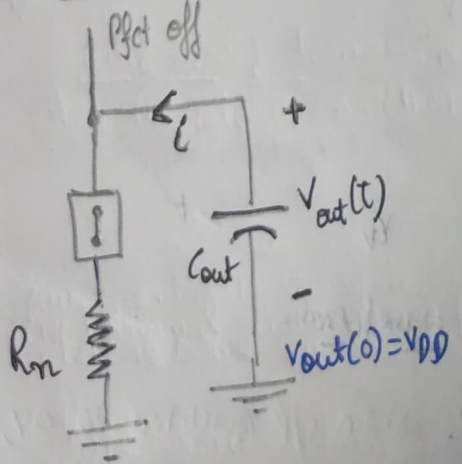
$C_L = 3C_{in}$ (caps are in parallel)

Total output capacitance $C_{out} = C_{FET} + C_L$

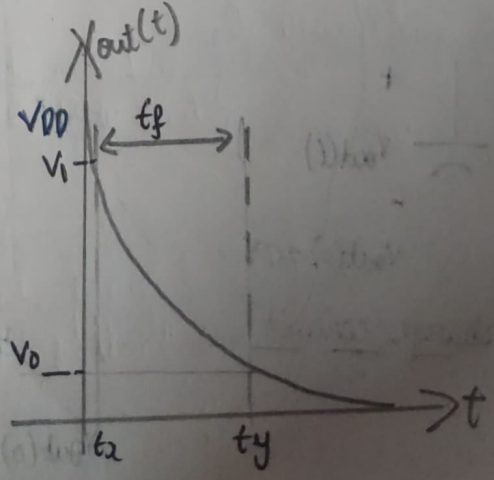
$C_{FET} = C_{Dn} + C_{DP}$



① Fall time :-



a) Discharge circuit



b) o/p waveform

The initial condition at the o/p is $V_{out}(0) = V_{DD}$. when the i/p is switch, the nFET goes active while PFET is driven into cutoff. The capacitor Cout initially charged to voltage V_{DD}.

The current leaving the capacitor is $i = -C_{out}\frac{dV_{out}}{dt} = \frac{V_{out}}{R_n}$

$$V_{out}(t) = V_{DD}e^{-t/\tau_n} \qquad \tau_n = R_n C_{out}$$

The fall time is defined to be the time interval from 90% V_{DD} to 10% V_{DD}

$$t = \tau_n \ln\left(\frac{V_{DD}}{V_{out}}\right)$$

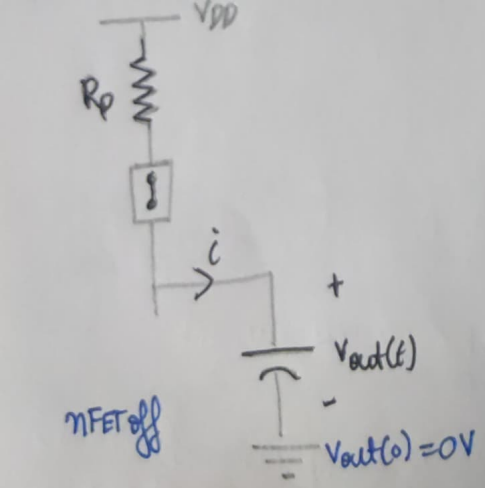
$$t_f = t_y - t_x$$

$$t_f = t_n \ln\left(\frac{V_{DD}}{0.1V_{DD}}\right) - \tau_n \ln\left(\frac{V_{DD}}{0.9V_{DD}}\right)$$

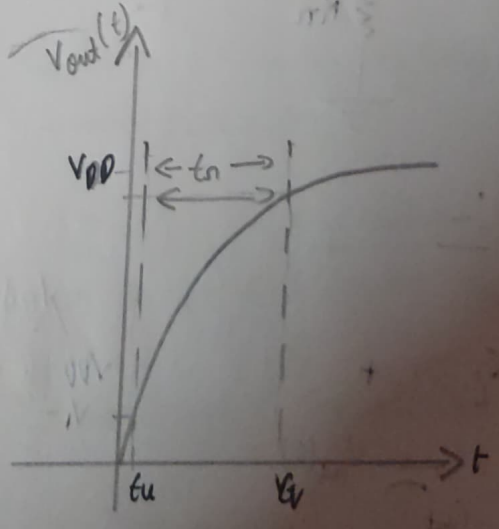
$$t_f = t_n \ln(9)$$

$$t_f = 2.2\tau_n = t_{HL}$$

⊙ Rise time :-



a) charge circuit



b) o/p waveform

The initial condition at the o/p is $V_{out}(0) = 0V$. when i/p switched to 0V, nFET turns off & PFET turns ON. The capacitor Cout is at 0V, at $t = 0$

charging current is given by

$$i = C_{out}\frac{dV_{out}}{dt} = \frac{V_{DD}-V_{out}}{R_n}$$

$$V_{out} = V_{DD}(1-e^{-t/\tau_n})$$

$$\tau_p = R_p C_{out}$$

The rise time is taken b/w 10% & 90%.

$$t_r = t_v - t_u$$

$$t_r = 2.2\tau_p$$

- maximum signal frequency $f_{max} = \frac{1}{t_{HL}+t_{LH}} = \frac{1}{t_r + t_f}$

① Propagation delay :-

The propagation delay time t_p is often used to estimate the "reaction" delay time from i/p to o/p

$$t_p = \frac{t_{pf} + t_{pr}}{2}$$

t_{pf} is the o/p fall time from the max. level to 50% voltage i.e V_{DD} to $\frac{V_{DD}}{2}$

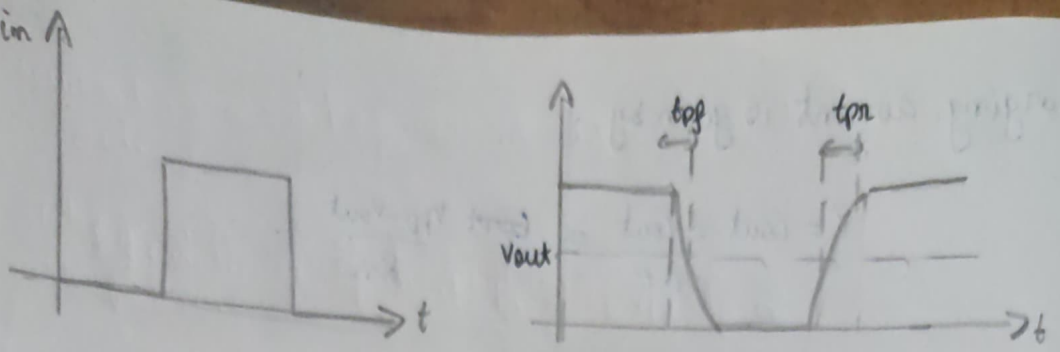
t_{pr} is the propagation rise time from 0V to $(V_{DD}/2)$.

$$t_{pf} = \ln(2)\tau_n = 0.693\tau_n$$

$$t_{pr} = \ln(2)\tau_p = 0.693\tau_p$$

$$t_p = 0.35(\tau_n + \tau_p)$$

** The propagation delay is a useful estimate of the basic delay, but does not provide detailed info. on the rise & fall times as individual quantities



$C_{out} = C_{FET} + C_L$

rise time $t_r = 2.2 R_n C_{out}$

$t_r = 2.2 R_n (C_{FET} + C_L)$

$t_r = t_{ro} + \alpha_n C_L$

$t_{ro} = 2.2 R_n C_{FET}$

$\alpha_n = 2.2 R_n$

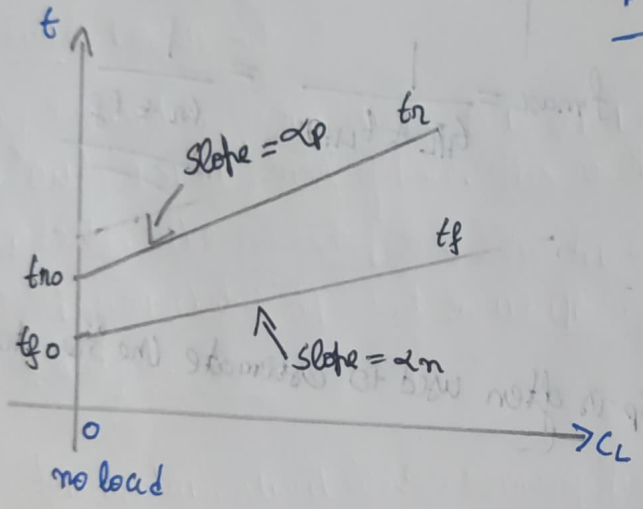
fall time $t_f = 2.2 R_p C_{out}$

$t_f = 2.2 R_p (C_{FET} + C_L)$

$t_f = t_{fo} + \alpha_p C_L$

$t_{fo} = 2.2 R_p C_{FET}$

$\alpha_p = 2.2 R_p$



Speed versus area trade off

⊙ Power dissipation :-

i) Static dissipation :- In CMOS inverter, one transistor is always OFF when the gate is in either of the logic states. Since no current flows into the terminal, there is no DC current path from V_{DD} to V_{SS}, the resultant quiescent (steady-state) current, hence power P_s is zero.

There is some small static dissipation due to reverse bias leakage b/w

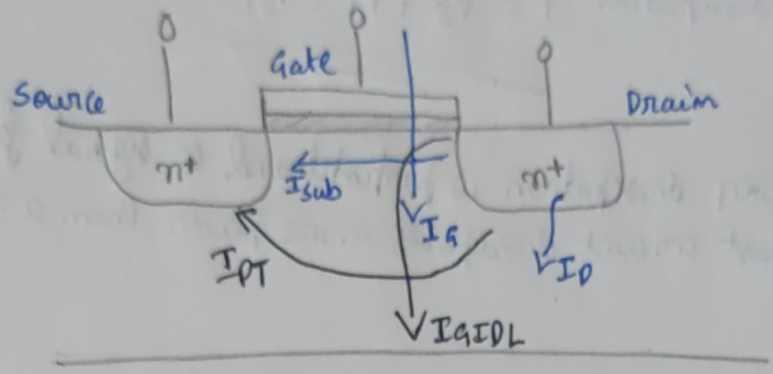
- the source-drain diffusions & n-well diffusion from parasitic diodes

The parasitic diodes is shown b/w n-well & substrate. Since parasitic diodes are reverse biased, only their leakage current contributes to static power dissipation.

Leakage current $I_0 = i_s (e^{qV/kT} - 1)$

Static power dissipation. $P_s = V_{DD} i_0$

⊙ Leakage power :-

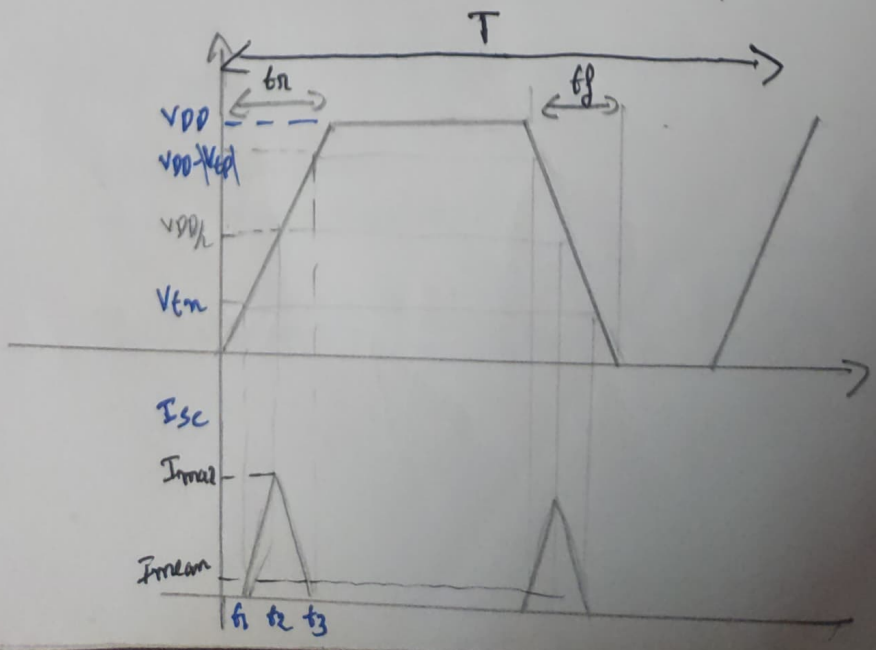


⊙ Dynamic Power :-

During transition from either 0 to 1, or 1 to 0, both n & p transistor are "ON" for short period of time. This results in short current pulse from V_{DD} to V_{SS}. The current pulse from V_{DD} to V_{SS} results in "short circuit" dissipation that is dependent on the i/p rise & fall time, the load capacitance & gate design.

For inverter without load, assuming that $t_r = t_f (t_{rf})$

$$P_{sc} = \beta/12 (V_{DD} - 2V_t)^3 \frac{t_{rf}}{T}$$



- Current is also required to charge & discharge the o/p capacitance load.

Dynamic dissipation $P_d = C_L V_{DD}^2 f_p \alpha$

Total Power dissipation $P = P_s + P_d + P_{SC}$

*** The dynamic power dissipation is proportional to signal frequency, other words a fast circuit dissipates more power than a slow circuit