Physical Verification (DRC)

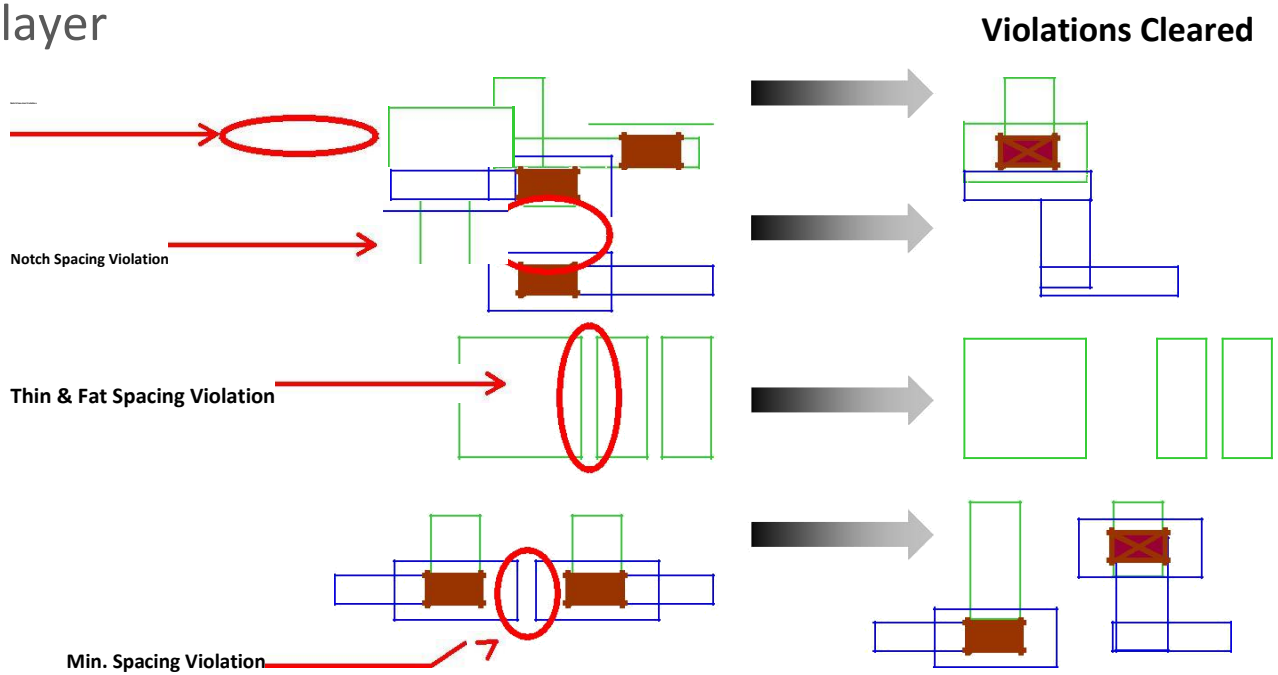
- Design Rule Check (DRC) is the process of checking physical layout data against fabrication-specific rules specified by the foundry to ensure successful fabrication
- Process specific design rules must be followed when drawing layouts to avoid any manufacturing defects during the fabrication of an IC
- Process design rules are the minimum allowable drawing dimensions which affects the X and Y dimensions of layout and not the depth/vertical dimensions
- As Technology Shrinks
  - Number of Design Rules are increasing
  - Complexity of Routing Rules is increasing
  - Increasing the number of objects involved
  - More Design Rules depending on Width, Halo, Parallel Length

DRC Rule130nm		90nm	65nm	45nm
Width-based Spacing	1-2	2-3	3-5	7
Min-Area Rule	1 pitch	2 pitch	3 pitch	5 pitch
Cut Number (Via)	N/A	1-2	4-5	5-6
Dense EoL (OPC)	N/A	N/A	M1/M2	All Layers
Min-step (OPC)	N/A	1	5	5

- Violating a design rule might result in a non-functional circuit or low Yield

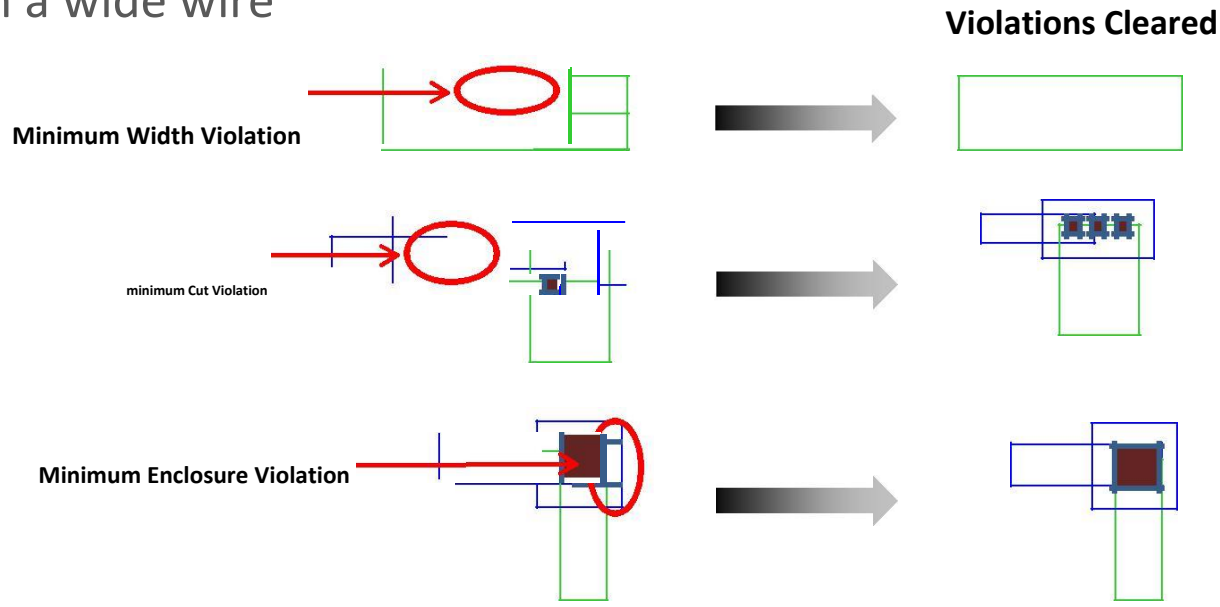
Physical Verification (DRC)

- Design Rule examples
  - Maximum Rules: Manufacturing of large continuous regions can lead to stress cracks. So 'wide metal' must be 'slotted' (holes)
  - Angles: Usually only multiples of 45 degree are allowed
  - Grid: All corner points must lie on a minimal grid, otherwise an "off grid error" is produced
  - Minimum Spacing: The minimum spacing between objects on a single layer



Physical Verification (DRC)

- Design Rule examples
  - Minimum Width: The min width rule specifies the minimum width of individual shapes on a single layer
  - Minimum Enclosure/ Overlap: Implies that the second layer is fully enclosed by the first one
  - Notch: The rule specifies the minimum spacing rule for objects on the same net, including defining the minimum notch on a single-layer, merged object
  - Minimum Cut: the minimum number of cuts a via must have when it is on a wide wire

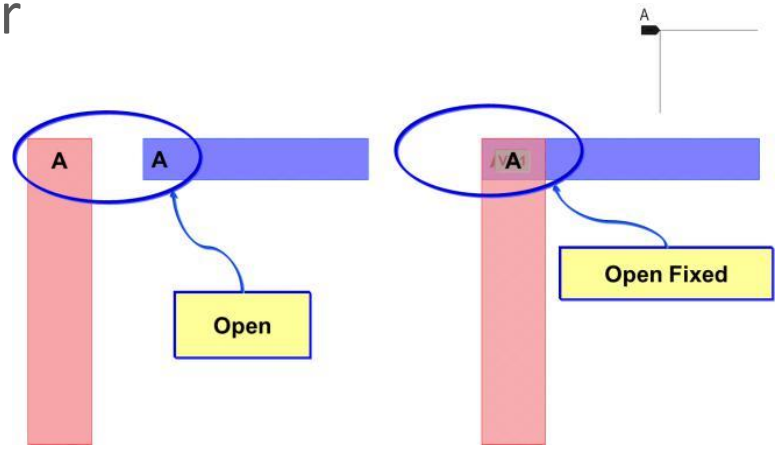


Physical Verification (LVS)

- Layout Versus Schematic (LVS) verifies the connectivity of a Verilog Netlist and Layout Netlist (Extracted Netlist from GDS)
- Tool extracts circuit devices and interconnects from the layout and saved as Layout Netlist (SPICE format)
- As LVS performs comparison between 2 Netlist, it does not compare the functionalities of both the Netlist
- Input Requirements
  - LVS Rule deck
  - Verilog Netlist
  - Physical layout database (GDS)
  - Spice Netlist (Extracted by the tool from GDS)
- LVS checks examples
  - Short Net Error, Open Net Error, Extract errors, Compare errors

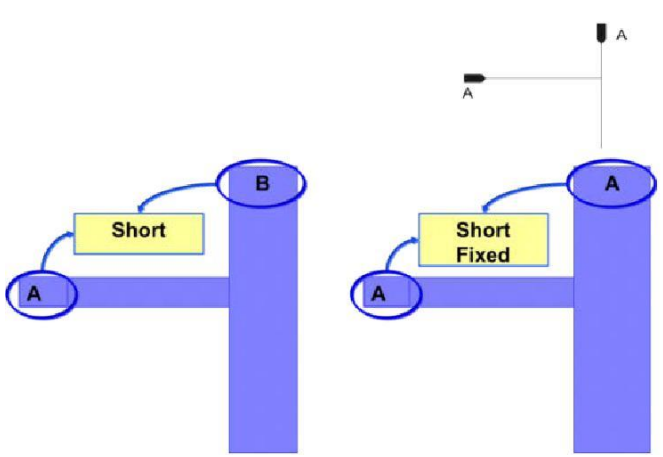
Physical Verification (LVS)

- Open Net Error

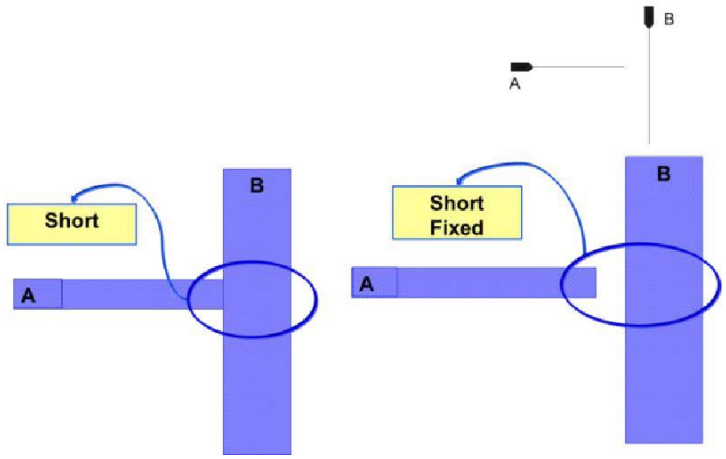


Same net is routed in two different metal layers but not connected

- Short Net Error



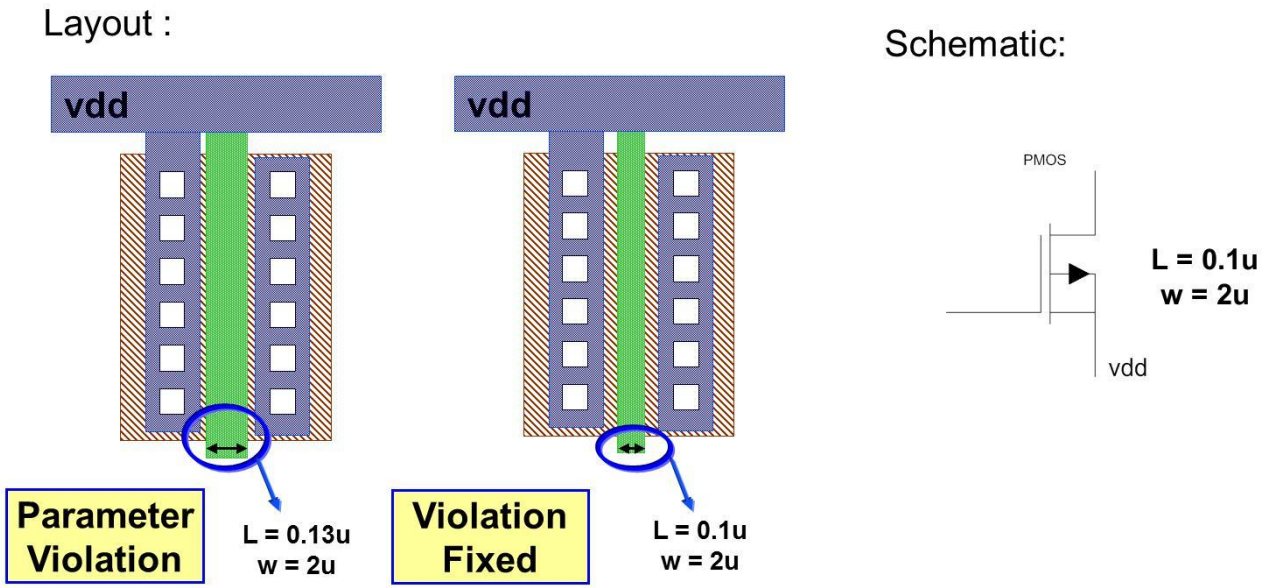
Same net with different pin names



Two different nets shorting together

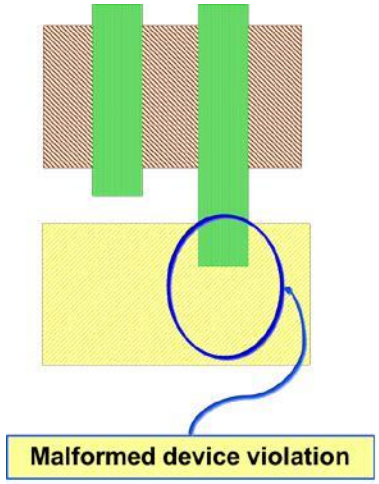
Physical Verification (LVS)

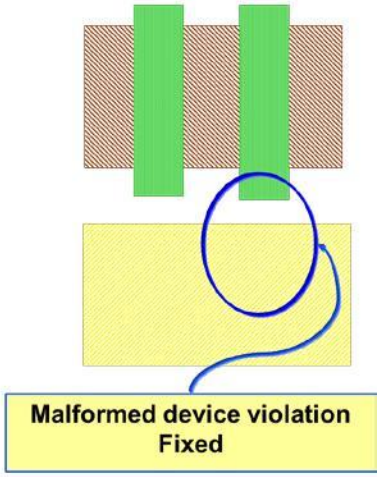
- Extract Errors
  - Parameter Mismatch
  - Device parameters on schematic and layout are compared
  - Example: Let us consider a transistor here, LVS checks are necessary parameters like width, length, multiplication factor etc.

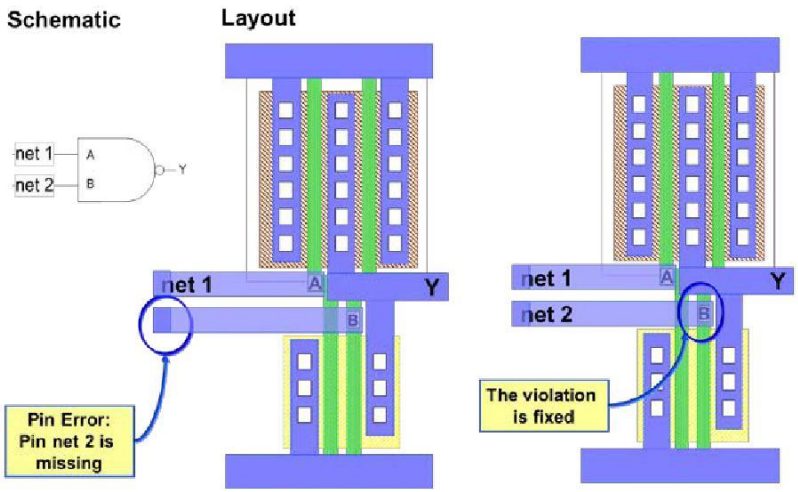


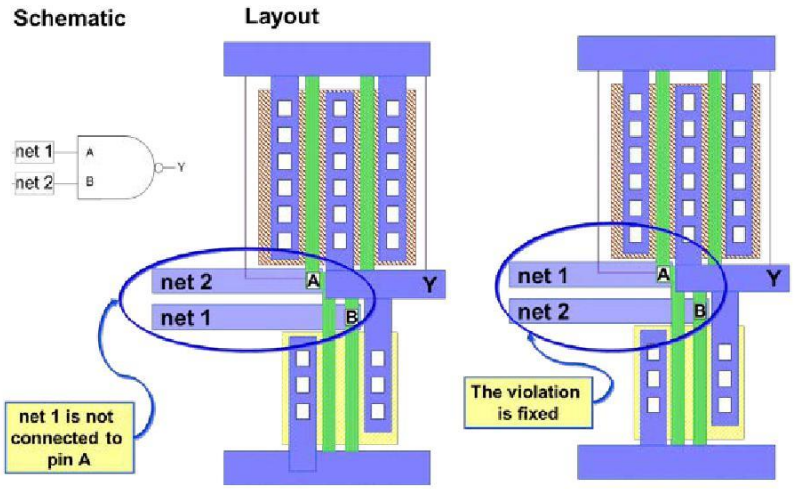
Physical Verification (LVS)

- Compare Errors
  - Malformed Devices
  - Pin Errors
  - Device Mismatch
  - Net Mismatch



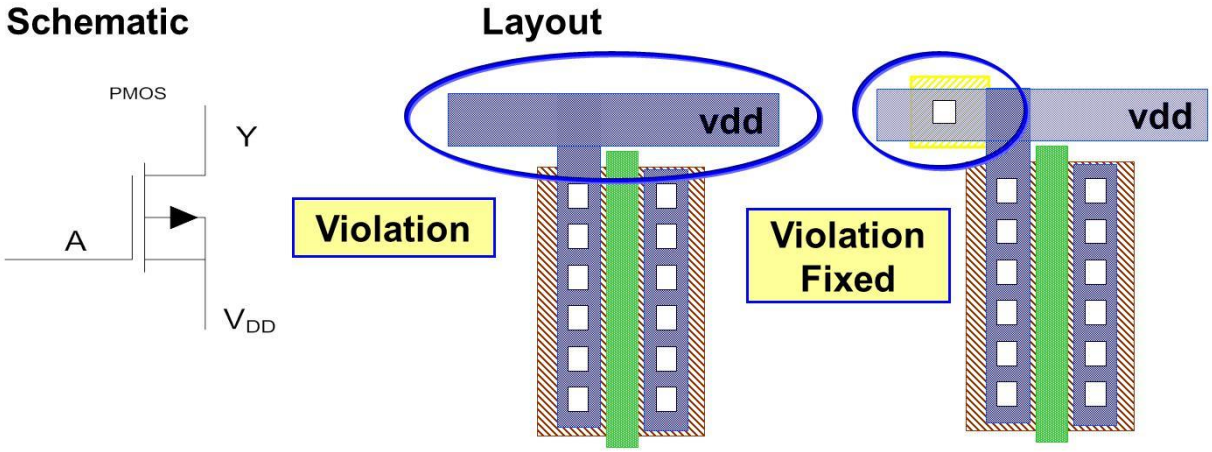






Physical Verification (ERC)

- Electrical Rule Check (ERC) is used to analyze or confirm the electrical connectivity of an IC design
- ERC checks are run to identify the following errors in layout
  - To locate devices connected directly between Power and Ground
  - To locate floating Devices, Substrates and Wells
  - To locate devices which are shorted
  - To locate devices with missing connections
- Well Tap connection error: The Well Taps should bias the Wells as specified in the schematics



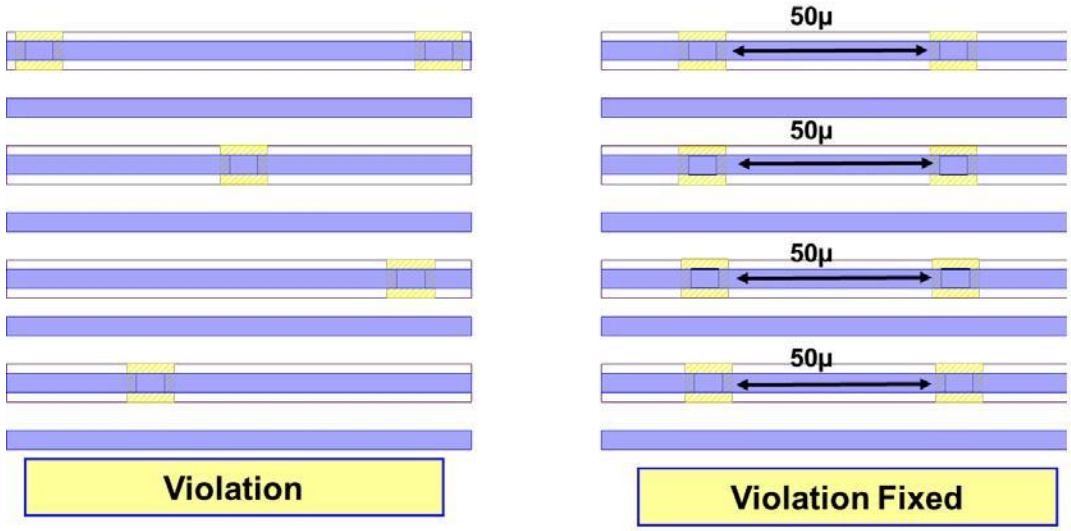
Courtesy: asicpd.blogspot.in

Physical Verification (ERC)

- Well Tap Density Error: If there is no enough Taps for a given area then this error is flagged
- Taps need to be placed regularly which biases the Well to prevent Latch-up

  e.g., In typical 90nm process the Well Tap Density Rule require Well-taps to be placed every 50 microns

- Tools: Mentor Graphics Calibre, Synopsys Hercules, Cadence Assura, Magma Quartz



DFM Checks

- Antenna Check (Gate-Oxide Integrity check)
  - Maximum net length restriction connected to Gate terminal
- Redundant Contacts/ Via
  - Multiple Via improves both Yield and Timing by resistance paralleling
- Metal Filling
  - Narrow Metal Layer separated from other Metal Layers may get high density of etchant than closely spaced wires
  - Over etched filling up empty tracks with metal shapes to meet Metal Density Rules
- Metal Slotting
  - Wide metal lines (Power Nets) expands significantly due to the high temperature during fabrication leads to destruction of the isolation and passivation layer that protect the wafer
  - To avoid it put slots or holes in these metal layers at regular intervals
  - Slotting also prevent the stress damage during wafer dicing and packaging

Formal Verification

- Formal Verification
  - Verify the two representations of circuit design exhibits same behavior
  - Checks the behavior of the Combinational Logics by checking the Compare Points
  - Targets implementation errors and not the design errors
  - Power checks: checks Power Switches/ Retention Cells/ Isolation Cells/ Level Shifters and all power connectivity
  - If any manual editing in the design then LEC has to be done at any point of time

- Formal Verification
  - Complete coverage
  - Effectively exhaustive simulation
  - Cover all possible sequences of inputs
  - Check all corner cases
  - No test vectors are needed

- Informal Verification (Simulation)
  - Incomplete coverage
  - Limited amount of simulation
  - Spot check a limited number of input sequences
  - Many corner cases not checked
  - Designer provides test vectors

Formal Verification

- Types of Formal Verification
  - Gate-level to Gate-level (Logical Equivalence Check after Routing)
    - To ensure that some netlist post-processing did not change the functionality of the circuit
  - RTL to Gate-level (after Synthesis)
    - To verify that the netlist correctly implements the original RTL code
  - RTL to RTL (before Synthesis)
    - To verify that two RTL descriptions are logically identical
- Logical Equivalence Check (LEC) will have two stages
  - Constrains setup stage
  - Logical Equivalence Check stage
- Tool will report equivalent/ non-equivalent/ abort/ not-checked
- Input Requirements
  - Netlists (.v)
  - Library (.lib and .lef)
  - Constraints (.sdc)
- Tools: Mentor Graphics FormalPro, Cadence Conformal, Synopsys Formality, Magma Quartz Formal

Parasitic Extraction

- Parasitic Extraction: Importance
  - Shrinking process geometries
  - New device structures
  - An increasing number of metal layers at each new process node
  - Much more closer nets at each new process node
  - Increasing wire aspect ratio of height to width
  - Increasing operating frequency
- Parasitic Capacitance can be reduced by using higher metals, provide spacing, shielding, Avoid parallel routing
- At higher clock frequencies, RC interconnect modeling is no longer adequate and inductance must be included in interconnect modeling
- Reluctance (Inductance) effect becomes more and more prominent as the resistance (both device and interconnect) decreases and the operating frequency increases

Parasitic Extraction

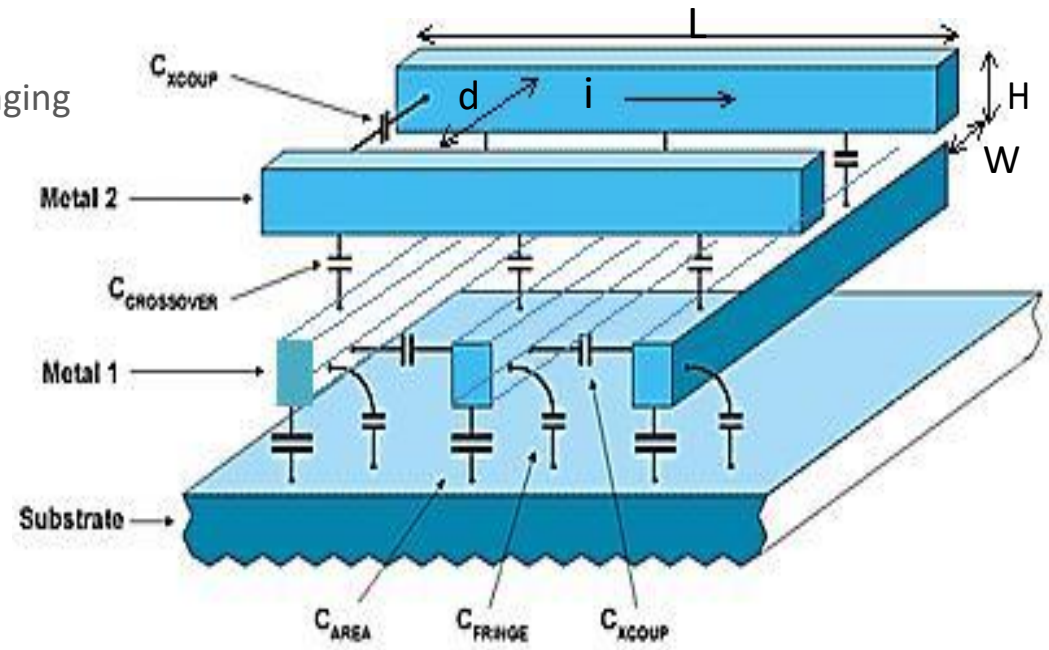
- Capacitance

  $C = \varepsilon_o W H/d$

  – Transistors
    - Depends on area of transistor gate, physical of materials, thickness of insulator, diffusion to substrate

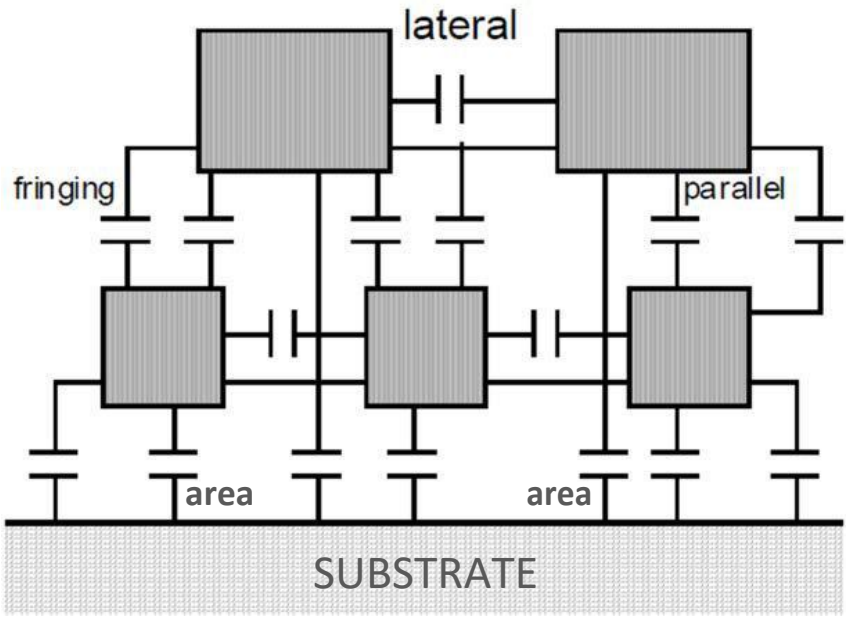
  – Poly to Substrate
    - Parallel plate and fringing

  – Capacitance between conductors
    - Coupling Capacitance
    - Area Capacitance
    - Fringing Capacitance
    - Crossover Capacitance



Parasitic Extraction

- Coupling Capacitance/ Lateral Capacitance
  - The capacitance between nets on the same Metal layer
  - Dominant over interlayer capacitances with every new process technology
- Fringing Capacitance
  - Capacitance between nets of different Metal layers and other layers due to Sidewall Capacitance
- Parallel/Crossover Capacitance
  - Capacitance between nets of 2 different Metal layers
- Area Capacitance
  - Capacitance between Metal layers and Substrate



- In modern processes, the width of interconnect wires at lower levels of metal is so small that the Fringing Capacitance of the wire is larger than the Area Capacitance

Parasitic Extraction

- Resistance

  R = ρ L/H W

  – Wire Resistivity

  – Complex 3D geometry around Vias

- Inductance

  – Self Inductance; $V = L\frac{di}{dt}$

  – Mutual Inductance, $M = K\sqrt{L_1 L_2}$

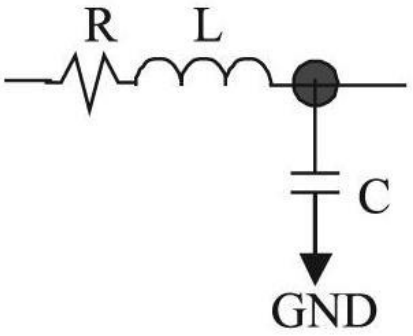
  – At high frequency Skin effect possibility

- Models used for Parasitic Extraction

  – Lumped-C, Lumped-RC, Lumped-RLC

  – Pi segment

  – Pin-to-pin delays are modeled by RC delays



Parasitic Extraction

- Sub-femto Farad accuracy required for extraction of designs at advanced technology nodes
- STA tool uses extraction data at fast corner while calculating hold and slow data while calculating setup to be pessimistic as possible, so that your chip doesn't fail after it comes back from the fab
- Common Extraction Formats: Standard Parasitic Format (SPF), Reduced Standard Parasitic Format (RSPF), Detailed Standard Parasitic Format (DSPF), Standard Parasitic Extraction Format (SPEF)
- Tools: Synopsys Star-RCXT, Cadence QRC, Mentor Graphics Calibre xRC

Timing Analysis

- Static Timing Analysis: Methodical analysis of a digital circuit to determine if the timing constraints imposed are met and to check the design is working properly
- Static Timing Analysis Flow
  - Read the inputs required
  - Setting up Constraints: IO Delay Constraints, DRVs, Timing Exceptions (False/ Multi-Cycle paths), Recovery and Removal, Minimum Pulse Width
  - Construct Timing Graph: Partition Clock Domain, Ideal/ Propagated Clock, Case Analysis
  - Propagation
  - Timing Report: End points with violations/ Paths enumeration
- Input Requirement
  - Routed Netlist (.v)
  - Libraries (.lib only)
  - Constraints (.sdc)
  - Delay Format (.sdf)
  - Parasitic Values (.spef)
- Tools: Synopsys PrimeTime, Cadence ETS, Cadence Tempus

Timing Analysis (SI)

- Signal Integrity (SI)
  - SI refers to the quality of the signal transportation during the circuit operation
  - In deep sub-micron the delays associated with the logic elements far outweighed delays associated with the interconnect
  - SI effects like Crosstalk (both noise and timing), Voltage (IR) Drop, Waveform Integrity and Electromigration have complex interdependencies
  - When the technology shrinks, the effect of coupling capacitance also increases
  - Crosstalk is the undesirable phenomenon, caused by the cross coupling capacitance between metal wires in a chip
  - Signal Integrity comes as an added feature of Timing Signoff tools
  - Crosstalk effects can be analyzed by enabling the SI switch in tools
  - If Crosstalk is enabled then the tool will by default do the timing in On Chip Variation (OCV) mode
  - Tool can read the .spef consists of coupling capacitance info.