Harshith Reddy Surakanti

8-Bit Manchester Adder Design Project Using Pass Transistors

Design Documentation and Analysis Report for Letni Corporation :

1. Project Objective:

We have designed an 8-bit Manchester adder using pass transistor logic. By employing pass transistors, we achieve lower power dissipation, a reduced transistor count, and a smaller area, while also minimizing propagation delay compared to traditional CMOS technology. The Manchester adder, being a parallel adder, enhances circuit performance by reducing propagation delay and increasing speed in comparison to a serial adder. Overall, this design offers a power-efficient, compact, and high-speed solution compared to conventional CMOS technology.

2. Key Specifications:

Transistor count:

208 transistors (26 Transistors for 1 bit Manchester adder)

Power dissipation (Info from second sample outputs) :

PreLayout : 10.319 uW
PostLayout :17.591uW

Propagation delay (Info second sample outputs) :

PreLayout: 131.124 pSec

PostLayout: 411.099 pSec

We were able to achieve less transistor count, less propagation delay, high speed Manchester Adder using pass transistors.

3. Design Specifications and Assumptions :

Clock specifications: Time period is 5 nSec and assume trise = tfall = 0.5nSec
Logic Family: Pass Transistors
Supply Voltage : 1.2 V

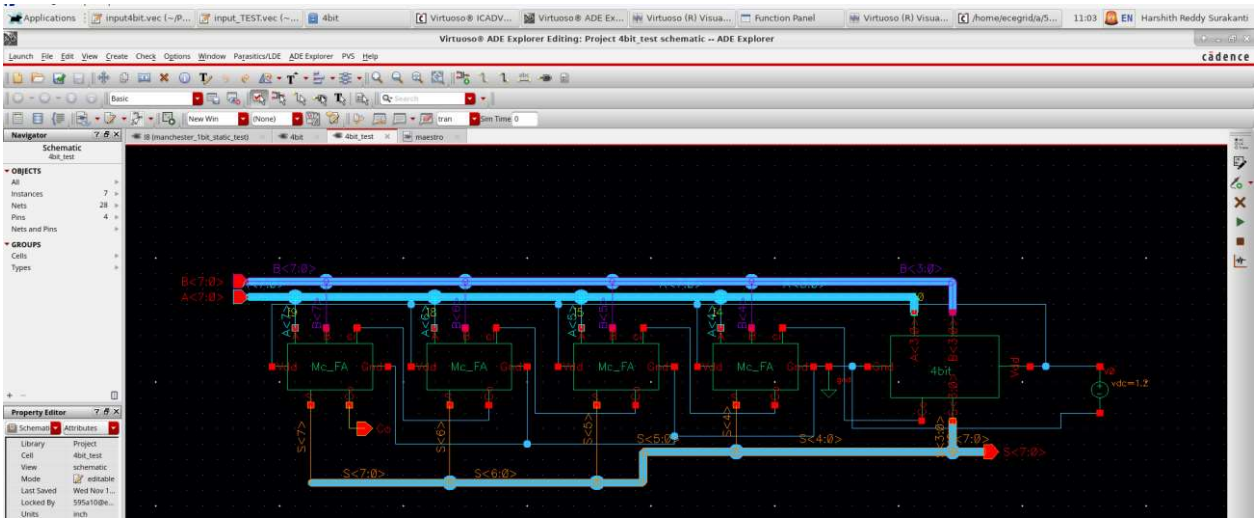
All Basic gates are designed using Pass transistors. The transistor count for all the gates used is mentioned below.

(Assuming complements are available, since I used common inverters for A and B inputs at high level hierarchy)

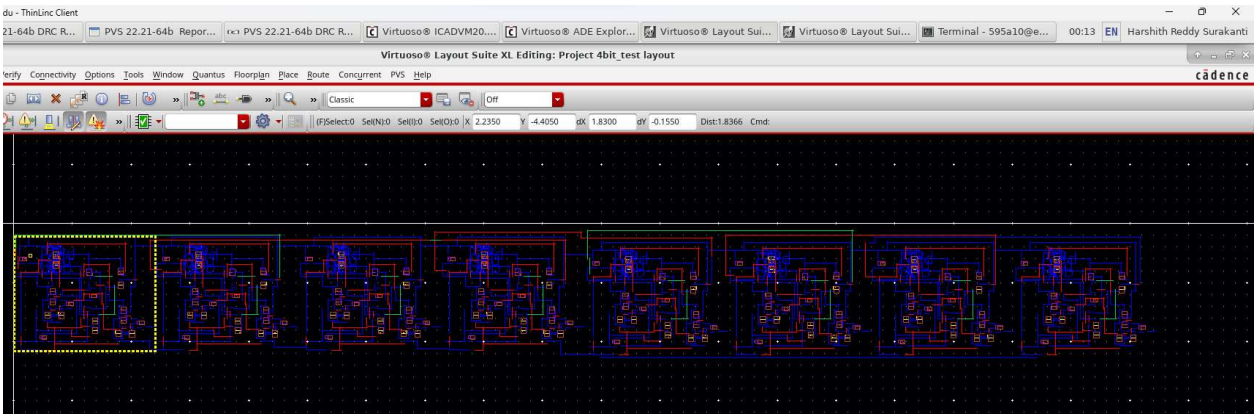
Gate	No.of Transistors Used
NAND	2
NOR	2
INVERTER	2
EX-OR	6

4. Circuit Implementation

8 bit Adder (4 individual bit + 4bit Adder) Schematic:



Layout of 8 bit Adder:



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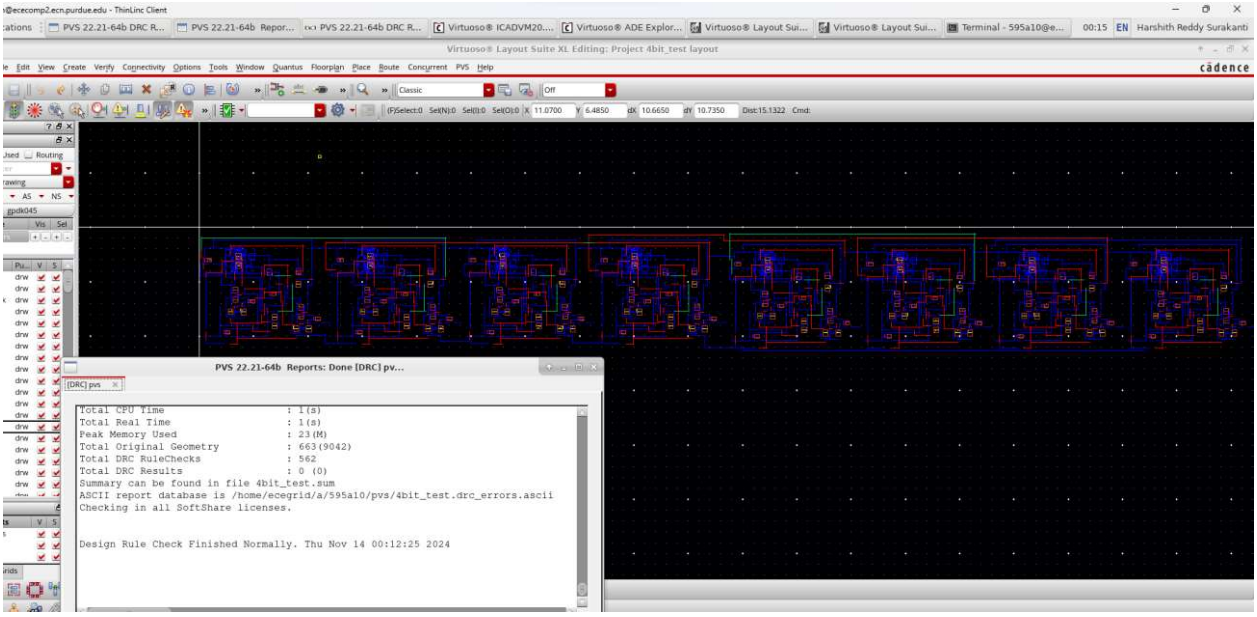
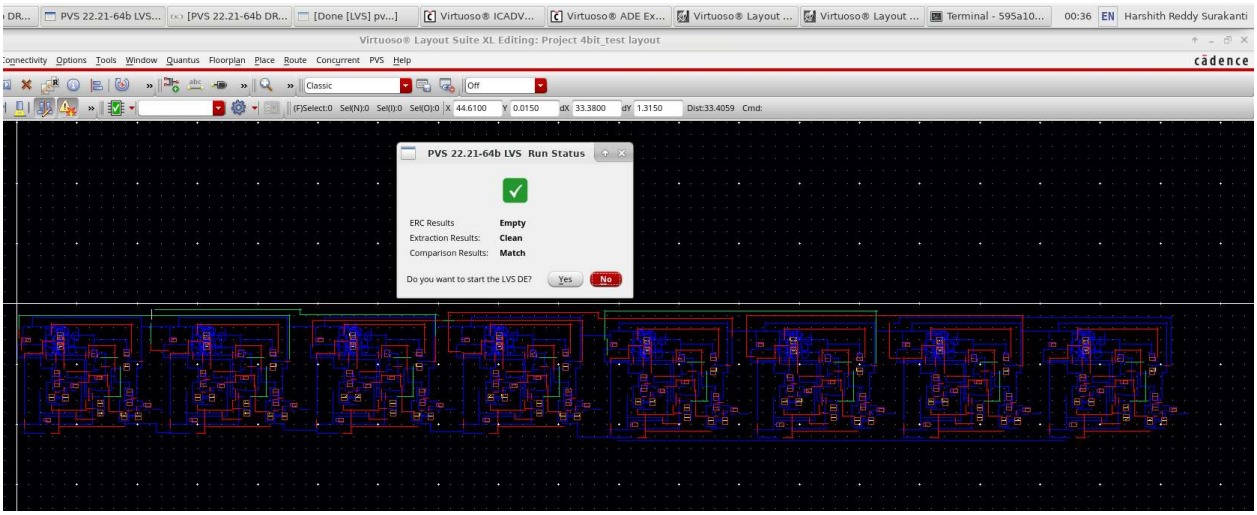
DRC Check:



LVS Check :



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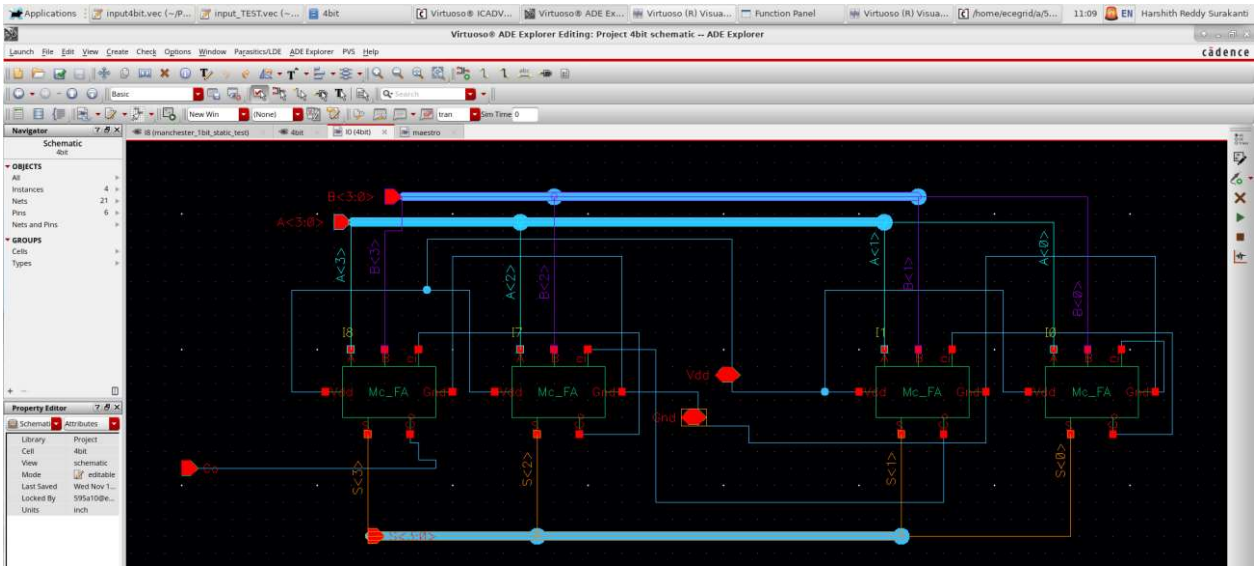
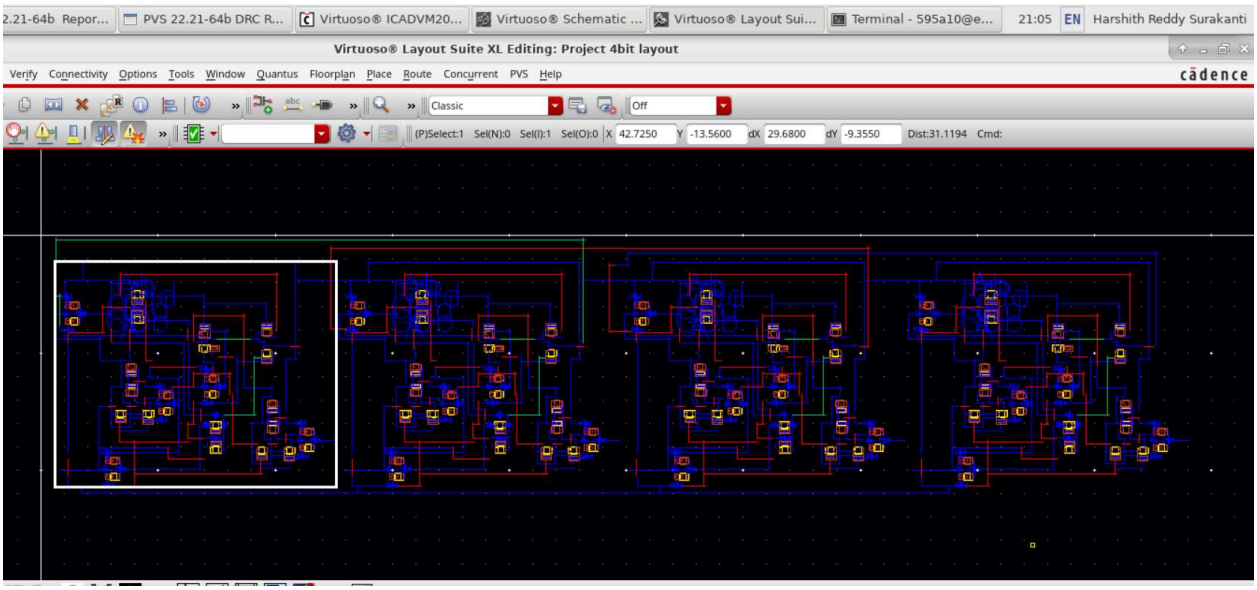
4bit Adder in the 8 bitAdder Schematic:



Layout of 4 bit Adder:



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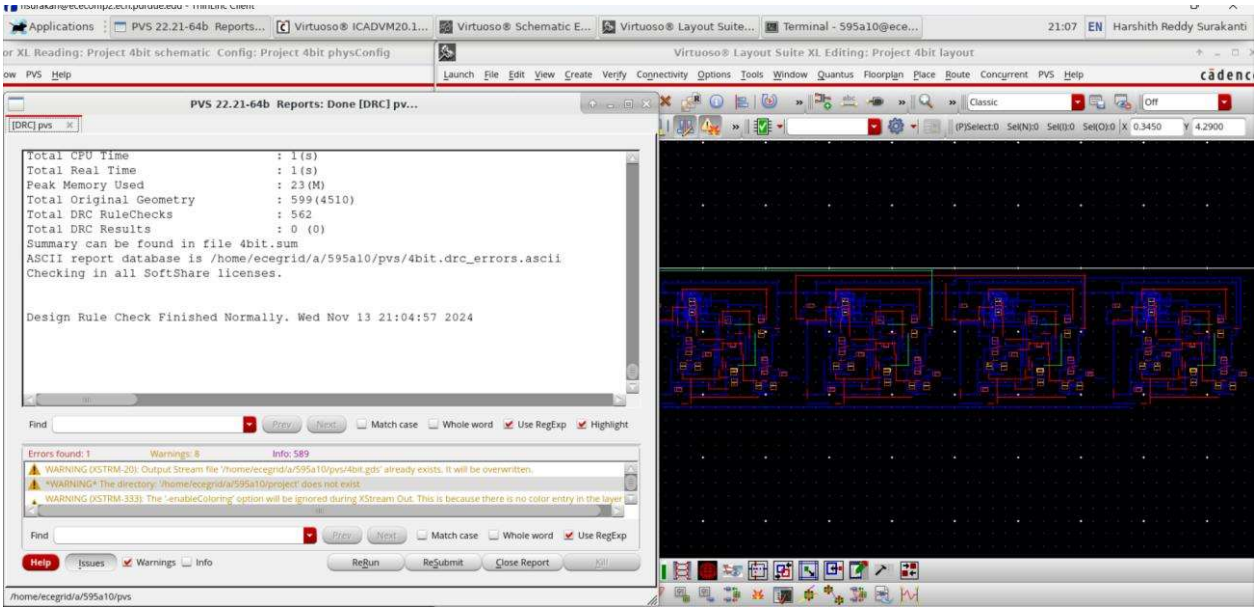
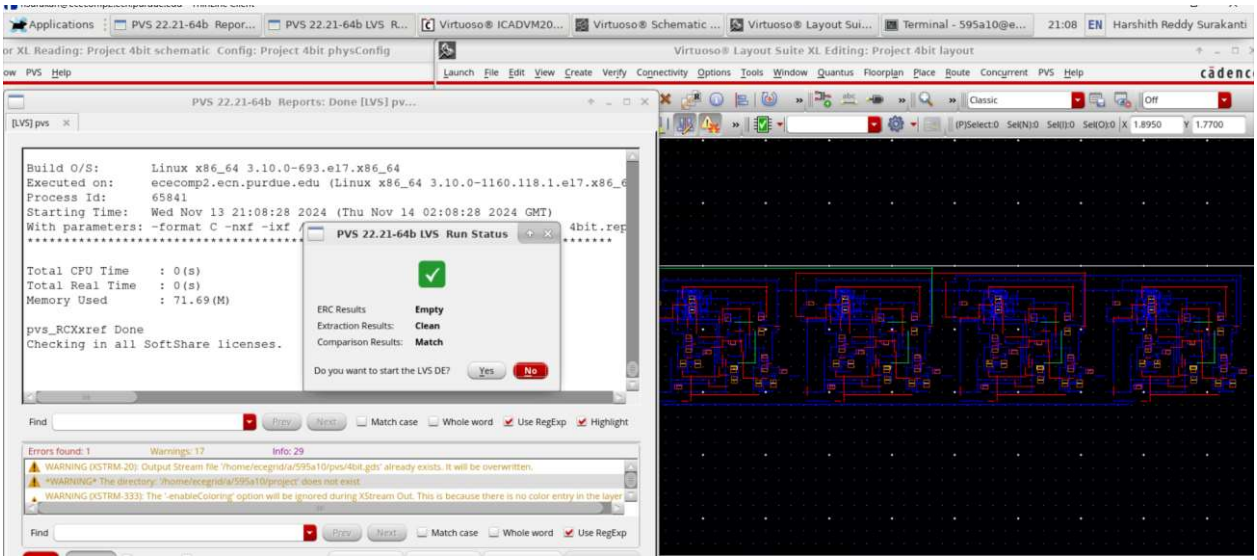
DRC check:



LVS Check:



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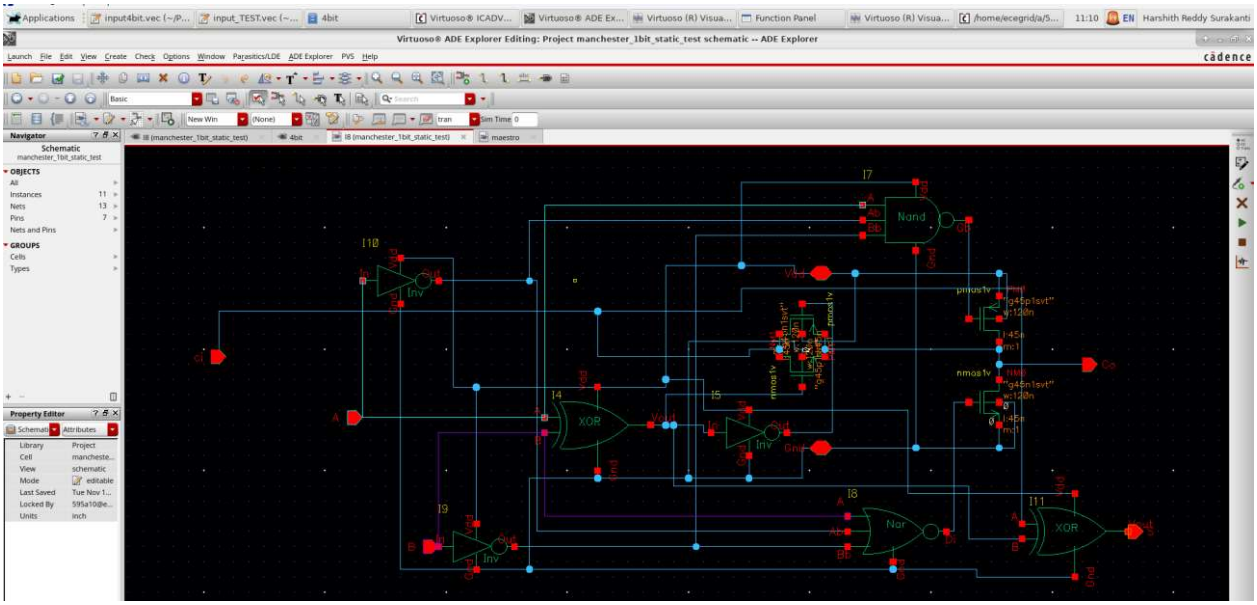
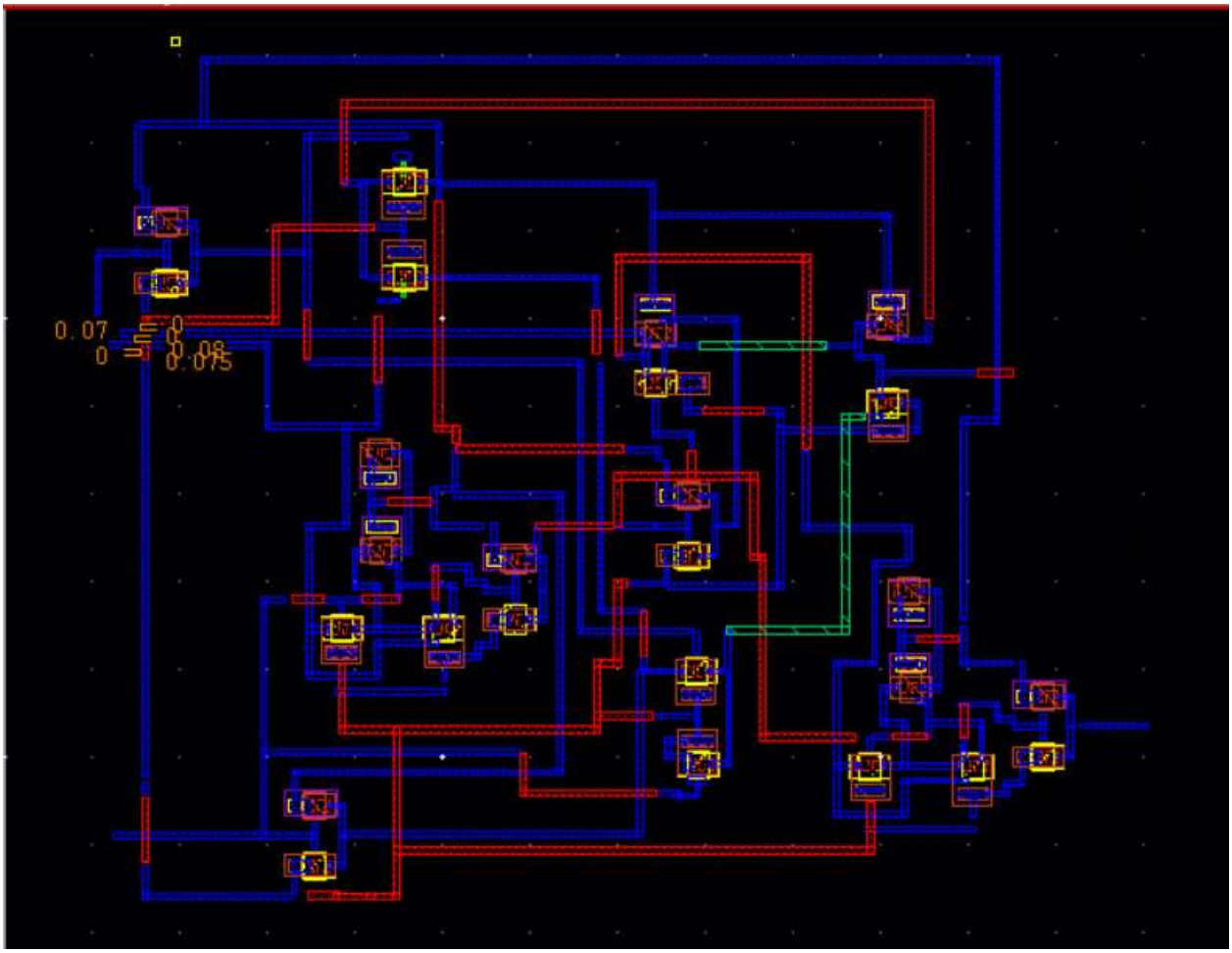
Individual bits schematic:



Layout:



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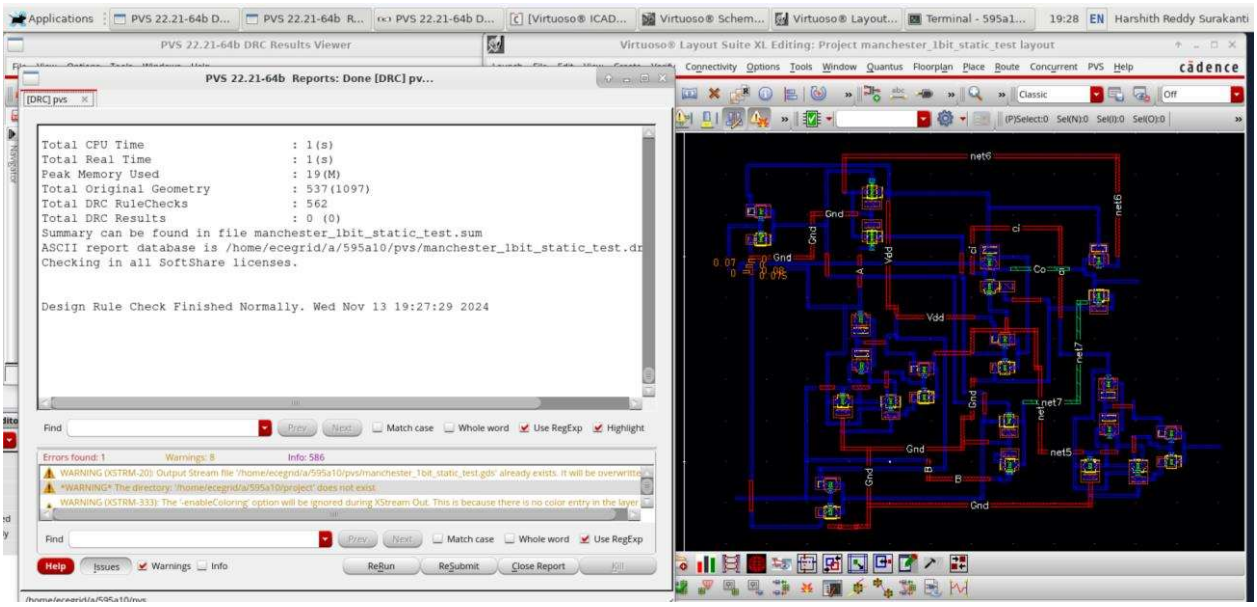
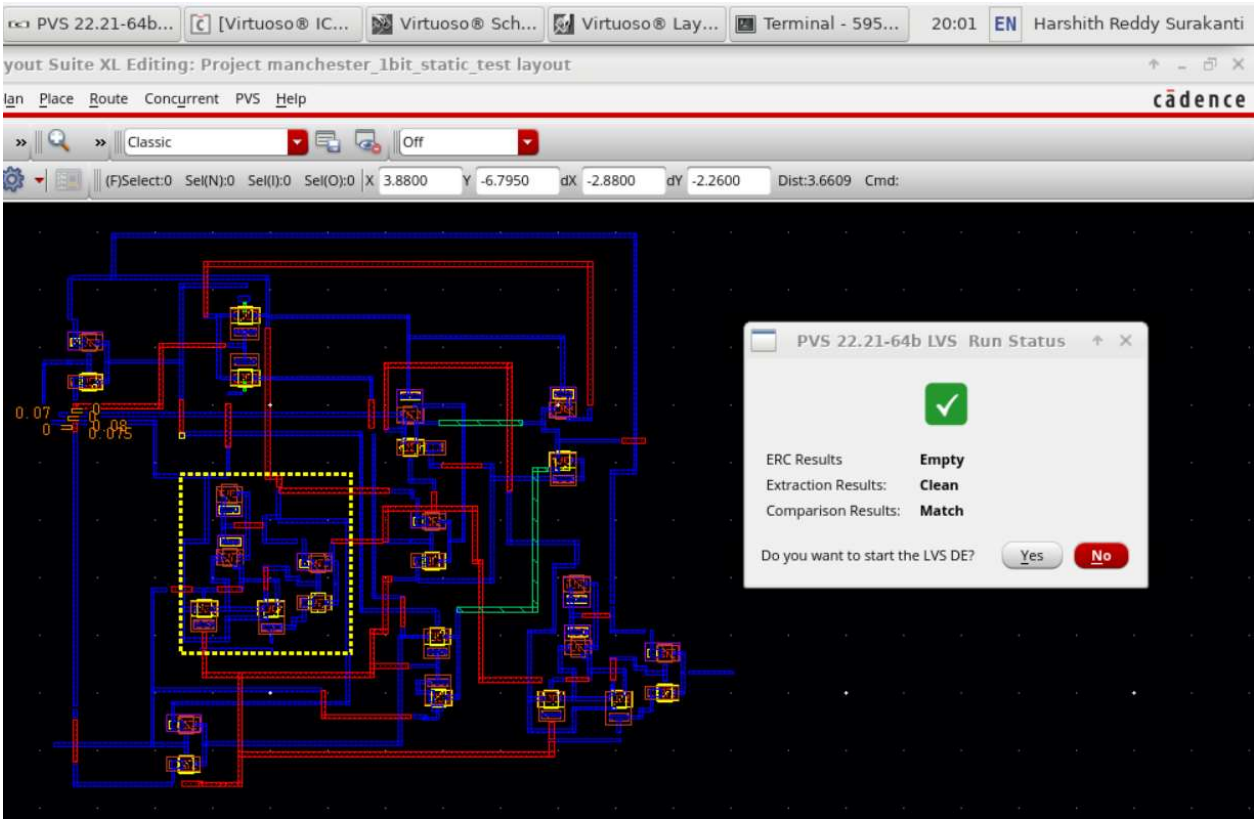
Layout and DRC Check 1bit:



Layout and LVS Check:



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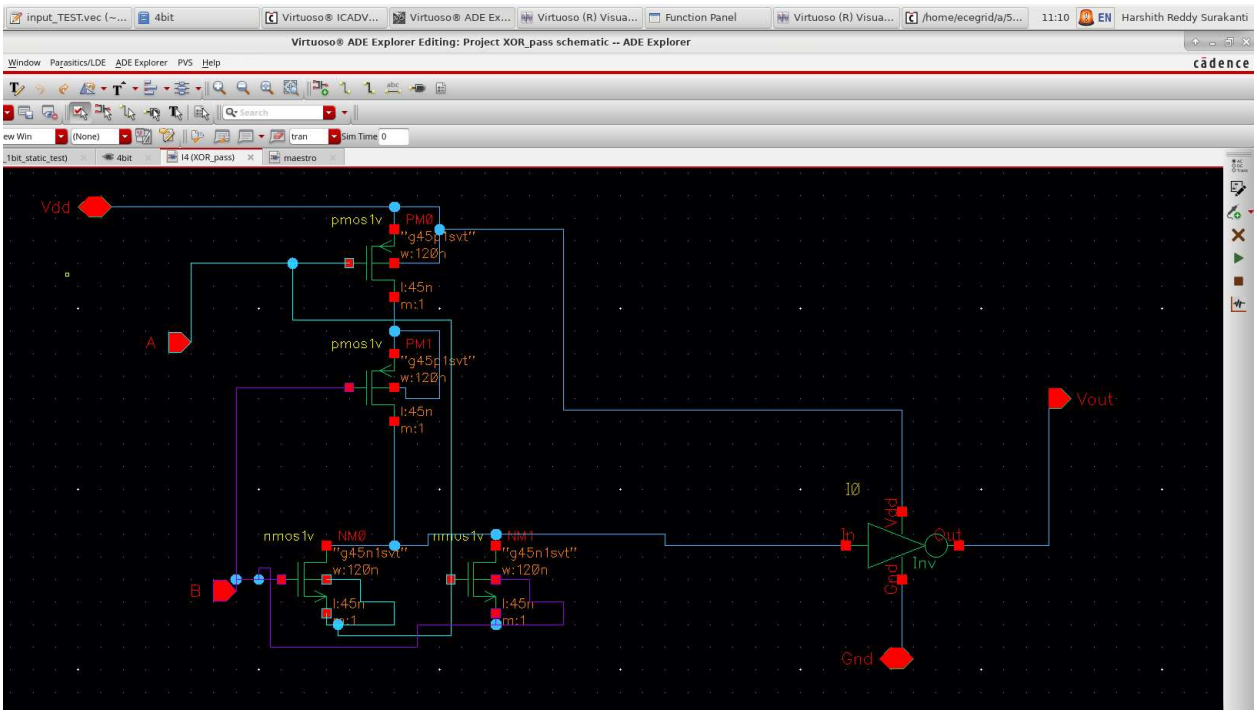
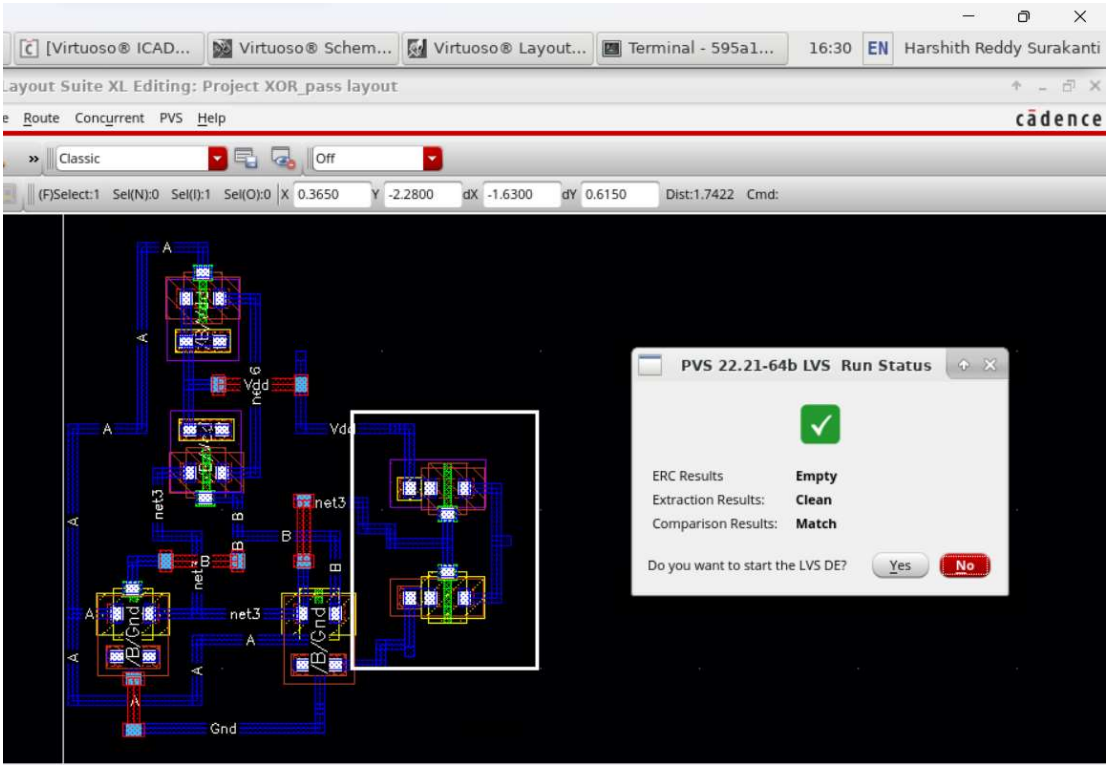
XOR using pass transistors:



Layout XOR and LVS check:



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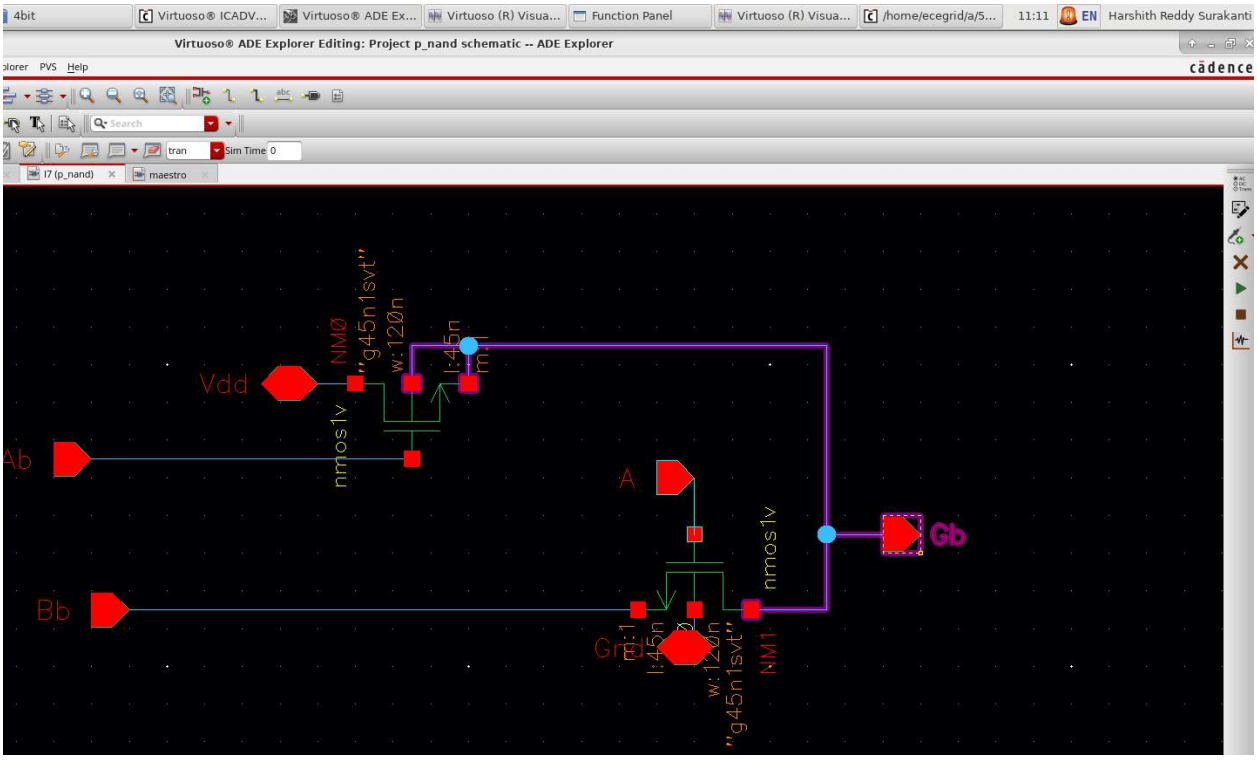
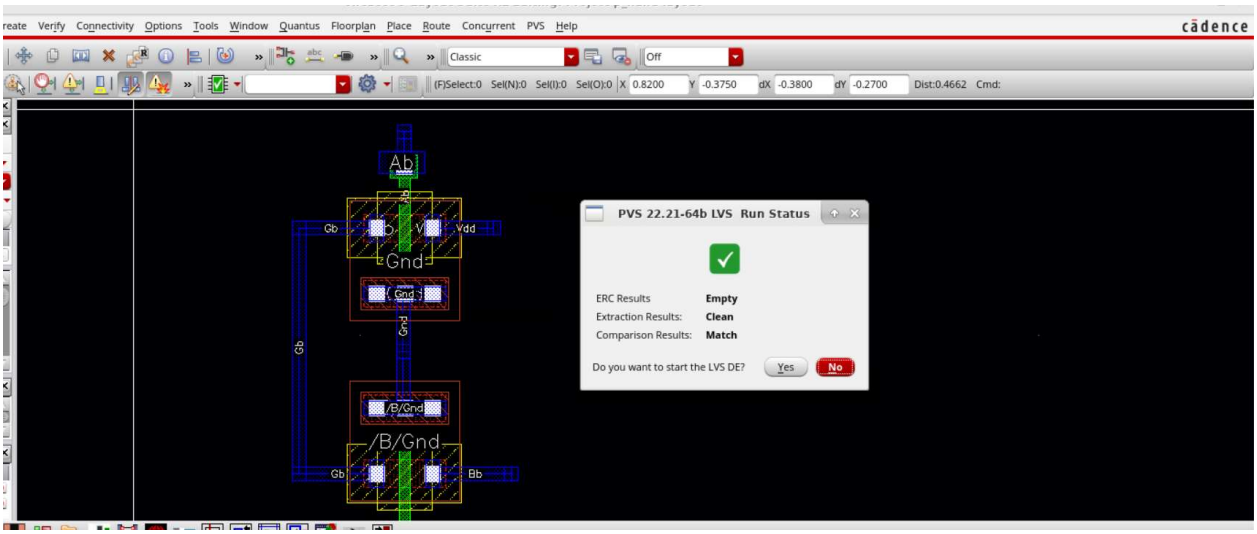
NAND using pass transistor :



LVS CHECK



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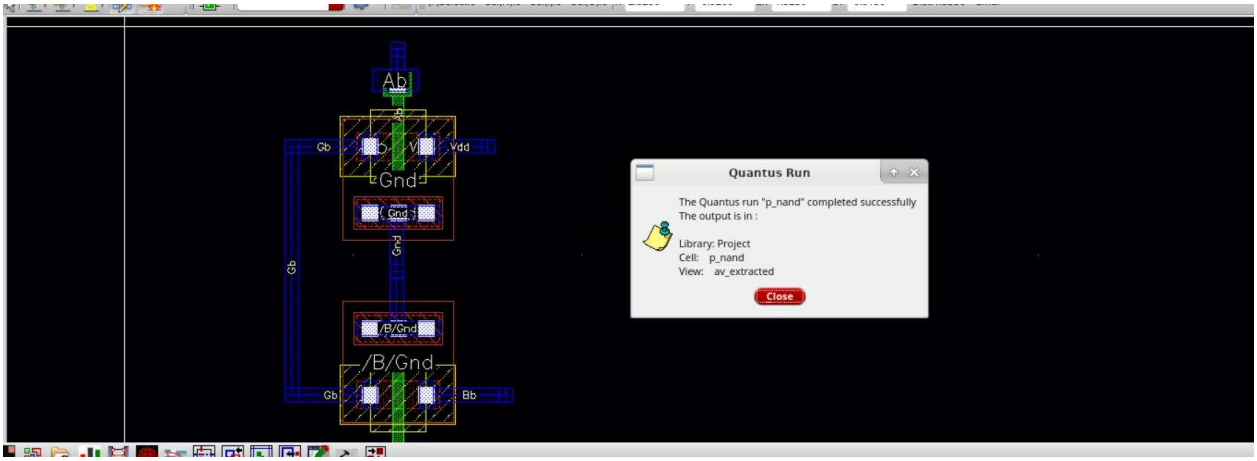
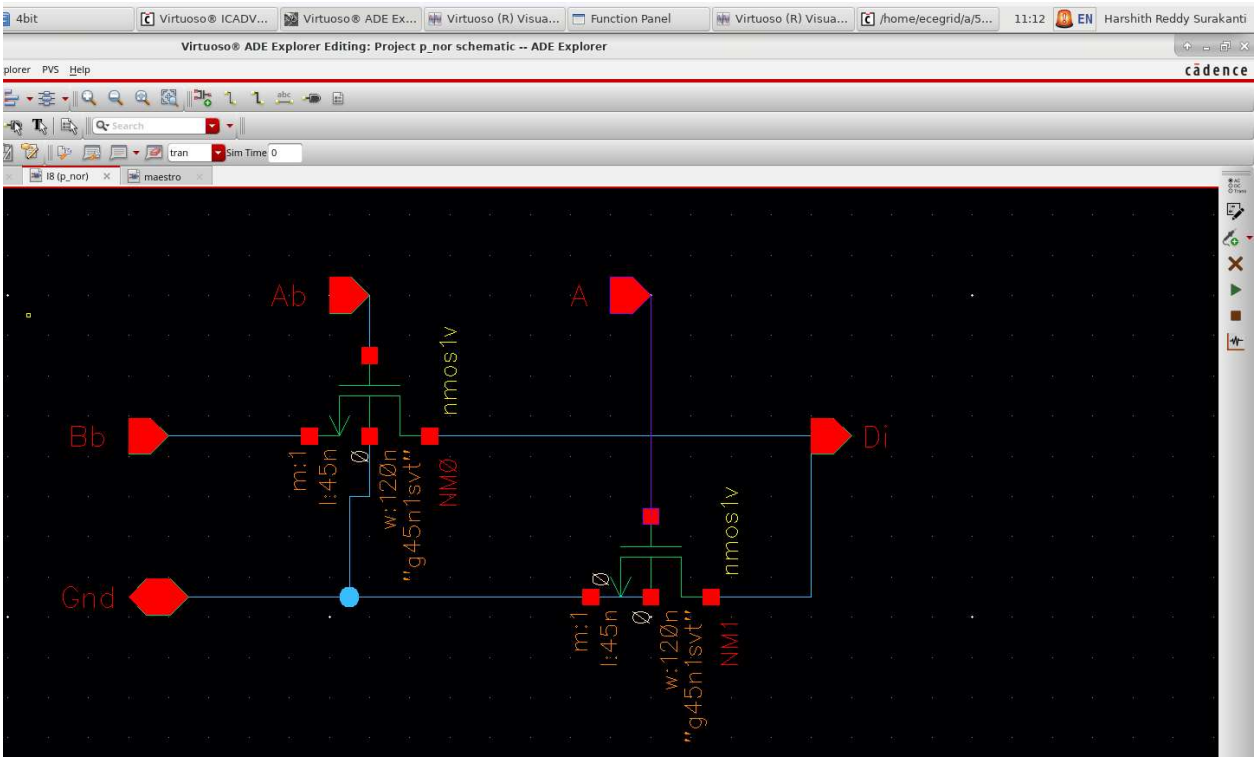
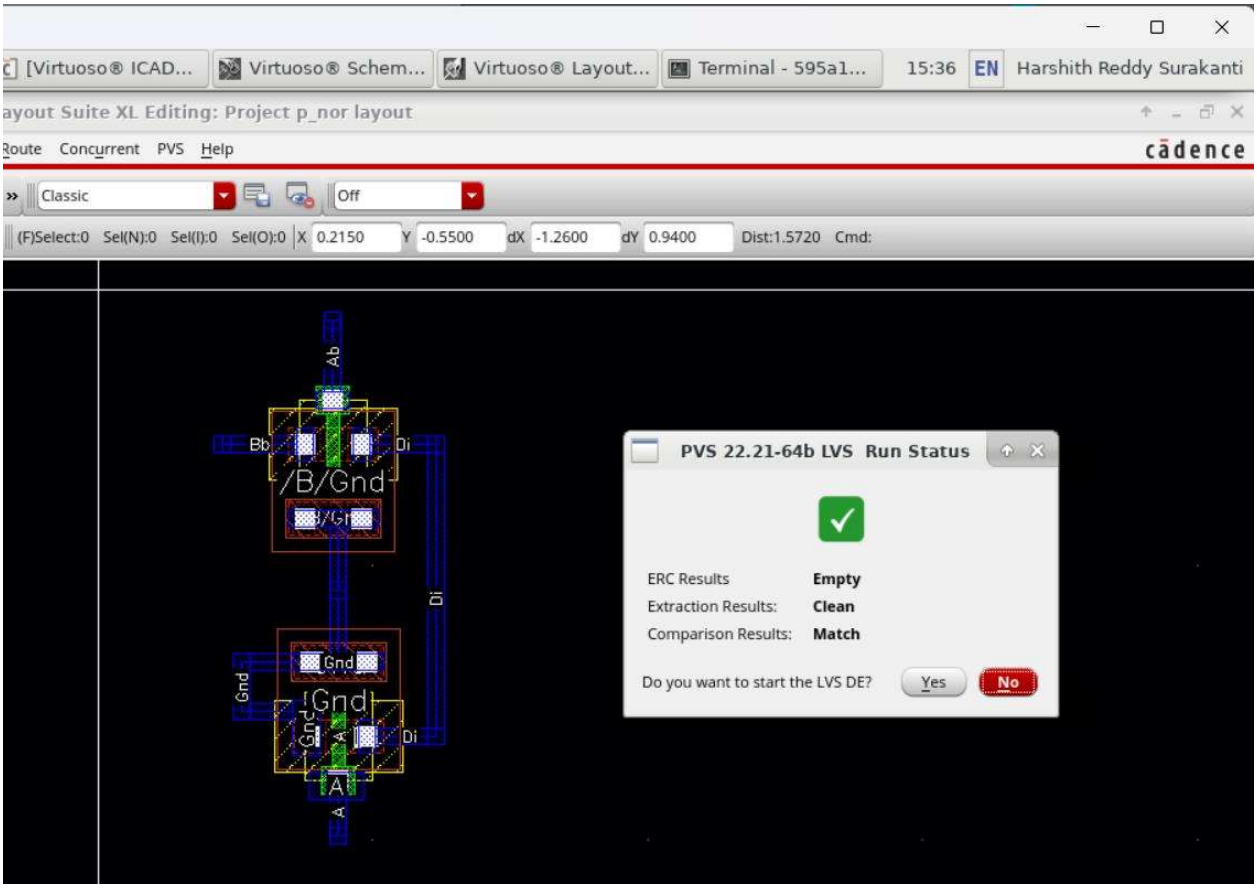
Quantus Extraction



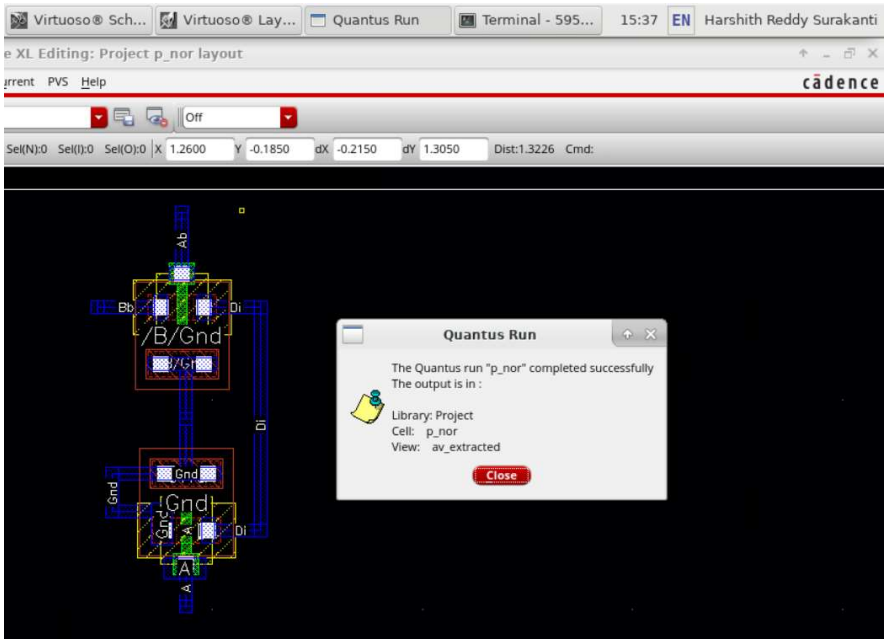
NOR using pass transistors:



LVS Check



Quantus Extraction



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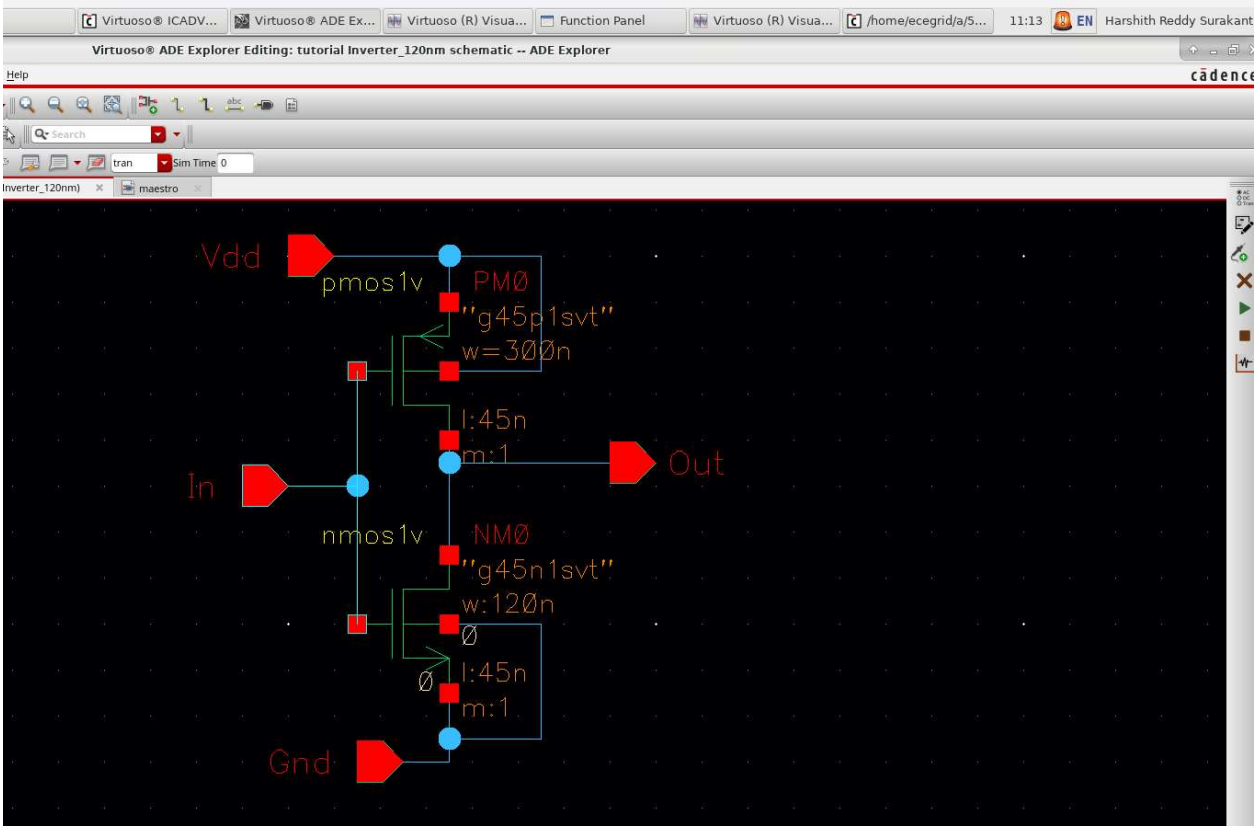
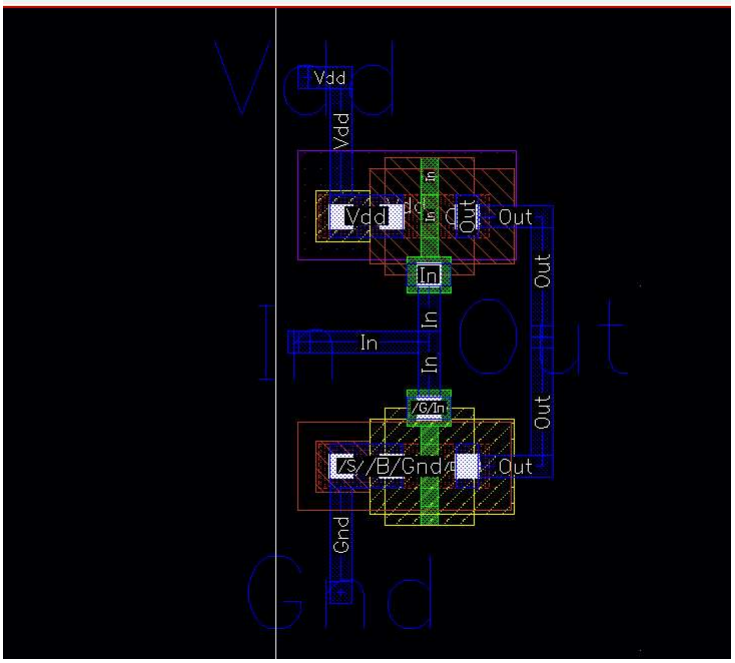
Inverter



Layout



5. PERFORMANCE ANALYSIS

To prove the Functionality of the design the following set of sample inputs are tested with time period 5nSec , trise=0.5nSec, tfall=0.5nSec and did transient analysis for 0- 50ns

A7-A0	B7-B0	S7-S0
BB	F5	B0
E9	3F	28
1F	49	68
F0	AF	9F
E5	C4	A9

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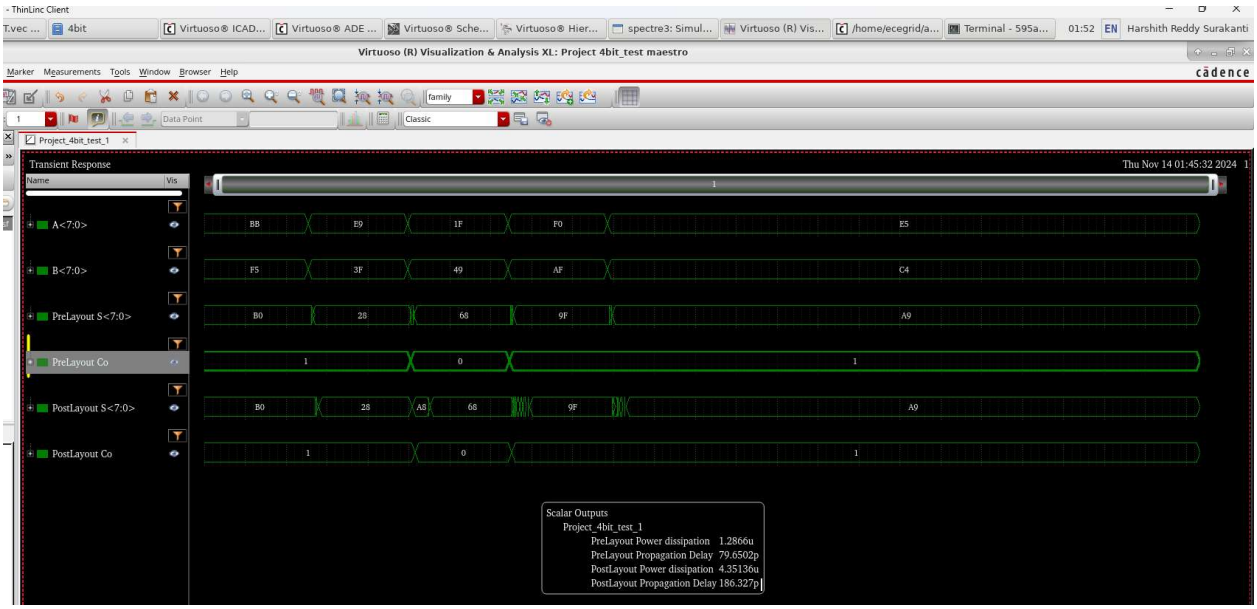
Output (Pre-Layout) :

Post Layout

Comparison between PreLayout and PostLayout



6. Power Dissipation

iii) Power calculated using power graph generated from transient analysis.

In Maestro , outputs > save all > check power signals to output (enable All checkbox)

In waveform, navigate browser > results >psf > trans >:pwr . plots the power waveform,

Now, waveform Data (getData(":pwr" ?result "tran")) is send to calculator and is averaged - average(getData(":pwr" ?result "tran")). Gives the power dissipation

Power graph is plotted below

Propagation delay and power dissipation provided as legend in the plot.

Power dissipation (from graph below) :

PreLayout : 10.319 uW
PostLayout :17.591uW

Power dissipation is almost doubled in postLayout simulation, the reason can be due to inclusion of Parasitic RC (Resistance & Capacitace) , real wire lengths, Real metal interconnects and more in post layout simulations

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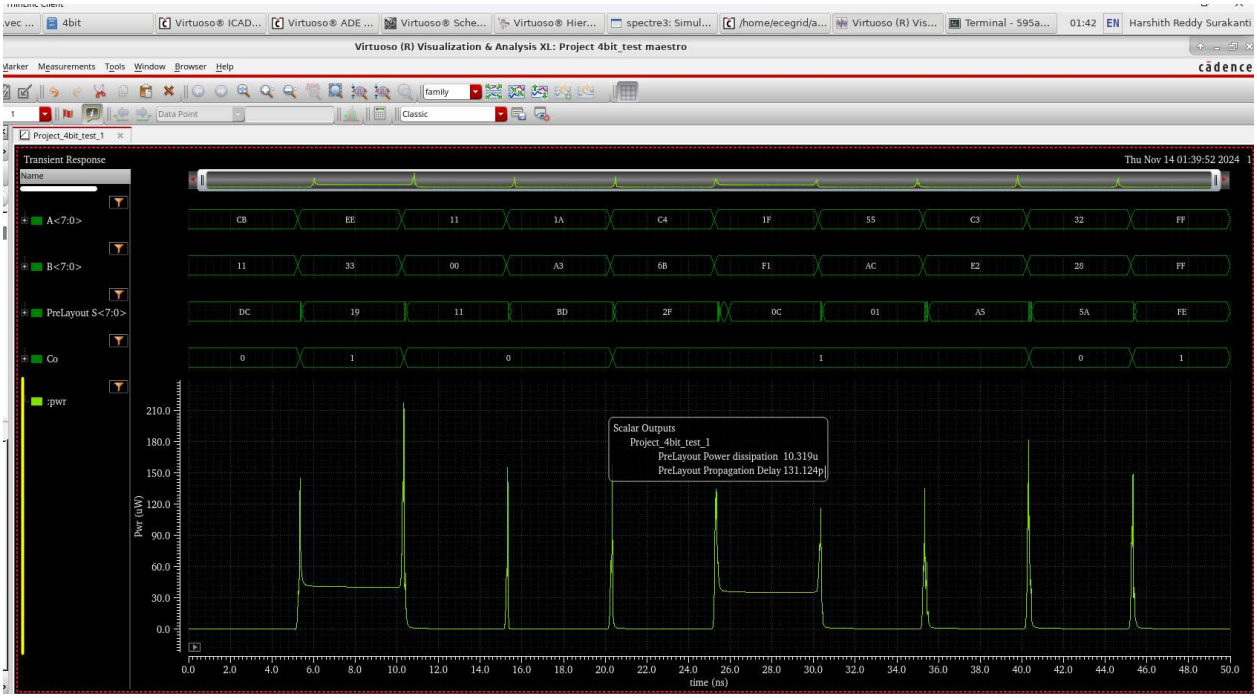
Pre-Layout Simulation graph



Post Layout simulation Graph and Power dissipation:

Comparison graph Pre and post layout simulations:

7. Adders Comparision :

	Brent Kung	Ladner Fischer	Han-carlson	Kogge-stone	Manchester Adder
Layout (wiring complexity)	Low	Medium	Medium	High	Low
Logic depth	5	4	5	4	5 (log2(3N)=log2(24)=5)
Fan-out	Low	Low	Medium	High	Low
Area	Low	Low	Medium	High	High

Input Vector file for simulation

Open *input_TEST.vec ~/Project/4bit Save

```
radix 44 44
io ii ii
vname A<[7:0]> B<[7:0]>

vih 1.2
vil 0
voh 1.2
vol 0
trise 0.5
tfall 0.5
period 5

; for Functionality check
;BB F5
;E9 3F
;1F 49
;F0 AF
;E5 C4

;for power calculation
CB 11
EE 33
11 00
1A A3
C4 6B
1F F1
55 AC
C3 E2
32 28
FF FF
```

Conclusion: **we** were able to achieve less transistor count, less propagation delay, high speed Manchester Adder using pass transistors compared to CMOS and high fan-out, high speed , power efficient when compared Parallel adders architectures mentioned above.