Design and Visualization of a MEMS 3D Capacitive Accelerometer Using PHIDL

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***Abstract*—This report presents the complete design, layout, and performance analysis of a MEMS-based three-axis capacitive accelerometer developed using PHIDL. Drawing inspiration from literature, particularly the work of Petsch et al., the structure integrates test features, spiral routing variations, and a layout optimized for manufacturability and mechanical performance assessment. The design includes key mechanical elements such as the proof mass, serpentine springs, and test structures. Electrode placement was deliberately omitted in this PHIDL-based implementation to concentrate on structural layout development and visualization.**

I. Introduction

MEMS capacitive accelerometers have found their importance in different domains, from the electronic industry to automobiles and medical devices. Their popularity is due to their several advantages, starting from their compact size, low power consumption, and ability to detect motion along multiple axes by tracking changes in capacitance.

This report focuses on the layout design of a three-direction accelerometer using PHIDL, a Python-based tool for creating MEMS and photonic layouts, which in turn can generate GDS files used in later fabrication steps. The design was motivated, and structural parameters were derived from the work of Petsch et al., whose contributions and research helped define the sensing approach and fabrication methodology in a better and more complete way .

In this paper we have visualized various spiral layouts to assess route choices and design viability, focusing on layout density and connection variations. The final structure includes essential mechanical components such as serpentine springs, a perforated proof mass, capacitor fingers, and a test structure that functions as a structural prototype for assessment. The project focuses on layout generation in PHIDL, intentionally excluding electrode placement to maintain emphasis on structural modeling and visualization and hence avoiding electrical complexity.

II. Working Principle of 3D MEMS Accelerometers

A MEMS capacitive accelerometer detects movement in three directions, that is, in the x, y, and z axes, by measuring changes in capacitance that happen when a suspended weight moves.

- **X/Y direction sensing:**This design uses interdigitated comb fingers. The shift or change in capacitance occurs When the device experiences lateral acceleration, the proof mass shifts sideways, changing the overlap area between movable and fixed fingers.
- **Z diretcion sensing:** Between the proof mass and a fixed electrode beneath it, a parallel plate capacitor forms. A vertical acceleration causes the proof mass to shift, altering the gap between the plates and, consequently, the capacitance.

The change in capacitance from the action is turned into an electrical signal by a readout circuit, allowing us to detect acceleration in all three directions.

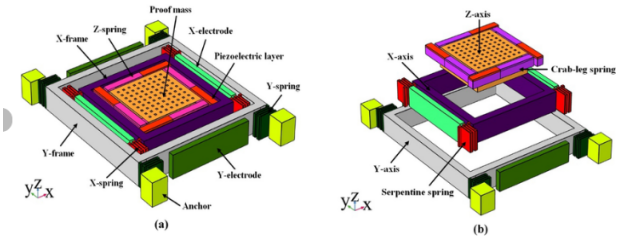

Fig. 1: Schematic of 3D MEMS capacitive sensing principle

A. Advantages

- Low power consumption
- High sensitivity and linearity
- CMOS compatibility
- Compact 3D motion detection

III. Detailed Fabrication Process

The fabrication of the MEMS accelerometer draws strong inspiration from the detailed work by Petsch et al. (ASEE 2012), who implemented a Silicon-on-Glass (SOG) approach to realize a three-axis capacitive MEMS sensor.

A. Detailed Process Used by Petsch et al.

1) **Glass Wafer Preparation:**
   - Borosilicate glass wafer coated with chromium.
   - Chromium patterned via photolithography.
   - HF etches 3 µm recess into the glass.
2) **Bottom Electrode Formation:**
   - Cr/Pt deposited by e-beam evaporation.
   - Lift-off used to leave patterned electrodes.
3) **Silicon Wafer and Anodic Bonding:**

- 100 µm thick silicon device wafer used.
- Anodic bonding at 350°C to seal glass and silicon.

4) **Top-Side Metallization:**
   - Cr/Au pads deposited on silicon surface.
5) **DRIE Etching:**
   - Structures (springs, proof mass, fingers) formed.
6) **Final Inspection:**
   - Photoresist stripped.
   - SEM and optical inspections performed.

- **Double-SOI Substrates:** Enable true symmetric sensing in the Z-direction and improved mechanical stability for stacked devices.
- **Polymer-Based Bonding (e.g., BCB):** Low-temperature bonding alternatives using benzocyclobutene help reduce thermal stress during wafer stacking.
- **Vacuum-Sealed Packaging:** Modern packaging techniques seal the MEMS cavity at ¡ 0.1 Pa, significantly improving the Q-factor and reducing air damping.
- **Integrated CMOS Readout:** On-chip signal processing improves the signal-to-noise ratio and reduces parasitic effects from long traces.
- **Glass-in-Silicon Reflow:** Used for low-profile electrodes and high-density wafer-level packaging.

The motto of these upcoming new and advanced methods is to overcome limitations in fabrication, alignment accuracy, and sensing linearity while still building on the proven Petsch-based platform. We could extend our current design to incorporate these technologies in future iterations and research.

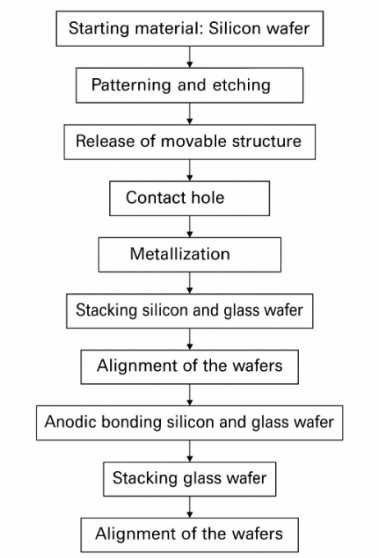

Fig. 2: Flowchart of Petsch-based SOG fabrication process

IV. Device Structure Description

Note: While the structural elements such as the proof mass, springs, and fingers were modeled in detail, electrodes were intentionally omitted in this design stage to streamline fabrication feasibility analysis and ensure a clearer evaluation of mechanical layout constraints.

The MEMS accelerometer designed in this project features a compact and symmetrical structure laid out over a 2000 µm × 2000 µm die area. The device was modeled and scripted using PHIDL with reference to structural dimensions and design methodology from Petsch et al., and further enhanced with design variation studies and manufacturability considerations.

A. Key Structural Elements

- **Proof Mass:** The central proof mass measures 395 µm × 395 µm and is perforated with 49 square damping holes (7 × 7 array). These holes reduce air damping in Z-axis motion and aid in etch release.
- **Springs:** Four serpentine springs (each with 4 turns) suspend the proof mass from the surrounding anchors at the corners. They define the mechanical response and resonant frequency.
- **X/Y Axis Sensing:** Interdigitated capacitor fingers (200 µm × 10 µm) extend from the movable proof mass toward fixed anchor fingers. Lateral motion changes the overlap area, modulating capacitance.
- **Z Axis Sensing:** A parallel-plate capacitor is formed between the bottom surface of the proof mass and a fixed Cr/Pt electrode recessed in the glass substrate. Vertical displacement alters the gap, and thus the capacitance.
- **Damping Holes:** Openings in the proof mass improve out-of-plane responsiveness and reduce squeeze-film damping.
- **Bond Pads:** A total of 12 bond pads are provided for external interfacing. They are distributed across the layout to connect to fingers, springs, and electrodes.

B. Layout Overview

The overall layout is designed with symmetric anchors, well-separated sensing structures, and integrated test elements. It enables clean routing, DRC compliance, and expandability for advanced testing.

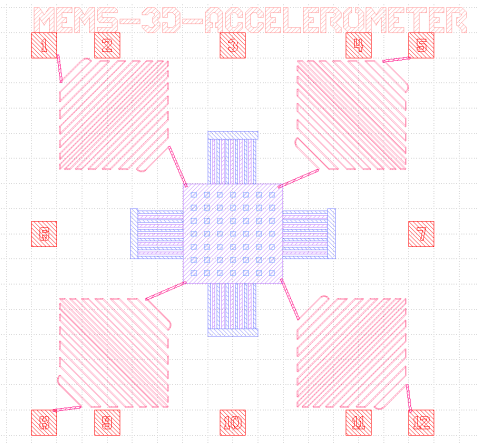

Fig. 3: GDS layout of the accelerometer structure

V. Design Variations in MEMS Accelerometer

To study the impact of spiral routing complexity and layout coverage on manufacturability, four models were developed with varied turn count and coverage area in each quadrant.

A. Model 1: 11 Turns, 50% Area Coverage

This model introduces a simple 11-turn spiral occupying half of the corner routing area. It maintains moderate complexity and ensures adequate separation between traces.

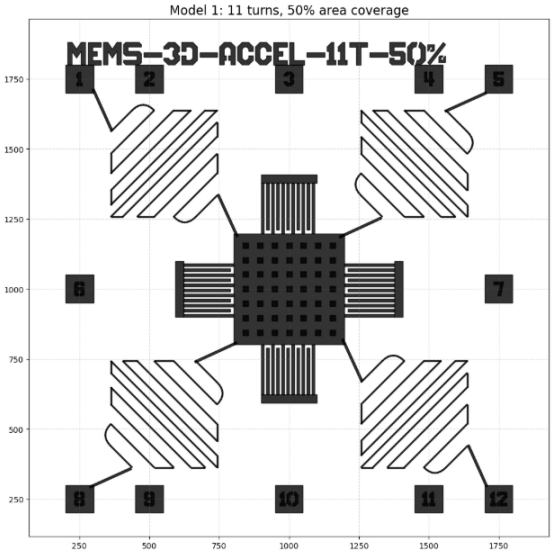

Fig. 4: Model 1: 11-turn spiral, 50% area coverage

B. Model 2: 22 Turns, 50% Area Coverage

Model 2 increases the routing density while keeping the same layout footprint as Model 1. This helps evaluate how finer pitch spirals impact DRC constraints and signal interference.

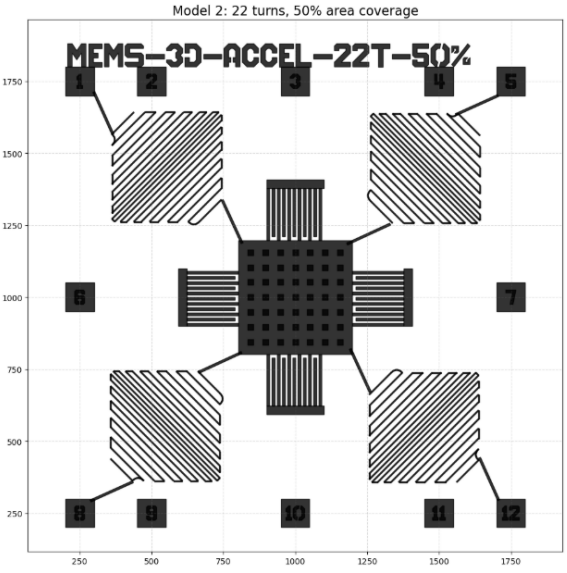

Fig. 5: Model 2: 22-turn spiral, 50% area coverage

C. Model 3: 11 Turns, 100% Area Coverage

The third model expands the same 11-turn routing into the entire quadrant, reducing density while allowing full spatial use. It balances complexity and layout space utilization.

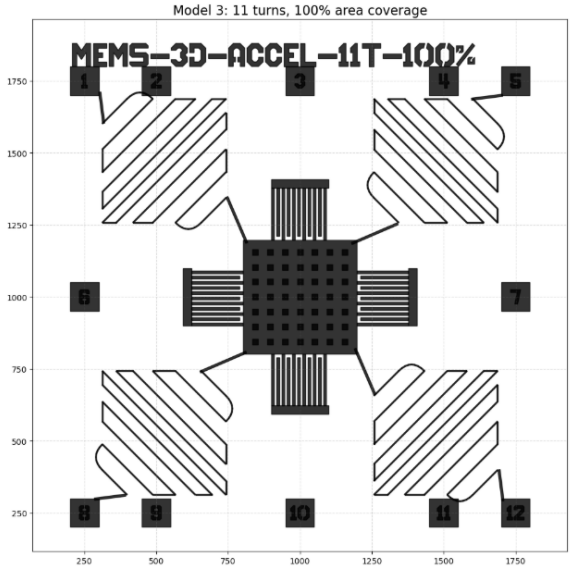

Fig. 6: Model 3: 11-turn spiral, 100% area coverage

D. Model 4: 22 Turns, 100% Area Coverage

This model represents the most complex case, combining high turn count and full area usage. It is useful for evaluating metal fill density and maximum trace complexity.

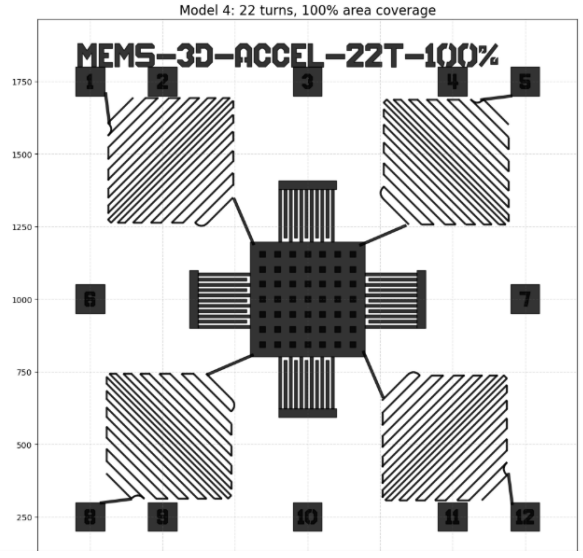

Fig. 7: Model 4: 22-turn spiral, 100% area coverage

E. Improved Model: 30 Turns, 100% Area Coverage

This improved version, based on the attributes of Models 3 and 4, features comprehensive quadrant coverage with 30-turn spirals. Engineered to minimize overlap infractions and

maintain trace uniformity, it is intended for optimal routing density. This model simulates the most challenging yet feasible routing scenario for complex MEMS integration.

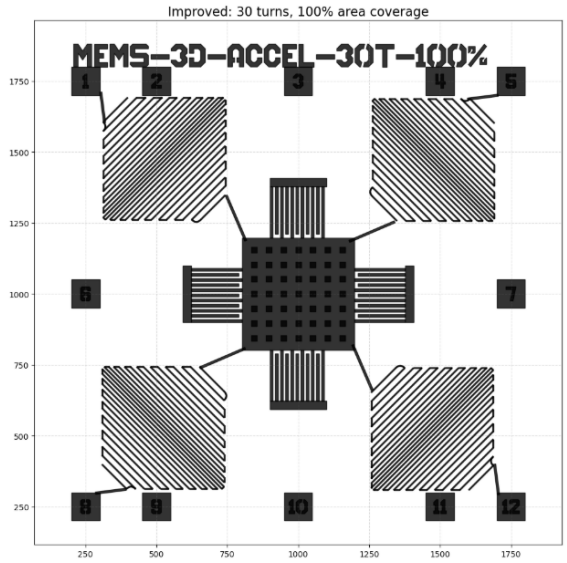

Fig. 8: Improved Model: 30-turn spiral, 100% area coverage

These layout changes significantly affected how we understand trace scalability, DRC limits, parasitic interactions, and the feasibility of integration in MEMS design.

VI. Test Structures in MEMS Accelerometer Design

To validate fabrication consistency and layout performance, multiple test structures were included across the chip and test blocks.

A. Serpentine Spring Test Structures

We used isolated spring patterns with varying turns (11, 22, 30) to evaluate the mechanical robustness and quality of DRIE etching.

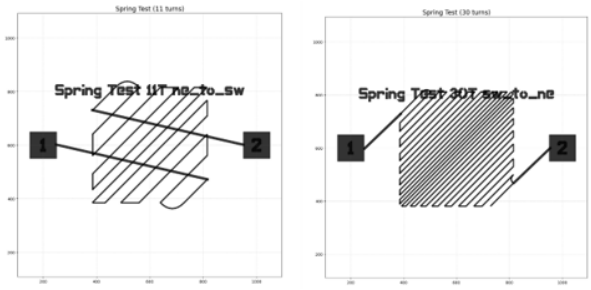

Fig. 9: serpentine Spring patterns

B. Comb Finger Capacitor Test Arrays

Interdigitated comb capacitor test arrays were added to verify lateral alignment, critical dimension control, and parasitic capacitance measurements.

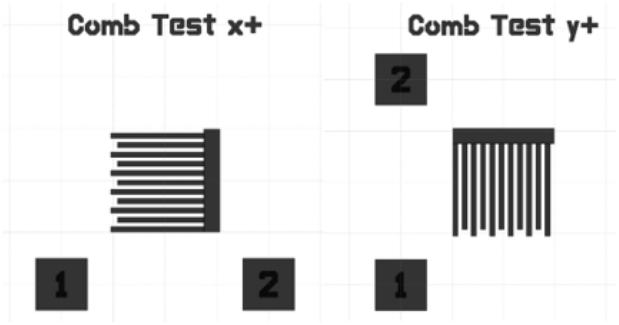

Fig. 10: interdigitated finger capacitor

C. Alignment Marks and CD Test Structures

Specially placed alignment crosses and line-space patterns were used to:

- Ensure proper mask alignment between layers.
- Confirm minimum feature sizes using CD (critical dimension) patterns.
- Enable inspection under optical and SEM tools.

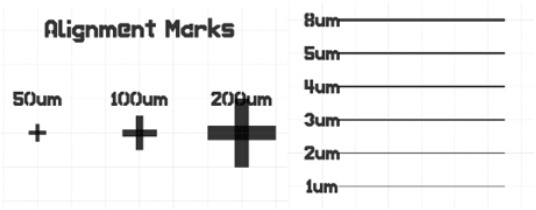

Fig. 11: Alignment marks and CD features

D. Integrated Test Chip Overview

To allow thorough investigation without compromising the main sensor zone. A test chip area has various test structures, including spirals, springs, and capacitive components.

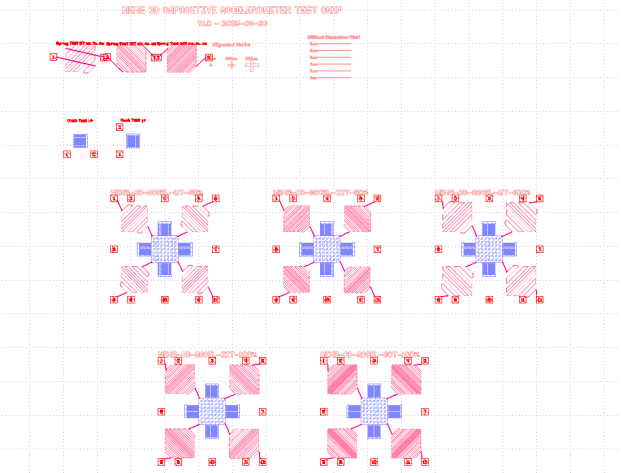

Fig. 12: Combined GDS layout of the test chip region

E. Test Structure Summary Table

TABLE I: Summary of Test Structures and Their Purposes

Test Structure	Purpose
Serpentine Springs	Check etch depth, pattern fidelity, and mechanical reliability.
Comb Fingers	Validate finger spacing, measure parasitic capacitance, and detect lateral shift.
Alignment Marks	Ensure proper alignment of lithographic layers.
CD Patterns	Confirm minimum feature size and dimensional tolerance post-etch.
Test Chip Region	Centralized test area to evaluate process outcome and calibration.

VII. Performance Analysis

A. 1. Capacitance Estimation

X/Y: 701 fF Z-axis: 303 fF

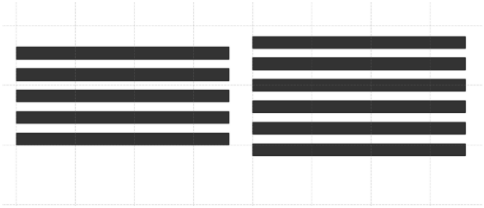

Fig. 13: Comb geometry used for capacitance model

B. 2. Sensitivity

$\Delta C = \frac{\varepsilon_0 A}{d-x} - \frac{\varepsilon_0 A}{d}$

Sensitivity 15–30 fF/µm

C. 3. Resonant Frequency

$f_r = \frac{1}{2\pi}\sqrt{\frac{k}{m}}$

Expected 2 kHz

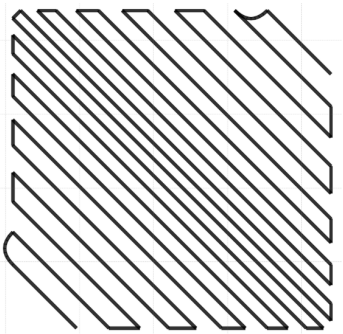

Fig. 14: Spring model influencing resonant frequency

D. 4. Mechanical Considerations

- Stress at spring bends
- Damping holes for squeeze-film control

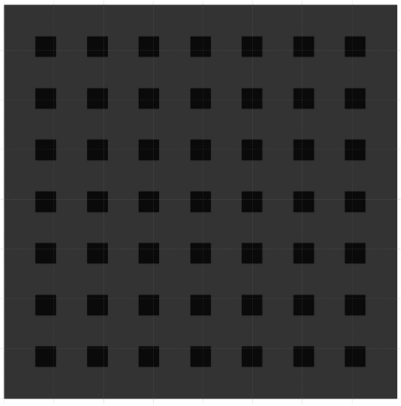

Fig. 15: Damping holes in proof mass for airflow

E. 5. Summary

- Range: ±5g
- Resolution: ¡1µg
- Bandwidth: 0–1.5 kHz
- Capacitance variation: 200 fF

Conclusion

The design is motivated by Petsch et al.'s ideas and visualization uses PHIDL structural layout. we created a various type configuration with mechanical components including the proof mass, serpentine springs, interdigitated capacitor fingers, and testing support structures.

Various spiral routing methods were tested to see how trace complexity, layout density, and quadrant coverage affect routing. Recent revisions have emphasized MEMS layout development trade-offs between area efficiency and design rules.

We have not considered electrodes while visualizing or writing code to simplify PHIDL modeling and design, concentrating on mechanical construction. Our method eliminates the need for electrical modeling to evaluate layout aspects.

This project provides a fundamental foundation for PHIDL-based MEMS layout development and analysis. Electrode design, CMOS integration, and fabrication receptivity can improve performance of the device.

References

- Petsch, K., and T. Kaya. "MEMS 3D Capacitive Accelerometer Design." ASEE, 2012.
- B. J. Baliga. Fundamentals of Power Semiconductor Devices, Springer, 2008.
- COMSOL, PHIDL, and LNF process documentation.