NARROW BAND
CMOS LOW NOISE AMPLIFIER DESIGN

EC384:RF Mini Project Report
submitted by

Harshitha S

under the guidance of
Dr Sandeep Kumar

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA
SURATHKAL, MANGALORE - 575025

November 29, 2020

ACKNOWLEDGEMENT

We are highly indebted to Dr Sandeep Kumar for allowing us to work on this captivating project, ‘Narrow Band CMOS Low Noise Amplifier Design’ under his able guidance and for being the motivation behind this project. We would like to thank Dr Sandeep Kumar for his valuable and timely inputs in developing the project.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Chapter 1

1.1. INTRODUCTION

One of the most important building blocks of radio frequency systems is Low Noise Amplifier. Low noise amplifiers (LNAs) play a key role in radio receiver performance. The low noise amplifier is a particular type of electronic amplifier used in communication systems, which amplifies very weak signals captured by an antenna. A proper LNA design should provide a minimum noise figure (NF). Moreover, it should also deliver a significant gain to minimize noise contribution of the subsequent stages and to amplify the attenuated signal received by the antenna so that it can be efficiently handled by the following stages (mixer, VGA, etc.).

1.2. MOTIVATION

Due to the growing demand for wireless transceivers, much attention has been paid to the design of high-performance RF and microwave circuits. MOS devices are considered slow and noisy, but as the benefit of technology scaling, the transistor's cutoff frequency continues to increase which is desirable to improve the noise performance of the CMOS circuits. So, CMOS circuits might be capable of replacing GaAs/BiCMOS/bipolar circuits in some RF circuit designs. CMOS technology also has advantages in the integration of RF building blocks due to its low cost and a high degree of functionality in a single chip.

1.3. OBJECTIVE

The main objective of this project is to learn the basics of Advanced Design System (ADS) and to implement the Narrowband LNA design topologies involving cascade and cascode Amplifier stages. The goal is to achieve a gain greater than 20dB and Noise factor less than 2dB. Along with these, it's very important to make sure that LNA provides a specific input impedance of 50 ohms to terminate the transmission line which delivers the signal from the antenna to the amplifier. A good input match is even more critical when a pre-select filter precedes the LNA because such filter is often sensitive to the quality of the terminating impedance. Our LNA design focuses on high gain, input matching, lowest noise figure, high linearity, and low power consumption.

CHAPTER 2

2.1. LNA TOPOLOGIES

Common−source, common−gate, and cascode are the three prevailing LNA topologies.

2.2. COMPARISON OF LNA TOPOLOGIES

Characteristics	Common-Source	Common-Gate	Cascode
Noise Figure	Lowest	Rise rapidly with frequency	Slightly higher than CS
Gain	Moderate	Lowest	Highest
Linearity	Moderate	High	Potentially Higher
Bandwidth	Narrow	Fairly Broad	Broad
Stability	Often requires compensation	High	High
Power Supply	Greater	Lesser	Lesser

Table 1: Comparison of LNA topologies

The cascode amplifier is the most versatile of these three topologies. It provides the most stable signal gain over the widest bandwidth with only a slight sacrifice in noise figure performance. The common−source transistor is sized to deliver the best possible noise figure, but that advantage often comes at the cost of greater sensitivity to bias, temperature, and component tolerances. The common−gate amplifier also has a low noise figure (particularly at lower frequencies), but the noise figure increases rapidly with signal frequency. The high drain−source capacitance in common−gate implementations requires inductive feedback, which serves to improve noise figure, gain, and stability at higher frequencies.

Chapter 3

3.1 DESIGN METHODOLOGY OF LNA

The following flow chart describes the steps followed to design low noise amplifier:

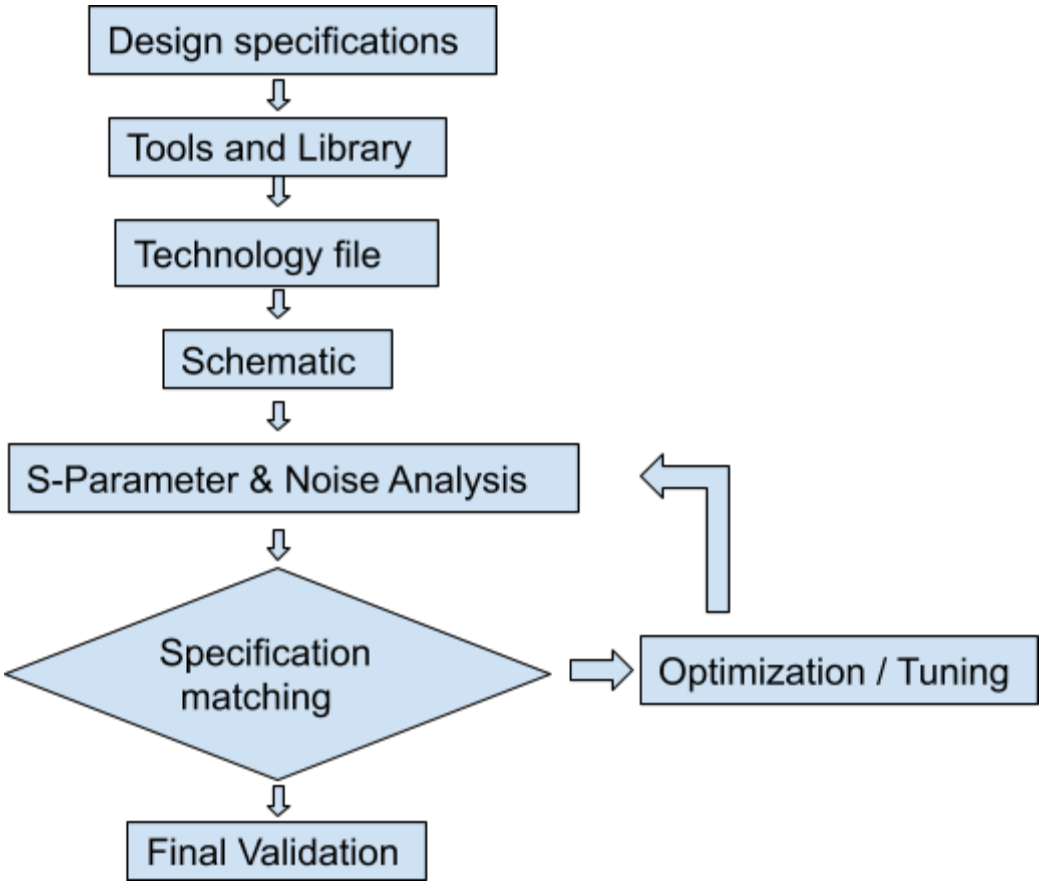

Figure. 1. Flow chart of project design

3.2. SPECIFICATIONS

Parameter	Specification
Frequency	2.5 - 3 GHz (S-Band)
Noise Figure	< 2 dB
Gain	>20 dB
Load Impedance	50 ohms

Table 2. Specifications

3.3. TOOLS & LIBRARIES

We have used Advanced Design System (ADS), which is the world's leading electronic design automation software for RF, microwave, and high-speed digital application. There are several libraries available in this tool. For our requirement, we have used RFlibrary.

3.4. TECHNOLOGY FILE

This is a very important step of the project because the MOSFET model parameters are dependent on its respective technology defined parameters. It is necessary to pick the feature size in which design is to be done and that technology file has to be imported to the ADS workspace. We wanted to design in 65nm feature size, so we downloaded the BSIM4 65nm level 54 technology file from the Predictive Technology Model (PTM) website and then imported it in our design.

3.5. DESIGN 1: INDUCTIVE DEGENERATED COMMON SOURCE LNA

To begin with ADS, we designed an inductive degenerated common source LNA.

3.5.1. SCHEMATIC:

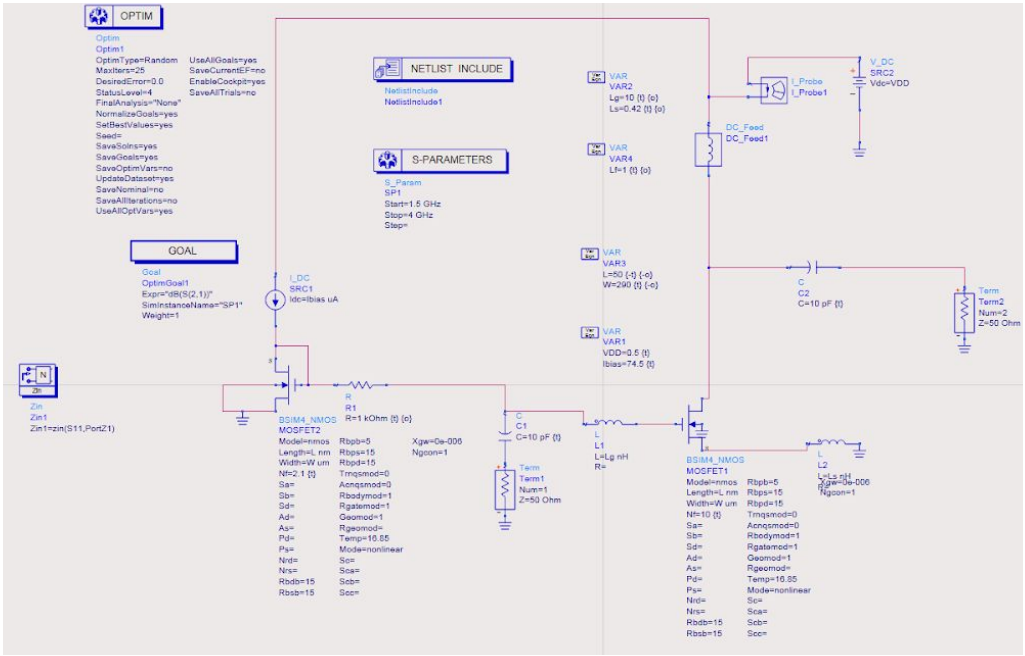

Figure 2: Schematic of common source LNA

The above schematic shows a common source LNA biased using the current mirror. The power supply of 0.5 V is used. Inductor Lg and Ls are used for the purpose of matching source resistance with that of input impedance Zin of MOSFET. Practically, the output is considered at the drain of Mosfet which is, in turn, an input to the mixer.

3.5.2. DESIGN AND ANALYSIS

We used a current mirror circuit to bias the MOSFET of inductively degenerated LNA. The most important task of LNA design is matching source resistance (Rs) to the input impedance of NMOSFET., We have used an inductor (Lg) which is responsible for matching. For a circuit to transfer maximum power it is required that load resistance (RL) has to be equal to the source resistance (Rs). The source resistance Rs=50 ohm, we need to match this to MOSFET impedance but we know that input impedance of common source MOSFET is purely capacitive. In order to get resistive input impedance at MOSFET, we need to resonate capacitance(Cgs) of MOSFET with the inductor. We are using one inductor(Lg) for matching and another inductor (Ls) as a degenerative inductor. So the capacitance of MOSFET oscillates with both the inductors (Lg+Ls). We do a small signal analysis of MOSFET to get appropriate values of Ls and Lg.

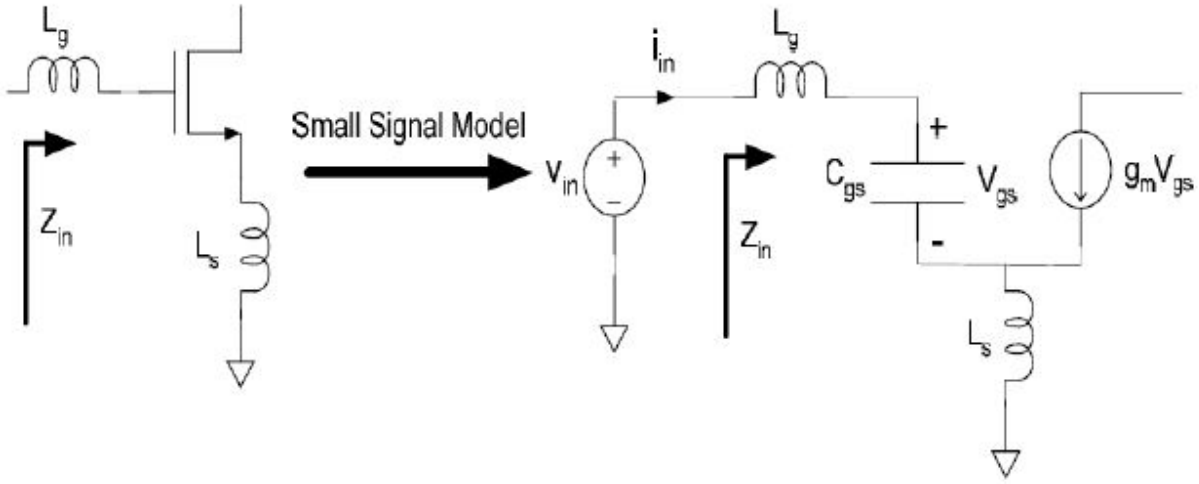

Figure 3: Small signal analysis

Applying KVL, we get

$V_{in} = I_{in} (Xg + Xcg) + (I_{in} + gm*Vgs)* Xs$----------1

$Vgs = I_{in} * Xcg$----------2

Where Xg = j*w*Lg, Xcg = 1/(j*w*Cgs), Xs = j*w*Ls Z

Substituting eq 2 in 1

$V_{in} = I_{in} (Xg + Xcg + Xs + gm*Xcg*Xs)$

$V_{in} = I_{in} \{ j*w*Lg + 1/(j*w*Cgs) + j*w*Ls + gm * [1/ (j*w*Cgs)]*j*w*Ls \}$

$Zin = V_{in}/I_{in} = j*w*Lg + 1/(j*w*Cgs) + j*w*Ls + gm * [1/ (j*w*Cgs)]*j*w*Ls$

$Zin = j*w *(Lg+Ls) + 1/(j*w*Cgs) +(gm *Ls)/Cgs$----------3

From equation 3, we can understand that with appropriate values of Lg and Ls we can eliminate capacitive input impedance of MOSFET and make Zin resistive. With this strategy, we ensure that the input impedance of resistance is resistive.

For maximum power transfer from the antenna to low noise amplifier, Rs should be equal to RL. Here, RL = Zin

So, $Rs = (gm *Ls)/Cgs$ ----------4

Design Parameter Ls

In LNA design the value of Ls is usually assumed and Lg, Cgs are calculated from Zin expression[3]. The value of Ls is arbitrary, so we choose Ls as 0.5 nH for our design. Later, we can optimize or tune the circuit for better performance.

Ls = 0.5 nH

Design Parameter W_T

The cutoff frequency W_T is given by

$W_T = gm/Cgs = Rs/Ls$ From [4]

$W_T = 50/0.5n$ Since Rs = 50 ohms amd Ls =0.5 nH

$W_T =$ 100 G rad/sec

Parameter Wo

The resonant frequency Wo is given by

$Wo = 2*pi*f = 2*3.14*2.5G$

Wo = 16.964 G rad/sec

Parameter Q

$Q = sqrt(1 + 1/p)$

Where $p = [delta * (alpha)^2] / (5*gamma)$

The values of delta, alpha and gamma are dependent on CMOS technology. In 65nm technology, gamma is automatically calculated during simulation so the parameter gamma is not specified. So we assume typical values of Q which lie between 3 to 4.

Considering Q = 4

Parameter Lg

Parameter Lg is calculated using the relation,

$Q = Wo * (Ls + Lg) / Rs$

$Lg = -Ls + (Q * Rs)/Wo$

On substituting values of Wo, Rs and Q, we get Lg as

Lg = 11.299 nH

Usually, inductor value beyond 10nH is not chosen for the design. So we approximate Lg = 10nH.

Parameter Cgs

Resonating frequency, $(Wo)^2 = 1/[Cgs * (Ls +Lg)]$

$Cgs = 1/[(Wo^2)*(Ls+Lg)]$

Cgs = 0.333 pF

Parameter W

Tox for 65nm technology, tox = 1.85 x 10^(-9)

Lmin = 50 nm

Cox = eox/tox = [3.9 * 8.854 * 10^(-12)] / [1.85 x 10^(-9)]

Cox = 18.665 x 10^(-3)

W = [3 * Cgs]/[2*Cox*Lmin]

On substituting Cgs and Cox in W, we get

W = [3 * 0.333 x 10^(-12)]/[2*18.665 x 10^(-3)*50 x 10^-9]

W = 5.35 x 10^(-4)

W = 535 um

Parameter gm

Gm = W_T * Cgs

Gm = 100 G * 0.535 p

Gm = 53.5 mS

Parameter overdrive

Voverdrive = Vgs - Vt

Device mobility, u_n= 0.0491

Vt = 0.423 V

Vgs - Vt = (Gm*Lmin)/(u_n*Cox*W)

Vgs - Vt = 5.45 mV

Bias current ID

Id = (½) * Gm*(Vgs -Vt)

Id = 145.78 uA

3.5.3 RESULTS:

Calculated parameters are used to specify model parameters in ADS. S parameter, Noise and input matching analysis was done.

Initially, the gain was found to be around 10dB. We tried to attain an S parameter S11 < -10dB at the required frequency range and tuned the parameters Lg to achieve higher gain ensuring better matching. We were also successful in reducing the bias current to 74uA. The results which we obtained are as follows:

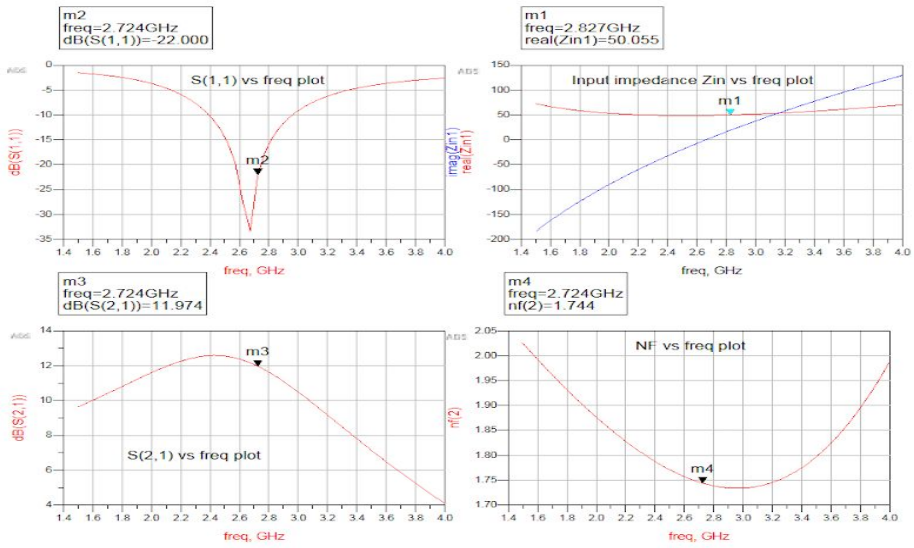

Figure 4: Results of Design 1

At frequency 2.724GHz we obtained S11 around -22 dB this indicates there is no power reflected and maximum power is transmitted from source resistance to load. The gain of LNA was around 11.974 dB. Noise factor of about 1.744 was achieved.

Frequency	2.724 GHz
Gain	11.974 dB
Noise figure	1.744
Input impedance	50.002 ohms
Power consumption	37.25 uW

Table 3. Tabulation of Design 1 results

Common source LNA has better noise performance but the gain obtained by using this MOSFET is less as per our specification we need the gain to be greater than 20dB.

Chapter 4

4.1 DESIGN 2 - CASCODE LNA

Cascode LNA promises high power gain, good noise performance, low power consumption. In lower bands of microwave frequencies, the noise sources of the upper transistor of the cascode stage (cascode transistor) are degenerated by the lower transistor output impedance. Consequently, the cascode stage has superior noise performance. Unfortunately, excellent noise and gain performance of the cascode stage degrades in very high frequencies. This is due to substrate parasitic admittance at the drain-source common node that increases as frequency increases. Like a CS stage, the cascode stage is proper for narrowband applications.

4.1.1 Schematic

A MOSFET [M2] is stacked at the drain of common source LNA. This is designed with the same parameters as discussed. Some optimization and tuning are done to improve performance.

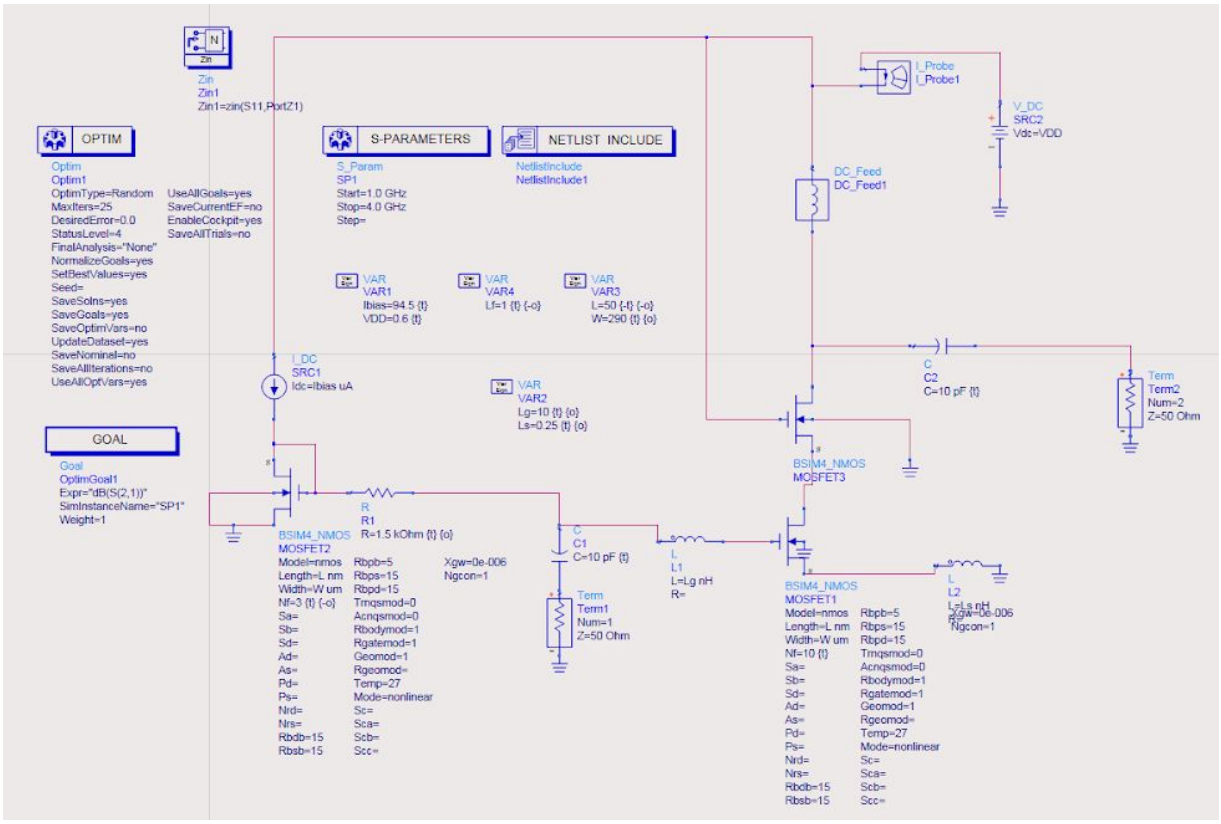

Figure 5: Schematic of Design 2

4.1.2 RESULTS

The gain obtained was greater than 12 dB. We can see an increase in nf from the previous case. Bias current used is 94.5uA. The supply VDD used is 0.6 V. Power consumed, in this case, is more than common source as we need to drive two MOSFETs.

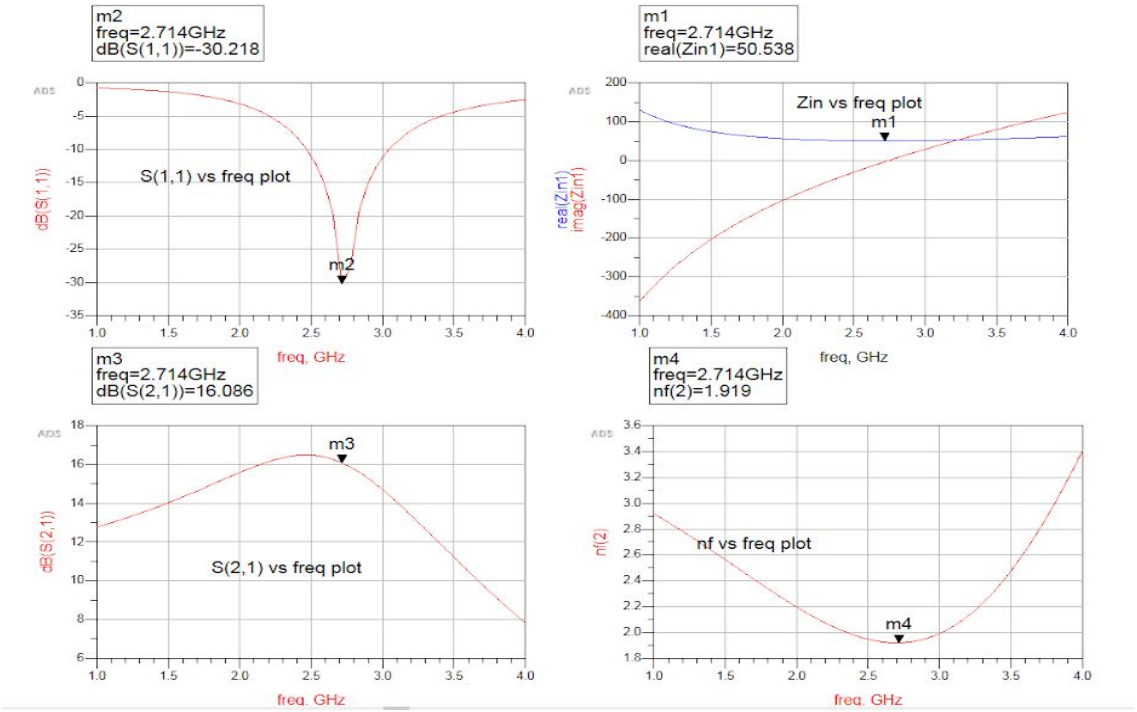

Figure 6: Results of Design 2

The gain obtained from this LNA design for frequency 2.714 GHz was 16.086 dB and Noise Figure of about 1.919. S11 is -30.218 representing good input matching.

Frequency	2.714 GHz
Noise figure	1.919
Input impedance, Zin (mag)	50.538 ohms
Gain	16.086 dB

Table 4. Tabulation of Design 2 results

4.1.3 NON - LINEARITY ANALYSIS

To analyse non-linearity of the system, we do analyze 1-dB compression point and Harmonics analysis.

GAIN COMPRESSION:

All amplifiers have a limit to the strength of the signal they can amplify with constant gain. As the input signal gets stronger, a point is reached where the output doesn't increase to the same degree as the input; that is, the gain is reduced. A measure for this property is called the 1 dB compression point.

HARMONIC DISTORTION:

If a sinusoid is applied to a nonlinear system, the output generally exhibits frequency components that are integer multiples ("harmonics") of the input frequency. In many RF circuits, harmonic distortion is unimportant or an irrelevant indicator of the effect of nonlinearity. For example, an amplifier operating at 2.4 GHz produces a second harmonic at 4.8 GHz, which is greatly suppressed if the circuit has a narrow bandwidth.

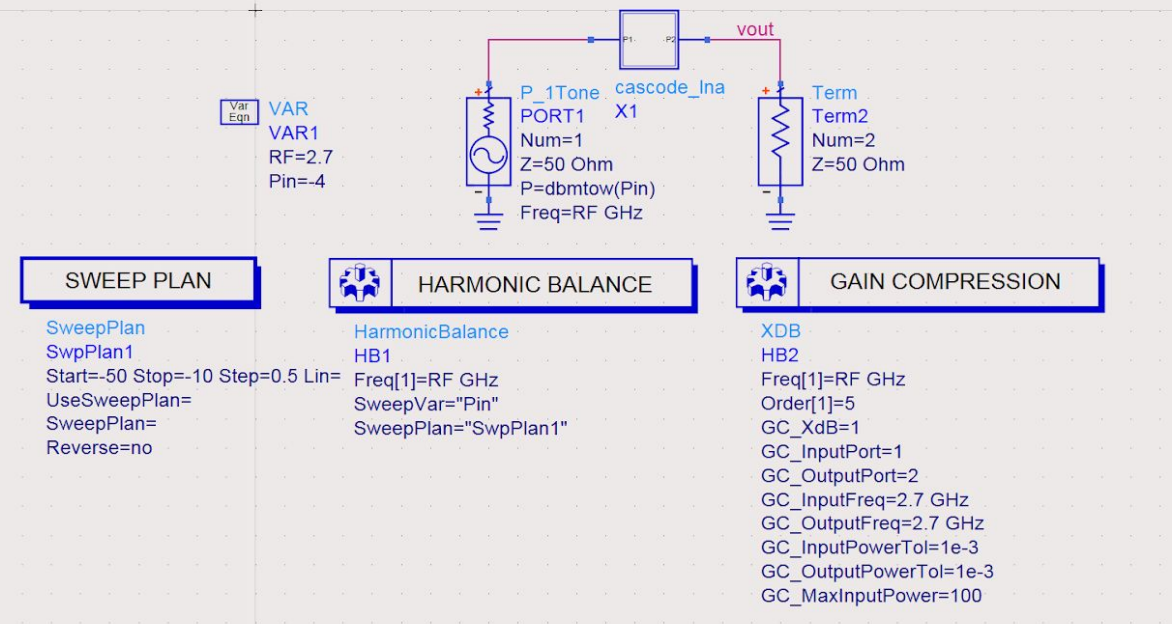

Figure. 7: Schematic of Design 2 for linearity analysis

4.1.4 RESULTS:

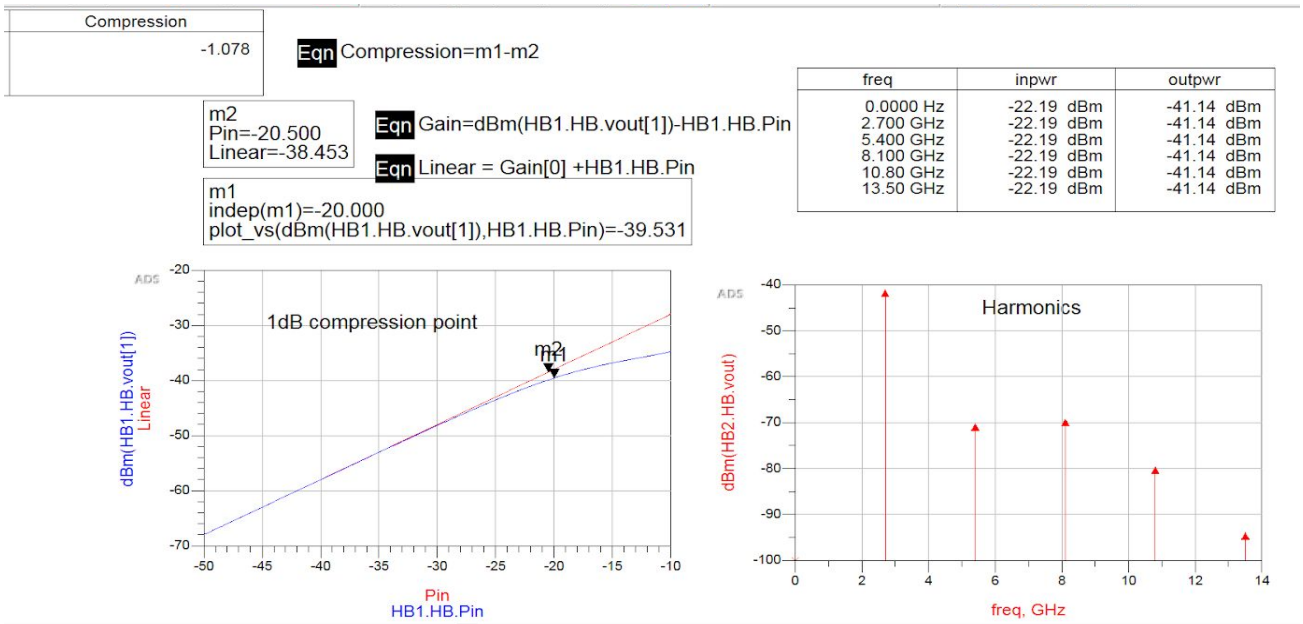

Figure 8: Non-Linearity analysis for design 2

As per the theory, we have plotted Output P1dB vs Input P1dB. Points m1 and m2 are adjusted to get 1dB compression. Gain and Linear equations are used to plot the 1dB compression point. We can observe that the second harmonic is somewhat attenuated due to narrowband.

CHAPTER 5

5.1. DESIGN 3: CASCADE LNA

5.1.1 SCHEMATIC

Additional amplifier (MOSFET M3) is cascaded with the design-2. The gate of M3 is driven by the cascode LNA. With this cascade stage, further amplification of the cascoded signal is observed which indicates we will obtain gain more than the previous cascode design.

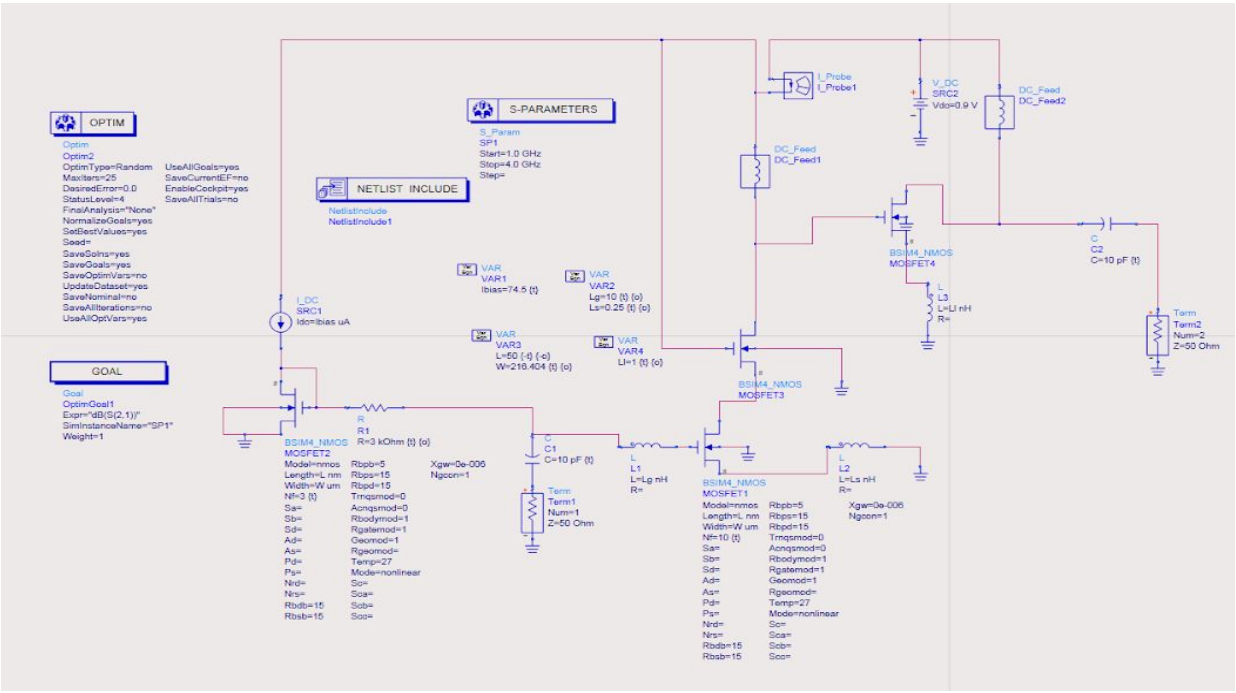

Figure 9: Schematic of design 3

5.1.2 RESULTS

The gain obtained in cascade LNA is greater than 20 dB. Simulation results after tuning and optimization are as follows.

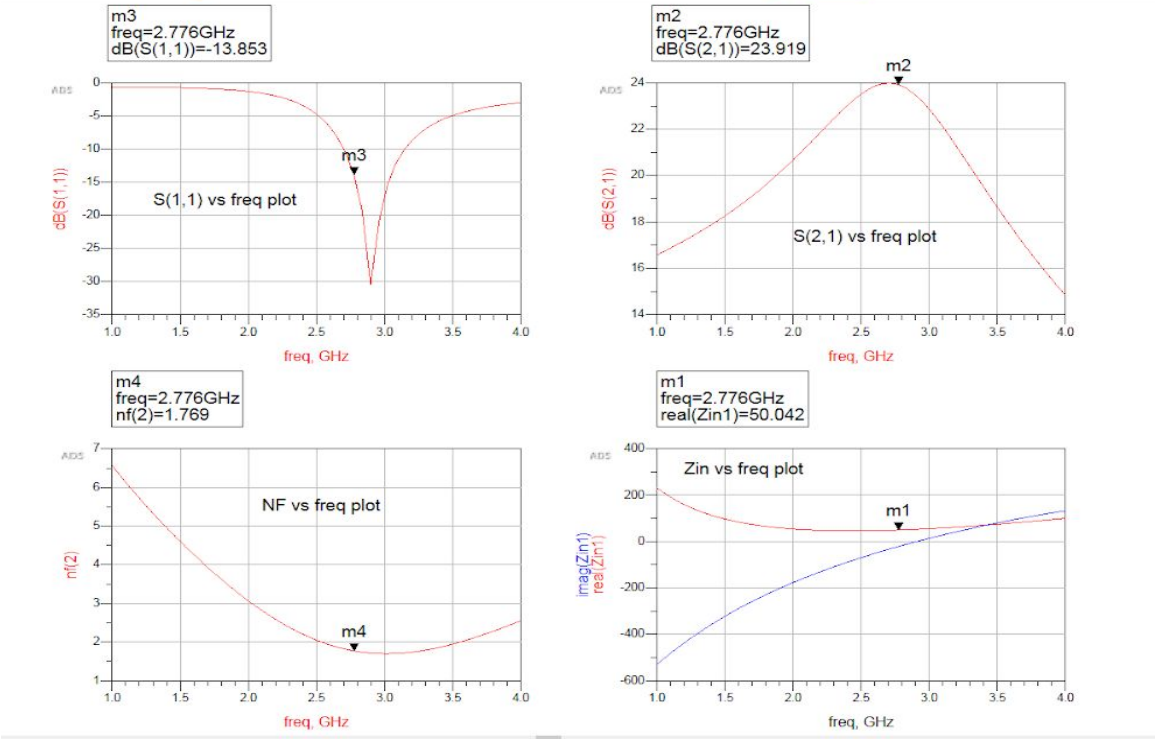

Figure 10. Results of design 3

The gain obtained at 2.776 GHz frequency is about 23.919 dB and noise factor of 1.779. With these results, we can say that the cascade amplifier has a very high gain when compared to the cascode.

Frequency	2.776 GHz
Gain	23.919 dB
Noise figure	1.779
Input impedance Zin (mag)	50.042 ohms

Table 5: Tabulation of Design 3 results

5.1.3 NON - LINEARITY ANALYSIS RESULTS:

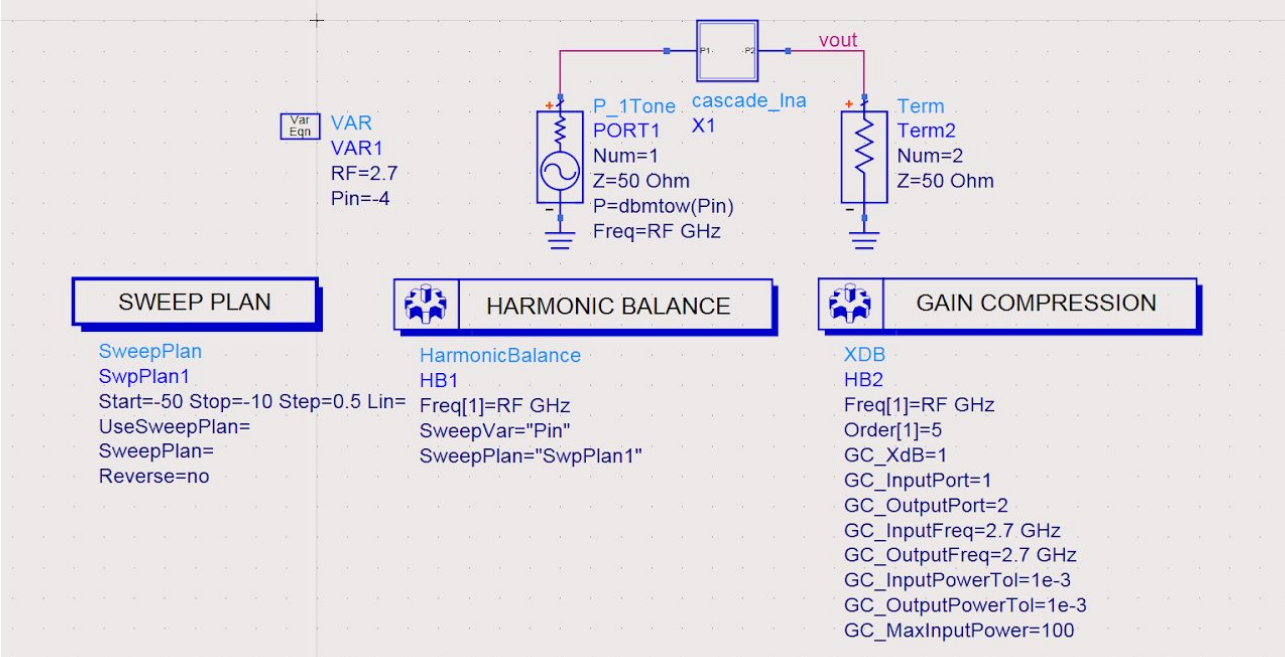

Figure 11: Schematic of Design-3 for linearity analysis

RESULTS:

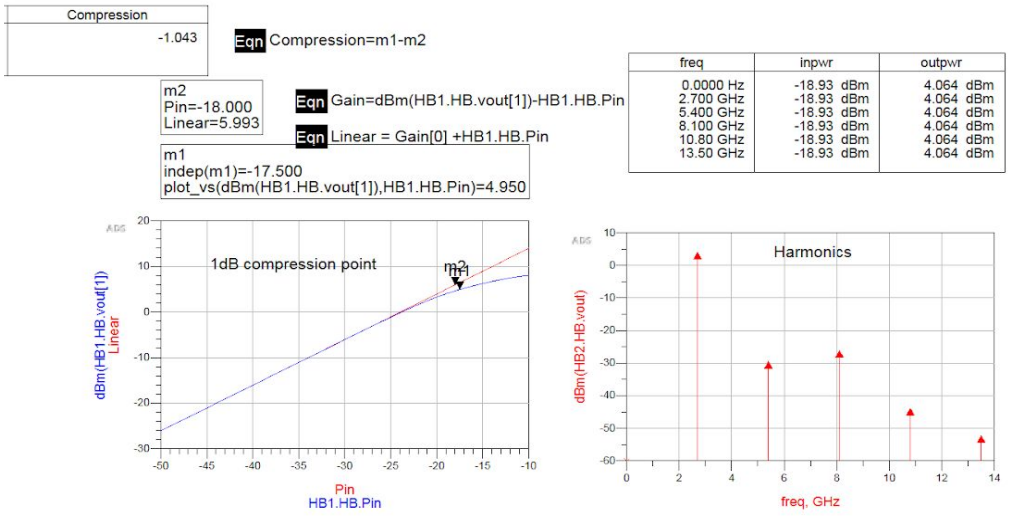

Figure 12: Nonlinearity analysis for design 3

Similar results were obtained in the cascode LNA. This non-linearity is due to the non-linearity of MOSFET and at some stage supply voltage limits the gain.

CHAPTER 6

6.1 COMPARISON OF RESULTS

Parameters	Design-1 (Common source LNA)	Design-2 (Cascode LNA)	Design-3 (Cascade LNA)
Technology	65nm	65nm	65nm
Supply voltage (V)	0.5	0.6	0.9
Frequency (GHz)	2.724	2.714	2.776
Gain (dB)	11.974	16.086	23.919
Noise factor	1.744	1.919	1.799

Table 6: Comparison of all designs

From the tabulation column, we can observe that gain observed in cascade LNA is high when compared to other design topologies. We notice that higher supply voltage to drive cascade LNA is high since it has to drive three MOSFETs. We can observe a slight increase in noise factor in cascode LNA which can be minimized in cascade LNA.

6.2 CONCLUSION

Theoretical study of different LNA topologies was verified practically. Basic principles of matching circuits were analysed. We started initially with source degenerated LNA design, for the same schematic we added cascode stage to improvise gain and noise figure. To improve the gain of LNA drastically, we cascaded LNA in which we achieved a gain of about 23.919 dB at frequency 2.7 GHz. This LNA can be used for S-band applications. Cascade and cascode LNA are suitable for narrowband LNA design. In narrow band impedance matching is easier but as we proceed to Wideband LNA different strategies have to be used.

6.3 FUTURE WORK

Designing LNA for Broadband implications at microwave frequencies. Along with LNA other chains of blocks like mixers, etc in receivers can be designed for specific applications.

6.4 REFERENCES

- Kusuma M.S, S. Shanthala and Cyril Prasanna Raj, "Design of Common Source Low Noise Amplifier with Inductive Source Degeneration in Deep Submicron CMOS Processes" | 2018.
- NXP Semiconductor blog, "Practical Considerations for Low Noise Amplifier Design", by Tim Das.
- NPTEL Lectures by Chatterjee
- "The Design of CMOS RF Integrated circuits", Thomas H Lee
- "RF Microelectronics", Razavi